CONTROL DATA

60463540

AT478-A/B, AT481-A/B
IOU AND ASSOCIATED EQUIPMENT

L0-L3 THEORY / DIAGRAMS

VOLUME 1

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (08-20-86)	Preliminary release.
B (11-07-86)	Manual released. Due to extensive changes to this manual, no change bars or dots have been used. This publication was previously part of publication number 60462210. This edition obsoletes all previous editions.
C (08-31-87)	Manual revised to include: Engineering Change Order 48479 which changes diagrams EXTI-ISI 3.1, 3.2, 3.3, and 3.5; Engineering Change Order 48330 which changes diagrams IOU 2.4 and 2.5; and Engineering Change Order 48633 which changes diagram TPM 3.6. This edition also adds DMA-170 0.0, 1.0 through 1.6, 2.0, BASI-170 3.0 through 3.8, EXTI-170 3.0 through 3.6, and A/D-170 3.0 through 3.6 diagrams and levels 0 and 1 theory of operation; and changes A-1. This edition also adds theory of operation for IOU 1.0 through 1.28 and updates the associated IOU diagrams; adds theory of operation for MAC 3.0 through 3.10; and adds diagrams IPI 0.0, 1.0 through 1.4, 2.0, BASI-IPI 3.0 and 3.1, EXTI-IPI 3.0 through 3.3, and A/D-IPI 3.0 through 3.6. Because extensive changes are made, change bars and dots are not used and all pages reflect the latest revision level. This edition obsoletes all editions.
D (01-30-88)	Manual revised to include: Engineering Change Order 48855 which changes Front Cover, 1-2 and diagrams, IPI 0.0, IPI 1.0, IPI 1.1, IPI 1.2, IPI 1.3, IPI 1.4, IPI 2.0, BASI-IPI 3.0, BASI-IPI 3.1, EXIT-IPI 3.0, EXIT-IPI 3.1, EXIT-IPI 3.2, EXIT-IPI 3.3, A/D-IPI 3.0, A/D-IPI 3.1, A/D-IPI 3.2, A/D-IPI 3.3, A/D-IPI 3.4, A/D-IPI 3.5, A/D-IPI 3.6. This edition also adds IPI theory of operation levels 0 and 1.
E (01-30-88)	Manual revised to include: Field Change Order 48862 which changes diagrams DMA-170 1.0, DMA-170 1.1, DMA-170 1.4, DMA-170 2.0, BASI-170 3.2, BASI-170 3.3, BASI-170 3.5, EXIT-170 3.2, EXIT-170 3.3, EXIT-170 3.5, and abbreviations pages A-1 and A-2.
F (08-10-88)	Manual revised; includes Field Change Order 49637. Also includes Engineering Change Orders 49486, 49487, and 49505. Pages 1-1, 1-3, 1-5, 1-28, 1-30, 1-31, 1-32, 1-43, 2-8, 3A-2, 3A-4, 3A-63, 3A-84, 3C-9, 3C-22, 3C-26, 3C-29, 3C-30, 3C-32, 3C-33, 3C-38, 3C-40, 3C-42, and A-1 are revised. Pages B-1 and B-2 are added.
G (08-10-88)	Manual revised; includes Engineering Change Order 49768. Pages 1-2, 1-38, 1-39, 1-41/1-42, 2-3, 2-4, 2-5, 2-6, 3A-28, 3A-29, 3A-30, 3A-37, 3A-39, 3A-40, 3A-41, 3A-45, 3A-53/3A-54, 3A-60, and 3A-61/3A-62 are revised.
H (09-27-88)	Manual revised; includes Field Change Order 49132. Changes pages 2-1, 3A-3, and 3A-5.

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REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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REVISION RECORD

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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AT478-A	01	-	Released
	02	47441	
	03	47450	
	04	ECO 47840	
	05	47727	
	06	47740	
	07	47748	
	08	48197	
	09	48326	
	10	48400	
	11	48318	
	12	48478	
	13	48631	
	14	48632	
	15	ECO 48404	
AT478-B	01	-	Released
AT481-A	01	-	Released
	02	ECO 47840	
	03	47748	
	04	48326	
	05	48400	
	06	48318	
	07	ECO 48494	
	08	48632	
	09	ECO 49485	
AT481-B	01	-	Released
AT482-A	01	-	Released
	02	ECO 49485	
AT482-B	01	-	Released
AT490-A	01	-	Released
	02	48479	
	03	ECO 49485	
AT490-B	01	-	Released
AT497-A	01	-	Released
	02	ECO 49485	
	03	ECO 49637	
AT497-B	01	-	Released
AT498-A	01	-	Released
	02	48862	
	03	ECO 49485	
AT498-B	01	-	Released
AT501-A	01	-	Released
AT501-B	01	-	Released
AT501-C	01	-	Released
AT509-A	01	-	Released
AT510-A	01	-	Released

PREFACE

This manual is for use in training personnel to understand the equipment and for use by Qualified Engineering Services personnel in maintaining and repairing it.

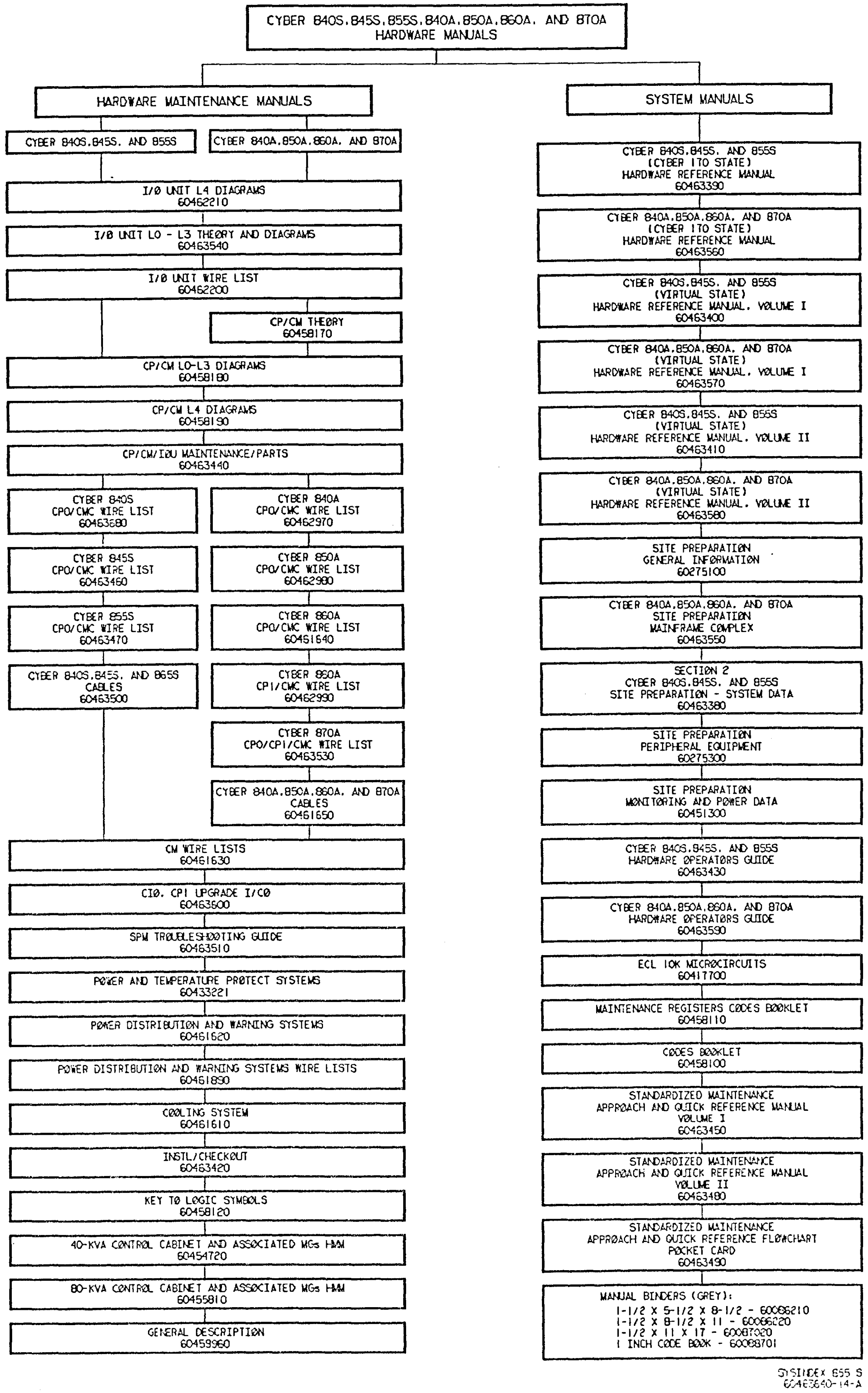
The manual contains the multi-level diagram set for:

- AT478-A Nonconcurrent Input/Output (NIO) Unit
- AT478-B CYBER 180 Input/Output Unit
- AT481-A 1st Concurrent PP Increment Input/Output (CIO) Unit
- AT481-B IOU DMA Expansion
- AT482-A 2nd Concurrent PP Increment Input/Output (CIO) Unit
- AT482-B 2nd Concurrent PP Increment Input/Output (CIO) Unit
- AT490-A Direct-Memory Access (DMA) Enhanced Intelligent Standard Interface (ISI) Channel Adapter
- AT490-B Direct-Memory Access (DMA) Enhanced Intelligent Standard Interface (ISI) Channel Adapter
- AT497-A AT490-A Direct-Memory Access (DMA) Enhanced Intelligent Peripheral Interface (IPI) Channel Adapter
- AT497-B AT490-A Direct-Memory Access (DMA) Enhanced Intelligent Peripheral Interface (IPI) Channel Adapter
- AT498-A Direct-Memory Access (DMA) Enhanced CYBER 170 Channel Adapter
- AT498-B Direct-Memory Access (DMA) Enhanced CYBER 170 Channel Adapter
- AT501-A CYBER 990 Secondary I4 Conversion Kit
- AT501-B CYBER 840/850/860 Secondary I4 Conversion Kit
- AT501-C CYBER 994 Secondary I4 Conversion Kit
- AT509-A IOU to CYBER 960 CM Interface
- AT510-A IOU to CYBER 994 CM Interface

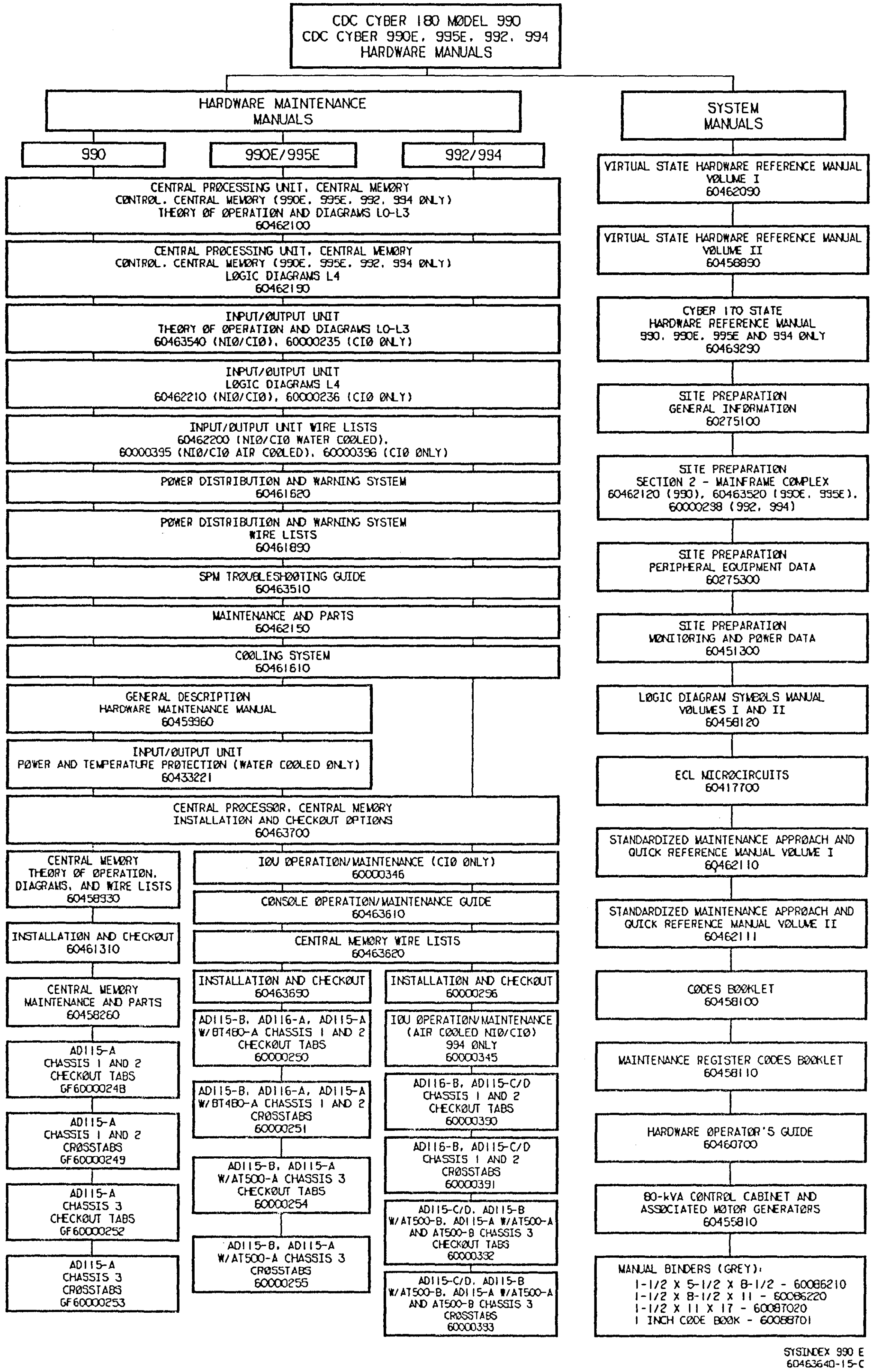
CONVENTIONS

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather then content has changed.

SYSTEM PUBLICATION INDEX


CYBER 840S,845S,855S,840A,850A,860A, AND 870A HARDWARE MANUALS
HARDWARE MAINTENANCE MANUALS
CYBER 840S,845S, AND 855S
CYBER 840A,850A,860A, AND 870A
I/O UNIT L4 DIAGRAMS 60462210
I/O UNIT LO - L3 THEORY AND DIAGRAMS 60463540
I/O UNIT WIRE LIST 60462200
CP/CM THEORY 60458170
CP/CM LO-L3 DIAGRAMS 60458180
CP/CM L4 DIAGRAMS 60458190
CP/CM/IOU MAINTENANCE/PARTS 60463440
CYBER 840S CPO/CMC WIRE LIST 60463680
CYBER 845S CPO/CMC WIRE LIST 60463460
CYBER 855S CPO/CMC WIRE LIST 60463470
CYBER 840S,845S, AND 865S CABLES 60463500
CYBER 840A CPO/CMC WIRE LIST 60462970
CYBER 850A CPO/CMC WIRE LIST 60462980
CYBER 860A CPO/CMC WIRE LIST 60461640
CYBER 860A CPI/CMC WIRE LIST 60462990
CYBER 870A CPO/CPI/CMC WIRE LIST 60463530
CYBER 840A,850A,860A, AND 870A CABLES 60461650
CM WIRE LISTS 60461630
CIO, CPI UPGRADE I/CO 60463600
SPM TROUBLESHOOTING GUIDE 60463510
POWER AND TEMPERATURE PROTECT SYSTEMS 60433221
POWER DISTRIBUTION AND WARNING SYSTEMS 60461620
POWER DISTRIBUTION AND WARNING SYSTEMS WIRE LISTS 60461890
COOLING SYSTEM 60461610
INSTL/CHECKOUT 60463420
KEY TO LOGIC SYMBOLS 60458120
40-KVA CONTROL CABINET AND ASSOCIATED MGs HMM 60454720
80-KVA CONTROL CABINET AND ASSOCIATED MGs HMM 60455810
GENERAL DESCRIPTION 60459960
SYSTEM MANUALS
CYBER 840S,845S, AND 855S (CYBER 170 STATE) HARDWARE REFERENCE MANUAL 60463390
CYBER 840A,850A,860A, AND 870A (CYBER 170 STATE) HARDWARE REFERENCE MANUAL 60463560
CYBER 840S,845S, AND 855S (VIRTUAL STATE) HARDWARE REFERENCE MANUAL, VOLUME I 60463400
CYBER 840A,850A,860A, AND 870A (VIRTUAL STATE) HARDWARE REFERENCE MANUAL, VOLUME I 60463570
CYBER 840S,845S, AND 855S (VIRTUAL STATE) HARDWARE REFERENCE MANUAL, VOLUME II 60463410
CYBER 840A,850A,860A, AND 870A (VIRTUAL STATE) HARDWARE REFERENCE MANUAL, VOLUME II 60463580
SITE PREPARATION GENERAL INFORMATION 60275100
CYBER 840A,850A,860A, AND 870A SITE PREPARATION MAINFRAME COMPLEX 60463550
SECTION 2 CYBER 840S,845S, AND 855S SITE PREPARATION - SYSTEM DATA 60463380
SITE PREPARATION PERIPHERAL EQUIPMENT 60275300
SITE PREPARATION MONITORING AND POWER DATA 60451300
CYBER 840S,845S, AND 855S HARDWARE OPERATORS GUIDE 60463430
CYBER 840A,850A,860A, AND 870A HARDWARE OPERATORS GUIDE 60463590
ECL 10K MICROCIRCUITS 60417700
MAINTENANCE REGISTERS CODES BOOKLET 60458110
CODES BOOKLET 60458100
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE MANUAL VOLUME I 60463450
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE MANUAL VOLUME II 60463480
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE FLOWCHART POCKET CARD 60463490
MANUAL BINDERS (GREY):
1-1/2 X 5-1/2 X 8-1/2 - 60086210
1-1/2 X 8-1/2 X 11 - 60086220
1-1/2 X 11 X 17 - 60087020
1 INCH CODE BOOK - 60088701
SYSINDEX 855 S
60463640-14-A

SYSTEM PUBLICATION INDEX


CDC CYBER 180 MODEL 990
CDC CYBER 990E, 995E, 992, 994
HARDWARE MANUALS
HARDWARE MAINTENANCE MANUALS
990
990E/995E
992/994
CENTRAL PROCESSING UNIT, CENTRAL MEMORY CONTROL, CENTRAL MEMORY (990E, 995E, 992, 994 ONLY) THEORY OF OPERATION AND DIAGRAMS LO-L3 60462100
CENTRAL PROCESSING UNIT, CENTRAL MEMORY CONTROL, CENTRAL MEMORY (990E, 995E, 992, 994 ONLY) LOGIC DIAGRAMS L4 60462150
INPUT/OUTPUT UNIT THEORY OF OPERATION AND DIAGRAMS LO-L3 60463540 (NIO/CIO), 60000235 (CIO ONLY)
INPUT/OUTPUT UNIT LOGIC DIAGRAMS L4 60462210 (NIO/CIO), 60000236 (CIO ONLY)
INPUT/OUTPUT UNIT WIRE LISTS 60462200 (NIO/CIO WATER COOLED), 60000395 (NIO/CIO AIR COOLED), 60000396 (CIO ONLY)
POWER DISTRIBUTION AND WARNING SYSTEM 60461620
POWER DISTRIBUTION AND WARNING SYSTEM WIRE LISTS 60461890
SPM TROUBLESHOOTING GUIDE 60463510
MAINTENANCE AND PARTS 60462150
COOLING SYSTEM 60461610
GENERAL DESCRIPTION HARDWARE MAINTENANCE MANUAL 60459960
INPUT/OUTPUT UNIT POWER AND TEMPERATURE PROTECTION (WATER COOLED ONLY) 60433221
CENTRAL PROCESSOR, CENTRAL MEMORY INSTALLATION AND CHECKOUT OPTIONS 60463700
CENTRAL MEMORY THEORY OF OPERATION, DIAGRAMS, AND WIRE LISTS 60458930
INSTALLATION AND CHECKOUT 60461310
CENTRAL MEMORY MAINTENANCE AND PARTS 60458260
AD115-A CHASSIS 1 AND 2 CHECKOUT TABS GF60000248
AD115-A CHASSIS 1 AND 2 CROSSTABS GF60000249
AD115-A CHASSIS 3 CHECKOUT TABS GF60000252
AD115-A CHASSIS 3 CROSSTABS GF60000253
IOU OPERATION/MAINTENANCE (CIO ONLY) 60000346
CONSOLE OPERATION/MAINTENANCE GUIDE 60463610
CENTRAL MEMORY WIRE LISTS 60463620
INSTALLATION AND CHECKOUT 60463690
AD115-B, AD116-A, AD115-A W/BT480-A CHASSIS 1 AND 2 CHECKOUT TABS 60000250
AD115-B, AD116-A, AD115-A W/BT480-A CHASSIS 1 AND 2 CROSSTABS 60000251
AD115-B, AD115-A W/AT500-A CHASSIS 3 CHECKOUT TABS 60000254
AD115-B, AD115-A W/AT500-A CHASSIS 3 CROSSTABS 60000255
INSTALLATION AND CHECKOUT 60000296
IOU OPERATION/MAINTENANCE (AIR COOLED NIO/CIO) 994 ONLY 60000345
AD116-B, AD115-C/D CHASSIS 1 AND 2 CHECKOUT TABS 60000390
AD116-B, AD115-C/D CHASSIS 1 AND 2 CROSSTABS 60000391
AD115-C/D, AD115-B W/AT500-B, AD115-A W/AT500-A AND AT500-B CHASSIS 3 CHECKOUT TABS 60000392
AD115-C/D, AD115-B W/AT500-B, AD115-A W/AT500-A AND AT500-B CHASSIS 3 CROSSTABS 60000393
SYSTEM MANUALS
VIRTUAL STATE HARDWARE REFERENCE MANUAL VOLUME I 60462090
VIRTUAL STATE HARDWARE REFERENCE MANUAL VOLUME II 60458890
CYBER 170 STATE HARDWARE REFERENCE MANUAL 990, 990E, 995E AND 994 ONLY 60463290
SITE PREPARATION GENERAL INFORMATION 60275100
SITE PREPARATION SECTION 2 - MAINFRAME COMPLEX 60462120 (990), 60463520 (990E, 995E), 60000298 (992, 994)
SITE PREPARATION PERIPHERAL EQUIPMENT DATA 60275300
SITE PREPARATION MONITORING AND POWER DATA 60451300
LOGIC DIAGRAM SYMBOLS MANUAL VOLUMES I AND II 60458120
ECL MICROCIRCUITS 60417700
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE MANUAL VOLUME I 60462110
STANDARDIZED MAINTENANCE APPROACH AND QUICK REFERENCE MANUAL VOLUME II 60462111
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SYSINDEX 990 E
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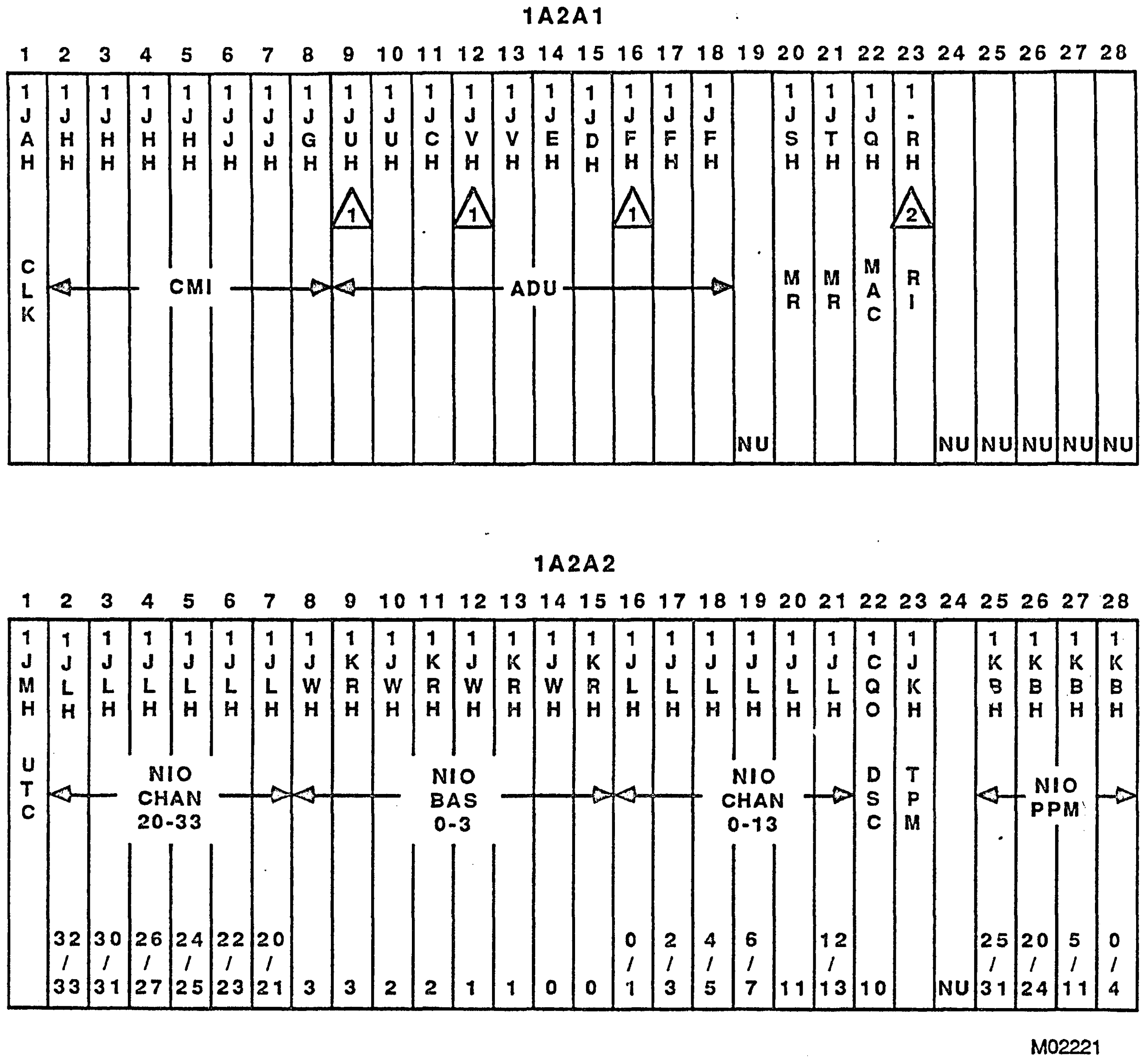

1A2A1

Slot	Module	Note	Function
1	1JAH		CLK
2	1JHH		CMI
3	1JHH		
4	1JHH		
5	1JHH		
6	1JJH		
7	1JJH		
8	1JGH		
9	1JUH	1	ADU
10	1JUH		
11	1JCH		
12	1JVH	1	
13	1JVH		
14	1JEH		
15	1JDH		
16	1JFH	1	
17	1JFH		
18	1JFH		
19	NU		
20	1JSH		MR
21	1JTH		MR
22	1JQH		MAC
23	1-RH	2	RI
24	NU		
25	NU		
26	NU		
27	NU		
28	NU		

1A2A2

Slot	Module	Function	Channel
1	1JMH	UTC	
2	1JLH	NIO CHAN 20-33	32/33
3	1JLH		30/31
4	1JLH		26/27
5	1JLH		24/25
6	1JLH		22/23
7	1JLH		20/21
8	1JWH	NIO BAS 0-3	3
9	1KRH		3
10	1JWH		2
11	1KRH		2
12	1JWH		1
13	1KRH		1
14	1JWH		0
15	1KRH		0
16	1JLH	NIO CHAN 0-13	0/1
17	1JLH		2/3
18	1JLH		4/5
19	1JLH		6/7
20	1JLH		11
21	1JLH		12/13
22	1CQO	DSC	10
23	1JKH	TPM	
24			NU
25	1KBH	NIO PPM	25/31
26	1KBH		20/24
27	1KBH		5/11
28	1KBH		0/4

M02221

NOTES:

1. PROVIDED AS A PART OF AT481-B (IF PRESENT).
2. LOGIC MODULE IS 1HRH IF AT509-A IS INSTALLED OR 1JRH IF AT510-A IS INSTALLED.

Figure 6-3. AT478-B Logic Cage Location Assignments

1. LEVEL 0 and 1 DIAGRAMS

IOU (IOU 0.0) 1-1
- Configuration 1-1
- NIO Units 1-1
  - Central Memory Interface 1-1
  - Assembly/Disassembly Units 1-1
  - Barrels and Slots 1-1
    - A Barrel 1-1
    - C Barrel 1-1
    - K Barrel 1-1
    - P Barrel 1-3
    - Q Barrel 1-3
    - R Barrel 1-3
    - PP Memory 1-3
  - Two-Port Mux 1-3
  - Maintenance Access Control 1-3
  - Maintenance Registers 1-3
  - Display Station Controller 1-3
  - Real Time Clock 1-3
- CIO Units 1-4
  - Assembly/Disassembly Units 1-4
  - Barrels and Slots and ISI Channel Adapters 1-4

CMI Read/Write Data Paths (NIO) (IOU 1.0) 1-6
- CMI Read Data 1-6
  - PP Read Data Path 1-6
  - ISI Channel Read Data Path 1-6
- CMI Write Data 1-6
  - PP Write Data Path 1-6
  - ISI Channel Write Data Path 1-6

CM Response and CM Tag (NIO) (IOU 1.1) 1-8
- Tag In Circuits 1-8
- CM Response Circuits 1-8
- Data Ready Circuits 1-8
- Address Mux 1-8

CM Request and Tag Out Bits (NIO) (IOU 1.2) 1-10
- Request Control and Resync 1-10
- PP Counter 1-10
- BAS/PP Priority 1-10
- Request Counter 1-10
- Tag Out Bits 1-10

Assembly (NIO) (IOU 1.3) 1-14
- ADU Write Data to CM 1-14
- ADU Tag and Function Code Output 1-14
- ADU Exchange 1-14

A4, R4, CM Address, R Data (NIO) (IOU 1.4) 1-16
- BAS Formation of CM Addresses 1-16
- R-to-Y Data Mux 1-16
- CMI Handling of CM Addresses 1-16

C Barrel, I Barrel, K Barrel (NIO) (IOU 1.5) 1-18
- PPM Data Registers 1-18
- K Barrel 1-18
- I Barrel and Instruction Decoding Circuits 1-18
- C Barrel 1-18

A Barrel, R Barrel (NIO) (IOU 1.6) 1-20
- A Barrel 1-20
- A Adder 1-20
- Shifter Y-to-A Mux 1-20
- A Barrel Parity Checking 1-20
- R Barrel 1-20

P Barrel, R Barrel, Q Barrel (NIO) (IOU 1.7) 1-22
- P Barrel and P Slot Circuits 1-22
- Q Barrel and Q Slot Circuits 1-22
- 4K/8K Memory Select Circuits 1-22

PP Memory (NIO) (IOU 1.8) 1-24
- PPM Functions 1-24
- PPM Configuration 1-24
- PPM Error Checking 1-24

IOU Channels 0-7, 11-13, 20-27, 30-33 (NIO) (IOU 1.9) 1-26
- Channel Selection 1-26
- Even/Odd Channel Control 1-26
- I/O Data 1-26

Channel 14 (Real Time Clk), Channel 15, Channel 17 (NIO) (IOU 1.10) 1-28
- Channel 14 1-28
- Channel 15 1-28
- Channel 17 1-28

Two Port Mux (NIO) (IOU 1.11) 1-30
- Z80 Microprocessor 1-30
- EPROM 1-30
- Channel 15 Interface 1-30
- Function Data Output Ports 1-30
- PP and Deadstart Number Counters 1-30
- Data Transfers 1-30
  - CC634 Display Terminal or CC598 System Console to Channel 15 1-30
  - Channel 15 to CC634 Display Terminal or CC598 System Console 1-32
  - Packet Data (CC598 System Console Only) 1-32
  - Transferring of MAC Data 1-32
  - Transferring of DSC Data 1-32

Display Station Controller (NIO) (IOU 1.12) 1-35
- DSC Functions 1-35
- DSC Operations 1-35
  - Operations Done Over Channel 10 1-35
    - Character Mode 1-35

Dot Mode 1-36
Keyboard Input Mode 1-36
Operations with TPM 1-36
Maintenance Access Channel, Radial Interface (NIO) (IOU 1.13) 1-38
MAC Functions 1-38
Error Detector Circuit 1-38
Function Word Decoding 1-38
Serial/Parallel Shifter Register and Pak Selector 1-38
RI Functions 1-38
Maintenance Register A (NIO) (IOU 1.14) 1-40
NIO Fault Status 1 Information 1-40
NIO Status Summary Information 1-40
Error Masking 1-40
Maintenance Register B (NIO) (IOU 1.15) 1-43
NIO Fault Status 2 Information 1-43
NIO EC Bits 1-43
Barrel and Slot Interface (CIO) (IOU 1.16) 1-47
ISI Channel Adapter Functions 1-47
BASI Data Flow 1-47
Data Flow From a PP 1-47
Data Flow to a PP 1-47
Function Decoding 1-47
Control Registers 1-48
Force Error Decoders 1-48
Flag Mask Network 1-48
Barrel and Slot Interface (CIO) (IOU 1.17) 1-50
Operational Status Network 1-50
Adapter PP/DMA Mode Registers 1-50
Adapter Interlock Output Mode Registers 1-50
Channel Flags and Microcode Translator 1-50
Barrel and Slot Interface (CIO) (IOU 1.18) 1-52
T Prime Register and Associated Circuits 1-52
CM Function Code and CM Response Code Translator 1-52
Error Status Network 1-52
MAC Interface and Mux 1-52
External Interface (CIO) (IOU 1.19) 1-55
Port A/B Data Input 1-55
Data Input Buffer 1-55
Valid Sync In Circuits 1-55
Outstanding Request Counter 1-55
ISI One-Second Timeout Circuit 1-55
ISI Busy Circuit 1-55
JZ Board Error Circuit 1-56
Test Features 1-56
Operand Generator and Compare Network 1-56
Transmitter/Receiver Echo 1-56
Inhibit Outstanding Request Counter Bit 1-56
External Interface (CIO) (IOU 1.20) 1-58
Port A/B Data Output 1-58
Port A/B Control Signal Output 1-58
Sync Out Resync Circuits 1-58
Assembly/Disassembly (CIO) (IOU 1.21) 1-60
I Register and Associated Circuits 1-60
CM-Address-to-CMI Circuit 1-60
Assembly/Disassembly (CIO) (IOU 1.22) 1-62
Assembly/Disassembly Circuits 1-62
Counters 1-62
Channel Go/CM Request/CM Response Circuits 1-62
C Barrel, I Barrel, K Barrel (CIO) (IOU 1.23) 1-64
A Barrel, R Barrel (CIO) (IOU 1.24) 1-66
P Barrel, Q Barrel (CIO) (IOU 1.25) 1-68
PP Memory (CIO) (IOU 1.26) 1-70
Maintenance Register A (CIO) (IOU 1.27) 1-72
Maintenance Register B (CIO) (IOU 1.28) 1-74

2. LEVEL 2 DIAGRAMS

BAS 0-3; PPM 0-3 (IOU 2.0) 2-1
BAS 0-3; PPM 0-3 (IOU 2.1) 2-2
CMI Address, CMI Data, CMI Control (IOU 2.2) 2-3
ADU Read Write, Control; A, R Registers (IOU 2.3) 2-4
MAC, Maintenance Register A (IOU 2.4) 2-5
Maintenance Register B, Radial Interface (IOU 2.5) 2-6
CIO BASC 0,1, CIO PPMC 0,1 (IOU 2.6) 2-7
CIO Channels 0-4 (BUS 0), CIO Channels 5-7, 10, 11 (BUS 1) (IOU 2.7) 2-8
CIO Maintenance Registers, CIO Clock (IOU 2.8) 2-9

3A. TPM, MRA, MRB, MAC, BASI-ISI, EXTI-ISI, and A/D-ISI LEVEL 3 DIAGRAMS

Z80 CPU, Address Decoder, EPROMs, RAM, Calendar Clock (JK) (TPM 3.0) 3A-2
Z80 CPU and Bus Drivers 3A-2
Reset Control 3A-2
Power Status Signals 3A-2
Memory Request and I/O Request Signals 3A-2
Address Decoder 3A-2
EPROMs and RAM 3A-2
Input/Output Ports (JK) (TPM 3.1) 3A-4
Battery Circuit 3A-4
Data Input Port 3A-4
Status Input Port 3A-4
Ports 0,1 UARTs 3A-4
Function and Data Output Ports 3A-4
Channel 15 Interface (JK) (TPM 3.2) 3A-6
RI Bus Driver 3A-6
Display Controller/Radial and Channel 15 Interfaces 3A-6
Channel 15 Input Port FIFO Buffers 3A-6
Z80 Data Out Registers, Non-RS232 and Port 0 Data Mux (JK) (TPM 3.3) 3A-8
Holding Register Strobe Control 3A-8
Holding Registers 3A-8
TPM/Status/Data Mux (JK) (TPM 3.4) 3A-10
Z80 Function Decoder (JK) (TPM 3.5) 3A-12
Z80 Function Converter and TTL Decoder 3A-12
Z80 Function Decoder 3A-12
TPM Function Decoder and Interface Control (JK) (TPM 3.6) 3A-14
TPM Function Decoder 3A-14
TPM - Channel 15 Interface Control 3A-14

- Deadstart Channel Number Selector (JK) (TPM 3.7) . . . 3A-16
  - PP and Deadstart Number Counters . . . 3A-16
  - Deadstart Channel Number Mux . . . 3A-16
- Master Clear Generator and Deadstart Branch Tester (JK) (TPM 3.8) . . . 3A-18
  - Master Clear Generator . . . 3A-18
  - Branch Test Timeout Counter . . . 3A-18
  - Deadstart Branch Test . . . 3A-18
- MAC Interface (JS) (MRA 3.0) . . . 3A-21
- Strobe Decoders and PPM Address Register (JS) (MRA 3.1) . . . 3A-22
- Mask Network (JS) (MRA 3.2) . . . 3A-23
- FSI Bytes 0-3 (JS) (MRA 3.3) . . . 3A-24
- FSI Bytes 4-7 (JS) (MRA 3.4) . . . 3A-25
- PP Counters and Error Stop Generator (JS) (MRA 3.5) . . . 3A-26
- Test Mode Network (JS) (MRA 3.6) . . . 3A-27
- Test Mode Register and Read Mux (JS) (MRA 3.7) . . . 3A-28
- Read Mux and MAC Interface (JT) (MRB 3.0) . . . 3A-29
- Mask Network and FS2 Register (JT) (MRB 3.1) . . . 3A-30
- EC Register and Channel Selection (JT) (MRB 3.2) . . . 3A-31
- BAS/PP Selector and Rank Synchronizer (JT) (MRB 3.3) . . . 3A-32
- Connect Code Register, Z80 and MCH Control Mux (JQ) (MAC 3.0) . . . 3A-34
  - Connect Code Register . . . 3A-34
  - Z80 and MCH Control Mux . . . 3A-34
- Z80 Response Control (JQ) (MAC 3.1) . . . 3A-37
  - Z80 Response Control . . . 3A-37
    - Responses Sent to TPM . . . 3A-37
    - I/O Status Passed to RIs . . . 3A-37
    - Tracking of Input/Output Mode . . . 3A-37
  - MCH Signals In - FF Reset Control . . . 3A-37
  - Control Word Request Control . . . 3A-37
- Z80 and MCH Interface, RI Data Mux (JQ) (MAC 3.2) . . . 3A-40
  - Z80 and MCH Interface . . . 3A-40
  - RI Data Mux . . . 3A-40
- Control Word and Type Code Registers and Decoders (JQ) (MAC 3.3) . . . 3A-42
  - Channel Receiver, Type Code Register, and Control Word Register . . . 3A-42
  - Type Code Decoder . . . 3A-42
  - Control Word Encoder . . . 3A-42
- Function Decoder (JQ) (MAC 3.4) . . . 3A-44
  - Function Decoder and Starting Address Encoder . . . 3A-44
  - Clear LED Control . . . 3A-44
  - Master Clear Network . . . 3A-44
- Nanocode Request and MAC Timing Control (JQ) (MAC 3.5) . . . 3A-46
  - Nanocode Request Control . . . 3A-46
  - MAC Timing . . . 3A-46
- Nanocode Control (JQ) (MAC 3.6) . . . 3A-49
  - Nanocode Address Mux Register . . . 3A-49
  - Nanocode ROMs and Parity Check . . . 3A-49
- Data Mux (JQ) (MAC 3.7) . . . 3A-52
  - Byte Counter . . . 3A-52
  - Element ID Mux . . . 3A-52
  - IOU Status Summary Register . . . 3A-52
  - Data Mux . . . 3A-52
  - Channel I/O Register . . . 3A-52
- Bit Serial Control and Shifter (JQ) (MAC 3.8) . . . 3A-55
  - Byte Code Incrementor . . . 3A-55
  - Serial/Parallel Shifter . . . 3A-55
  - Bit-Serial Control . . . 3A-55
- Bit Serial Pak and Input Selector (JQ) (MAC 3.9) . . . 3A-58
  - Bit-Serial Pak Selector . . . 3A-58
  - Input Selector . . . 3A-58
- Error Detector, MCH Control, Timeout Counter (JQ) (MAC 3.10) . . . 3A-60
  - Error Detector . . . 3A-60
  - Channel Communications Controls . . . 3A-60
  - Invert and Resynchronize Control . . . 3A-60
  - MCH Control . . . 3A-60
  - Timeout Counter . . . 3A-60
- Channel Control (JX) (BASI-ISI 3.0) . . . 3A-63
- Channel Data Input/Output (JX) (BASI-ISI 3.1) . . . 3A-64
- Function Register and Decode PROMs (JX) (BASI-ISI 3.2) . . . 3A-65
- Adapter Mode Registers, CM Function Code (JX) (BASI-ISI 3.3) . . . 3A-66
- Control Registers, Force Error Decoder, Flag Mask Network (JX) (BASI-ISI 3.4) . . . 3A-67
- T Register Network (JX) (BASI-ISI 3.5) . . . 3A-68
- CM Response Code Translator, Error Status Network (JX) (BASI-ISI 3.6) . . . 3A-69
- Operational Status Network, MAC Interface (JX) (BASI-ISI 3.7) . . . 3A-70
- Output Buffer Address Counters, Resynchronizer (JZ) (EXTI-ISI 3.0) . . . 3A-71
- Outstanding Request Counter, Pause Control, ISI Busy and Timeout (JZ) (EXTI-ISI 3.1) . . . 3A-72
- Output Buffer, Board Error Detector (JZ) (EXTI-ISI 3.2) . . . 3A-73
- Ports A,B Transmitters and Receivers, Control Signal Input Mux (JZ) (EXTI-ISI 3.3) . . . 3A-74
- Data Input Buffer, PP Input Data Mux (JZ) (EXTI-ISI 3.4) . . . 3A-75
- Input Buffer Word Counter, Synchronizer (JZ) (EXTI-ISI 3.5) . . . 3A-76
- Operand Generator, Compare Network (JZ) (EXTI-ISI 3.6) . . . 3A-77
- Direct Memory Access Data Assembly (JY) (A/D-ISI 3.0) . . . 3A-79
- CM Data Assembly (JY) (A/D-ISI 3.1) . . . 3A-80
- T Register (JY) (A/D-ISI 3.2) . . . 3A-81
- CM Address to CMI (JY) (A/D-ISI 3.3) . . . 3A-82
- Channel Word, CM Word, Response, and Address Counters (JY) (A/D-ISI 3.4) . . . 3A-83
- Assembly/Disassembly Control (JY) (A/D-ISI 3.5) . . . 3A-84
- Error Detector (JY) (A/D-ISI 3.6) . . . 3A-85

3B. 170-DMA LEVELS 0 THROUGH 3 DIAGRAMS 3B-1

- DMA Enhanced C170 Channel Adapter (DMA-170 0.0) . . . 3B-1
  - Adapter Overview . . . 3B-1
  - Function Register and Decode PROMs . . . 3B-1
    - Master Clear (8000) . . . 3B-1
    - Clear T (8200) . . . 3B-1
    - Start DMA Input/Output (84XX/86XX) . . . 3B-1
    - Clear DMA Mode (8800) . . . 3B-1
    - Disable Test Mode (8C00) . . . 3B-1
    - Enable Test Mode (8E00) . . . 3B-2
    - Read Control Register (9000) . . . 3B-2
    - Write Control Register (9200) . . . 3B-2
    - Read Error Status Register (9400) . . . 3B-2
    - Read Operational Status Register (9800) . . . 3B-2
    - Read T (9C00) . . . 3B-2
    - Write T Prime (9E00) . . . 3B-2
  - Control Register . . . 3B-3
    - Enable Cache Invalidate (Bit 48) . . . 3B-3

    - 60-Bit Mode (Bit 50) 3B-3
    - Enable Test Clock (Bit 51) 3B-3
    - Disable External Clock (Bit 52) 3B-3
    - Block Full Out (Bit 53) 3B-3
    - Enable Overflow (Bit 54) 3B-3
    - Disable Error Register Clear (Bit 55) 3B-3
    - Enable Force Error Codes (Bit 56) 3B-3
    - Force Error Codes (Bits 59-63) 3B-3
        - Invert PROM Parity (01) 3B-3
        - Invert Input Data Parity (02) 3B-3
        - Force Invalid Response (04) 3B-3
        - Invert Response Code Parity (05) 3B-4
        - Invert Control Register Parity (06) 3B-4
        - Invert Shifter Parity (10) 3B-4
        - Invert Conversion Parity (11) 3B-4
        - Invert Transmit Register Parity (12) 3B-4
        - Invert Input Parity (13) 3B-4
        - Force Channel Input Parity 0,1 (20/21) 3B-4
        - Force T Parity Low (22) 3B-4
        - Invert Output Parity Upper/Lower (23/24) 3B-4
        - Force Address Parity Prediction Error (25) 3B-4
        - Force Byte Count Equal to Zero (26) 3B-4
- Operational Status Register 3B-5
    - Output Buffer Full (Bit 52) 3B-5
    - Input Buffer Full (Bit 53) 3B-5
    - Data Available to Channel (Bit 54) 3B-5
    - Fast Transfer (Bit 55) 3B-5
    - External Clock Present (Bit 56) 3B-5
    - Test Mode (Bit 57) 3B-5
    - PP Word Count Equal to Zero (Bit 58) 3B-5
    - DMA Output (Bit 59) 3B-5
    - DMA Input (Bit 60) 3B-5
    - DMA Halted (Bit 61) 3B-6
    - T Register Empty (Bit 62) 3B-6
    - Transfer in Progress (Bit 63) 3B-6
- Error Status Register 3B-6
    - Uncorrectable CM Error (Bit 50) 3B-6
    - CM Reject (Bit 51) 3B-6
    - Invalid Response (Bit 52) 3B-6
    - Any Response Code Parity Error (Bit 53) 3B-6
    - CMI Read Data Parity Error (Bit 54) 3B-6
    - Clock Fault (Bit 55) 3B-7
    - Overflow Error (Bit 56) 3B-7
    - Input Data Error (Bit 57) 3B-7
    - 12/16 Conversion Error (Bit 58) 3B-7
    - A/D Data Error (Bit 59) 3B-7
    - BAS Parity Error (Bit 60) 3B-7
    - KZ Error (Bit 61) 3B-7
    - JY Error (Bit 62) 3B-7
    - KX Error (Bit 63) 3B-7
- MAC Interface 3B-8
- DMA Transfers 3B-9
- Fast DMA Transfers 3B-10
- Channel/CM Data Mapping 3B-10
    - Data Paths 3B-11
        - PP to T Prime Register 3B-11
        - PP From T Register 3B-11
        - PP to Function Register, Control Register, and PP Word Counter 3B-11
        - PP from Status and Control Registers 3B-11
        - Inter-PP Transfer 3B-11
        - PP Output Transfer 3B-11
        - PP Input Transfer 3B-11
        - DMA Output Transfer 3B-11
        - DMA Input Transfer 3B-11
    - Test Mode 3B-12
        - PP Transfers 3B-12
        - DMA Transfers 3B-12
- BASC Data Input/Output (DMA-170 1.0) 3B-15
    - Adapter Output Register Rank I 3B-15
    - Adapter Output Parity Checker 3B-15
    - T Register Data In and Out 3B-15
    - External Input Data Mux 3B-15
    - Register Select Mux 3B-15
    - Adapter Input Register Rank II 3B-15
    - Adapter Input Parity Checker 3B-15
    - Microcode Decode 3B-15
    - Channel Flag and Active Flag 3B-16
    - Adapter Full Flags 3B-16
- Control Register, Function Decoding, Operational Status (DMA-170 1.1) 3B-18
    - Function Register 3B-18
    - Function Decode PROMs A Through E 3B-18
    - Power On Master Clear 3b-18
    - T Register Read/Write Control 3B-18
    - DMA Control FF´s 3B-18
    - PP Word Counter 3B-18
    - Operational Status Network 3B-18
    - Control Register 3B-18
    - Force Error Decoders 3B-18
- Error Status, MAC Interface (DMA-170 1.2) 3B-20
    - CM Response Code Translator 3B-20
    - CM Function Code 3B-20
    - Error Status Network 3B-20
    - Error Status Register 3B-20
    - MAC Interface Mux, MAC Interface 3B-20
    - Channel Type Identifier 3B-20
- Data Output, 12/16 Conversion (DMA-170 1.3) 3B-22
    - Output Control Logic 3B-22
    - Output Buffer Address Counters 3B-22
    - Output Resynchronize Network 3B-22
    - Output Resynchronize Buffer 3B-22
    - Transmit Register 3B-22
    - Transmit Enables 3B-22
    - Empty, Active, Inactive Output Networks 3B-22
    - 12/16 Converter Input 3B-22
    - 12/16 Conversion Shifter 3B-22
    - 12/16 Parcel Counter 3B-22
    - Data Accept Network 3B-22
- Data Input, Error Summing, Clock Formation (DMA-170 1.4) 3B-24

- Input Buffer Write, Read Control 3B-24
- Input Receivers and Deskew Register 3B-24
- Input Resynchronize Buffer 3B-24
- Input Buffer Data Merge 3B-24
- Error Summing Network 3B-24
- Control In Resynchronizer 3B-24
- End Transfer Network 3B-24
- External Clock Tuning Network 3B-24
- External Clock T1/T2 Formation 3B-24
- External Clock Detection Network 3B-24
- Clock Formation and Fanout 3B-24

- Assembly/Disassembly, Control Counters (DMA-170 1.5) 3B-26
  - Assembly 3B-26
  - Disassembly 3B-26
  - Counters 3B-26
  - Channel Go/CM Request/CM Response 3B-26
- T Register, Error Summing (DMA-170 1.6) 3B-28
  - T Register 3B-28
  - T Prime Register 3B-28
  - CM Address to CMI 3B-28
- DMA Enhanced C170 Channel Adapter (DMA-170 2.0) 3B-30
- Adapter Output Register, T Register Input/Output (BASI-170 3.0) 3B-31
- External Input Data Mux, Register Select Mux, Adapter Input Register (BASI-170 3.1) 3B-32
- Microcode Decode, Channel Flag, Active Flag (BASI-170 3.2) 3B-33
- Adapter Full Flags (BASI-170 3.3) 3B-34
- Function Decode, T Register Control (BASI-170 3.4) 3B-35
- DMA Control, PP Word Counter, Operational Status Network (BASI-170 3.5) 3B-36
- Control Register, Force Error Decoders (BASI-170 3.6) 3B-37
- CM Response and Function Codes, Error Status Network (BASI-170 3.7) 3B-38
- MAC Interface, Channel Type Indentifier (BASI-170 3.8) 3B-39
- Output Control, Buffer Address Counters, Resynchronize Network (EXTI-170 3.0) 3B-40
- Output Data and Control (EXTI-170 3.1) 3B-41
- Input Data, Data Accept Network (EXTI-170 3.2) 3B-42
- Input Buffer Read and Write Control (EXTI-170 3.3) 3B-43
- Input Buffer, Error Summing Network (EXTI-170 3.4) 3B-44
- Control In Resynchronizer, End Transfer Network (EXTI-170 3.5) 3B-45
- Clock Formation (EXTI-170 3.6) 3B-46
- Direct Memory Access Data Assembly (A/D-170 3.0) 3B-47
- CM Data Disassembly (A/D-170 3.1) 3B-48
- T Register (A/D-170 3.2) 3B-49
- CM Address to CMI (A/D-170 3.3) 3B-50
- Channel Word, CM Word, Response, and Address Counters (A/D-170 3.4) 3B-51
- Assembly/Disassembly Control (A/D-170 3.5) 3B-52
- Error Detector (A/D-170 3.6) 3B-53

3C. IPI LEVELS 0 THROUGH 3 DIAGRAMS 3C-1

- DMA Enhanced IPI Channel Adapter (IPI 0.0) 3C-1
  - Adapter Overview 3C-1
  - Barrel and Slot Interface (BASI) 3C-1
  - External Interface (EXTI) 3C-1
  - Assembly/Disassembly (A/D) 3C-1
  - Function Codes 3C-1
    - Internal Functions 3C-2
    - Bus Control Functions 3C-2
    - Channel Functions 3C-2
  - IPI Status Register 3C-2
  - IPI Error Register 3C-3
  - DMA Control Register 3C-3
  - DMA Operational Status Register 3C-3
  - DMA Error Status Register 3C-3
  - Data Paths 3C-4
    - PP to T Prime Register 3C-4
    - PP from T Register 3C-4
    - PP to Function Register and Control Register 3C-4
    - PP from Error Status, Operational Status, and Control Registers 3C-4
    - Inter-PP Transfer 3C-4
    - PP Output Transfer 3C-4
    - PP Input Transfer 3C-4
    - DMA Output Transfer 3C-4
    - DMA Input Transfer 3C-5
  - Test Mode 3C-5
    - PP Output Transfer 3C-5
    - PP Input Transfer 3C-5
    - DMA Output Transfer 3C-5
    - DMA Input Transfer 3C-5
  - Maintenance Access Control (MAC) Interface 3C-5
- Barrel and Slot Interface (IPI 1.0) 3C-8
  - Data Paths 3C-8
    - BAS Data Bus 3C-8
    - Channel Data Bus 3C-8
    - T Register Data Bus 3C-8
  - Channel Flags and Microcode Translator 3C-8
  - CM Function Code 3C-8
  - CM Response Code 3C-8
  - Error Status 3C-8
  - MAC Control 3C-8
  - MAC Interface 3C-8
- DMA and IPI Arrays, Data Bus, MAC Mux (IPI 1.1) 3C-10
    - Data Paths PP to Function Register and Control Register 3C-10
    - PP from Error Status, Operational Status, and Control Registers 3C-10
    - PP Output Transfer 3C-10
    - PP Input Transfer 3C-10
    - DMA Output Transfer 3C-10
    - DMA Input Transfer 3C-10
  - Test Mode Data Paths 3C-10
    - PP Output Transfer 3C-10
    - PP Input Transfer 3C-10
    - DMA Output Transfer 3C-10
    - DMA Input Transfer 3C-10
  - Power On One Shot 3C-11
  - Dead Man Timeout Oscillator 3C-11
  - LED 3C-11
  - DMA Array 3C-11
    - Internal Function Codes 3C-11
      - Master Clear (0000) 3C-11
      - Read Random Data Generator (0004) 3C-11

        Write Random Data Generator (0014) . . . 3C-11
        Clear IPI Error (0022) . . . 3C-12
        Force Error (0X22) . . . 3C-12
        Set Sync Period (XX42) . . . 3C-12
        External Clock/Port Select (0X62) . . . 3C-13
        Clear Error (0100) . . . 3C-13
        Read Control Register (0200) . . . 3C-13
        Write Control Register (0300) . . . 3C-13
        Select PP from DMA (0400) . . . 3C-13
        Select PP to DMA (0500) . . . 3C-13
        Read Error Status Register (0600) . . . 3C-13
        Read Operational Status Register (0700) . . . 3C-14
        Illegal Function (0900) . . . 3C-14
        Read T Register (0A00) . . . 3C-14
        Write T Prime Register (0B00) . . . 3C-14
        Select IPI to DMA (0C00) . . . 3C-14
        Select DMA to IPI (0D00) . . . 3C-14
        Clear T Prime Registers (0E00) . . . 3C-14
        Illegal Functions (XF00) . . . 3C-14
    Bus Control Functions . . . 3C-15
    Channel Functions . . . 3C-15
        Master Terminate (00A1) . . . 3C-16
        Attention Present (00C1) . . . 3C-16
        Read IPI Status Register (00E1) . . . 3C-16
        Read IPI Error Register (00F1) . . . 3C-16
        Data Transfer Functions (0X81) . . . 3C-16
    Control Register . . . 3C-16
        Enable Cache Invalidate (48) . . . 3C-16
        Enable Test Mode (51) . . . 3C-17
        Inhibit Test Mode Increment (52) . . . 3C-17
        Enable Transfer In Progress Flag (53) . . . 3C-17
        Enable T Prime Empty Flag (54) . . . 3C-17
        Enable Force Error Codes (56) . . . 3C-17
        Force Error Codes (59-63) . . . 3C-17
            Invert Operational Status Parity Upper, Lower (00, 01) . . . 3C-17
            Force T Register Read/Write Counter Parity Error (02) . . . 3C-17
            Force Function Register Parity Error (03) . . . 3C-17
            Force Invalid Response (04) . . . 3C-17
            Invert Response Code Parity (05) . . . 3C-17
            Force BAS Parity Error Upper, Lower (06, 07) . . . 3C-17
            Invert Input Data Parity to BAS (08) . . . 3C-17
            Force PP BAS Input Data Parity Error (09) . . . 3C-17
            Force DMA/IPI Input Data Parity Error Upper, Lower (0A, 0B) . . . 3C-17
            Force Oputput Data Parity Error Upper, Lower (0C, 0D) . . . 3C-18
            Force Error Status Register Parity Error Upper, Lower (0E, 0F) . . . 3C-18
            Force Channel Input Parity 0, 1 (10, 11) . . . 3C-18
            Force T Parity Low (12) . . . 3C-18
            Invert Output Parity Upper, Lower (13, 14) . . . 3C-18
            Force Address Parity Prediction Error (15) . . . 3C-18
            Force Byte Count Equal to Zero (16) . . . 3C-18
            Force Control Register Parity Error (17) . . . 3C-18
            Force Deadman Timer Counter Parity Error (18) . . . 3C-18
    Operational Status Register . . . 3C-18
        Parity Errors (48 through 53) . . . 3C-18
        DMA Transfer in Progress (56) . . . 3C-18
        IPI Transfer in Progress (57) . . . 3C-18
        Output Mode (58) . . . 3C-18
        DMA/IPI Mode (60) . . . 3C-18
        PP/IPI Mode (61) . . . 3C-19
        T Prime Register Empty (62) . . . 3C-19
        Transfer in Progress (63) . . . 3C-19
    Error Status Register . . . 3C-19
        Illegal Function of Sequence (49) . . . 3C-19
        Uncorrectable CM Error (50) . . . 3C-19
        CM Reject (51) . . . 3C-19
        Invalid Response (52) . . . 3C-19
        Response Code Parity Error (53) . . . 3C-19
        CMI Read Data Parity Error (54) . . . 3C-19
        IPI Error (55) . . . 3C-19
        DMA Register Parity Error (56) . . . 3C-19
        MAC Status Parity Error (57) . . . 3C-19
        Timeout (58) . . . 3C-19
        A/D Data Error (59) . . . 3C-19
        BAS Parity Error (60) . . . 3C-19
        LZ Error (61) . . . 3C-20
        JY Error (62) . . . 3C-20
        LX Error (63) . . . 3C-20
    IPI Array . . . 3C-20
        IPI Status Register . . . 3C-20
        IPI Error Register . . . 3C-21
IPI Data Out Mux, Random Data Generator Transmitters, Receivers (IPI 1.2) . . . 3C-23
    Data Paths . . . 3C-23
        PP and DMA Output Transfers . . . 3C-23
        PP and DMA Input Transfers . . . 3C-23
    Test Mode Data Paths . . . 3C-23
        PP and DMA Output Transfers . . . 3C-23
        PP and DMA Input Transfers . . . 3C-23
    Random Data Generator . . . 3C-23
    Maintenance Transfer Control . . . 3C-23
Assembly/Disassembly, Control Counters (IPI 1.3) . . . 3C-25
    Assembly . . . 3C-25
    Disassembly . . . 3C-25
    Counters . . . 3C-25
    Channel Go/CM Request/CM Response . . . 3C-25
T Register, Error Summing (IPI 1.4) . . . 3C-27
    T Register . . . 3C-27
    T Prime Register . . . 3C-27
    CM Address to CMI . . . 3C-27
DMA Enhanced IPI Channel Adapter (IPI 2.0) . . . 3C-29
BAS/Channel and T Register Data, CM Function and Response Code (BASI-IPI 3.0) . . . 3C-30
MAC Interface, Channel Flags (BASI-IPI 3.1) . . . 3C-31
DMA Array and Data Bus, Channel Data Bus (EXTI-IPI 3.0) . . . 3C-32

IPI Array, MAC Mux (EXTI-IPI 3.1) 3C-33
Maintenance Transfer Control, IPI Transmitters/Receivers, Clock Generator (EXTI-IPI 3.2). 3C-34
IPI Data Out Mux, Random Data Generators (EXTI-IPI 3.3) 3C-35
Direct Memory Access Data Assembly (A/D-IPI 3.0). 3C-36
CM Data Disassembly (A/D-IPI 3.1) 3C-37
T Register (A/D-IPI 3.2). 3C-38
CM Address to CMI (A/D-IPI 3.3) 3C-39
Channel Word, CM Word, Response, and Address Counters (A/D-IPI 3.4) 3C-40
Assembly/Disassembly Control (A/D-IPI 3.5). 3C-41
Error Detector (A/D-IPI 3.6). 3C-42

APPENDIXES

A IOU BLOCK DIAGRAM A-1
B ABBREVIATIONS B-1

FIGURES

1-1 Computer System Elements 1-2
1-2 Function Word Format 1-38
1-3 Idle Mode Bus Busy/Attention Bit Format. 1-55

TABLES

1-1 8-Bit to 9-Bit Tag Conversion. 1-8
1-2 Bus 0/1 Tag Bits 3 Through 7 1-12
1-3 Tag Bits 0 Through 2 1-12
1-4 Function Bits 0 Through 3. 1-14
1-5 TPM Function Codes 1-31
1-6 DSC Function Words 1-35
1-7 Horizontal and Vertical Control Signals. 1-36
1-8 NIO Fault Status 1 Information 1-40
1-9 NIO Fault Status 2 Information 1-43
1-10 NIO EC Bits. 1-44
1-11 ISI Adapter Function Codes 1-48
1-12 CIO Fault Status 1 Information 1-72
1-13 CIO Fault Status 2 Information 1-74
3A-1 Start of a MAC Read/Write Operation. 3A-38
3A-2 MAC Operations and Opcodes 3A-44
3A-3 Nanocode Starting Addresses. 3A-49
3A-4 Nanocode Bits. 3A-50
3A-5 Serial Interface Line Selection. 3A-58

VOLUME 2

4. LEVEL 4 DIAGRAMS①

BOOK 1

Panel A

JA† 53575500. 4-1
JA† 22105670. 4-15
JC/JU 53575502. 4-29
JC/JU 22105671. 4-57
JD 4-85
JE/JV 53575504. 4-101
JE/JV 22105672. 4-121
JF 53575505. 4-141
JF 22105620. 4-159
JG 53575506. 4-177
JG 22105673. 4-199
JH 53575507. 4-221
JH 22105679. 4-251
JJ 53575508. 4-281
JJ 22105674. 4-305

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① Where two diagram sets of the same type are listed, two board versions are supported. Equipment must be checked to match diagrams to board. Refer to panel maps.

†Also in panel C.

BOOK 2

Panel A

JQ 4-329
JR 53575515. 4-351
JR 22105675. 4-363
JS† 53575516. 4-375
JS† 22130333. 4-403
JT† 4-431
HR 4-660.1

Panel B

CQ 4-447
HK/JK 4-473
JL 4-503
JM 4-527
JW†† 53575537. 4-555
JW 22105621. 4-595
KB†† 4-635
KR†† (Diagrams are located in book 3). 4-661

BOOK 3

Panels C and D

KR††† 4-661
JX 53575512. 4-695
JX 22105623. 4-725
JY 53575513. 4-755
JY 22105622. 4-783
JZ 4-841
KA 22127690. 4-871
KA 22105610. 4-877
KX 4-883
KZ 4-905
LX 4-927
LZ 4-941

APPENDIX

A PANEL MAPS A-1

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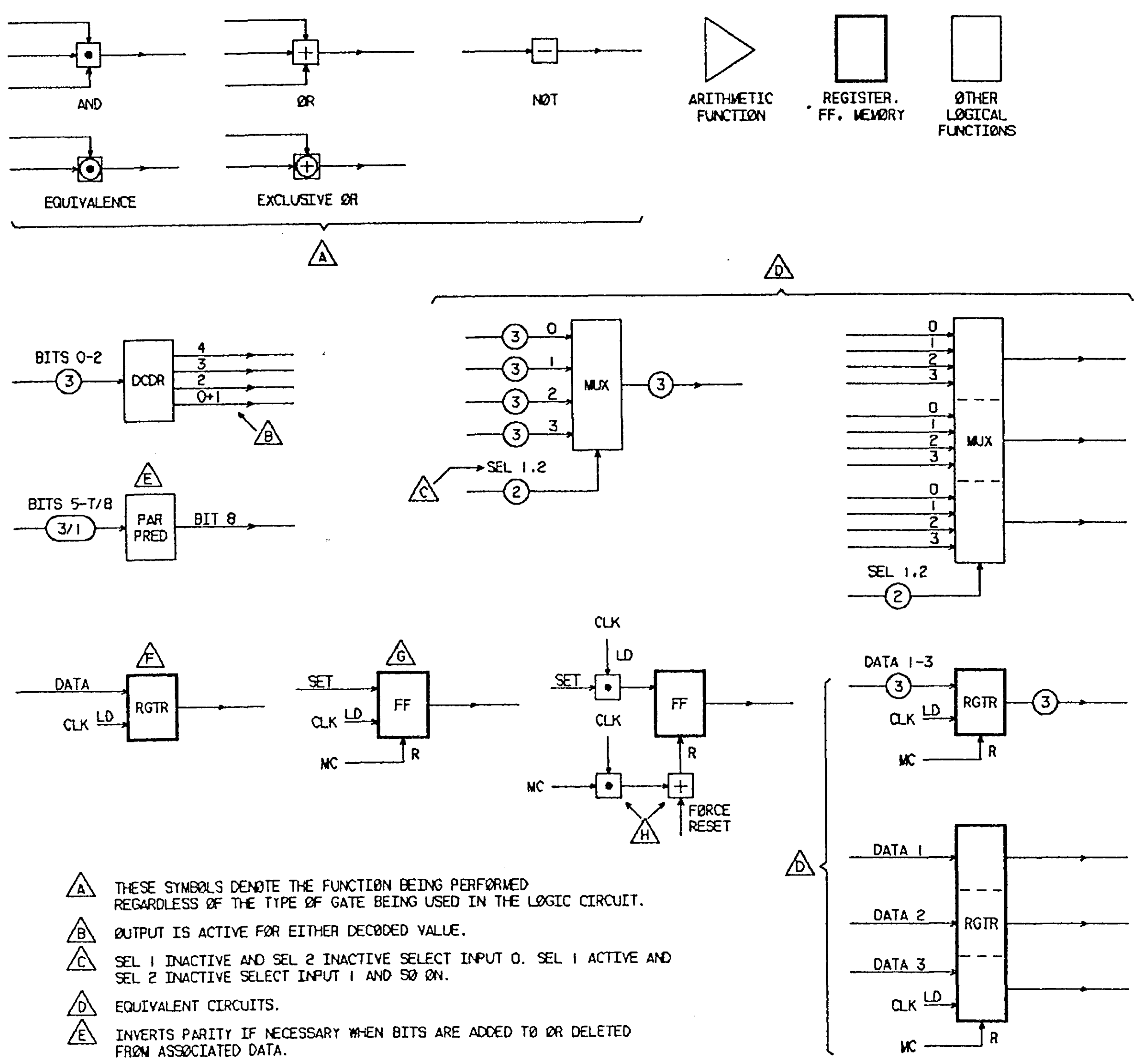
† Also in panel D.
†† Also in panels C and D.
††† Also in panel B.

The following page contains the block diagram symbols.

LOGIC SYMBOLS



A THESE SYMBOLS DENOTE THE FUNCTION BEING PERFORMED REGARDLESS OF THE TYPE OF GATE BEING USED IN THE LOGIC CIRCUIT.

B OUTPUT IS ACTIVE FOR EITHER DECODED VALUE.

C SEL 1 INACTIVE AND SEL 2 INACTIVE SELECT INPUT 0. SEL 1 ACTIVE AND SEL 2 INACTIVE SELECT INPUT 1 AND SO ON.

D EQUIVALENT CIRCUITS.

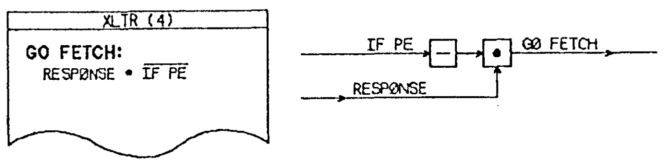
E INVERTS PARITY IF NECESSARY WHEN BITS ARE ADDED TO OR DELETED FROM ASSOCIATED DATA.

F NEW DATA ENTERS RGTR WHEN LOAD TERM IS PRESENT. RGTR MAY CONTAIN ANY NUMBER OF DATA BITS OR SIGNALS.

G AFTER FF SETS, ONLY THE ARRIVAL OF RESET WILL CLEAR IT. IN EXAMPLE SHOWN, CLOCK LOADS SET AND RESET.

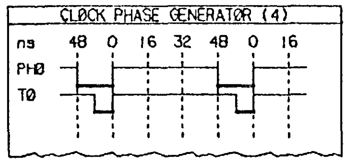
H FORCE RESET ENTERS FF DIRECTLY. CLOCK LOADS RESET.

PRESENCE OR ABSENCE OF SIGNAL



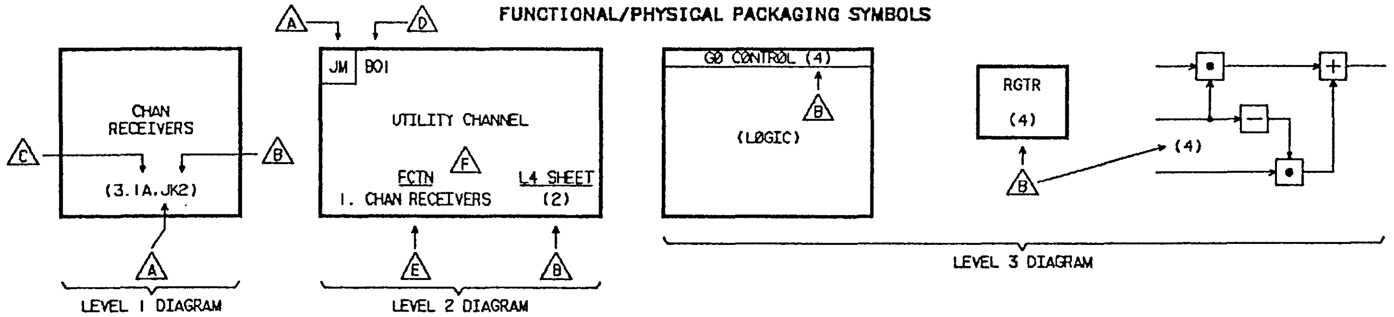
NOT BAR INDICATES SIGNAL MUST BE ABSENT TO PRODUCE OUTPUT. ABSENCE OF NOT BAR INDICATES SIGNAL MUST BE PRESENT TO PRODUCE OUTPUT.

TIMING DIAGRAM



BOLD LINE INDICATES ACTIVE PULSE. ACTUAL VOLTAGE LEVELS ARE NOT TO BE INFERRED FROM DIAGRAM.

FUNCTIONAL/PHYSICAL PACKAGING SYMBOLS



A BOARD TYPE.

B LEVEL 4 SHEET NUMBER.

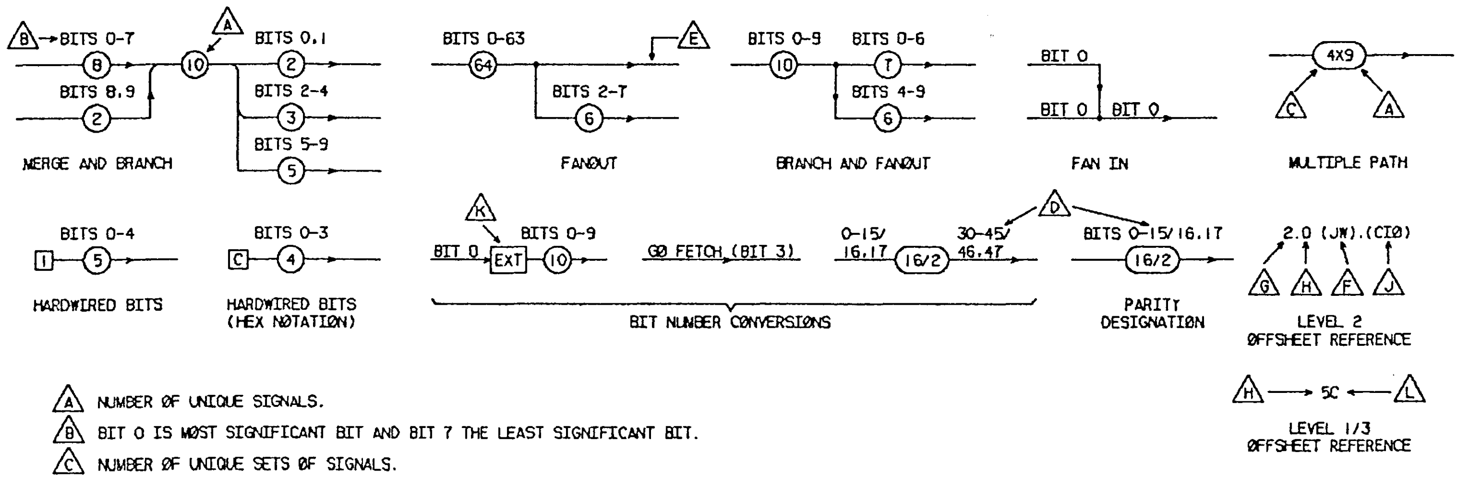
C LEVEL 3 SHEET NUMBER AND DIAGRAM BLOCK NUMBER.

D BOARD LOCATION.

E FUNCTION HEADING ON LEVEL 4.

F A SPECIFIC BOARD APPEARS ONLY ONCE IN LEVEL 2 DIAGRAMS.

SIGNAL PATHS



A NUMBER OF UNIQUE SIGNALS.

B BIT 0 IS MOST SIGNIFICANT BIT AND BIT 7 THE LEAST SIGNIFICANT BIT.

C NUMBER OF UNIQUE SETS OF SIGNALS.

D A SLASH SEPARATES THE NUMBER OF UNIQUE PARITY BITS FROM THE NUMBER OF UNIQUE DATA BITS OR SIGNALS.

E CONTINUATION OF 64-BIT PATH.

F LEVEL 2 BOARD TYPE.

G DIAGRAM LEVEL NUMBER.

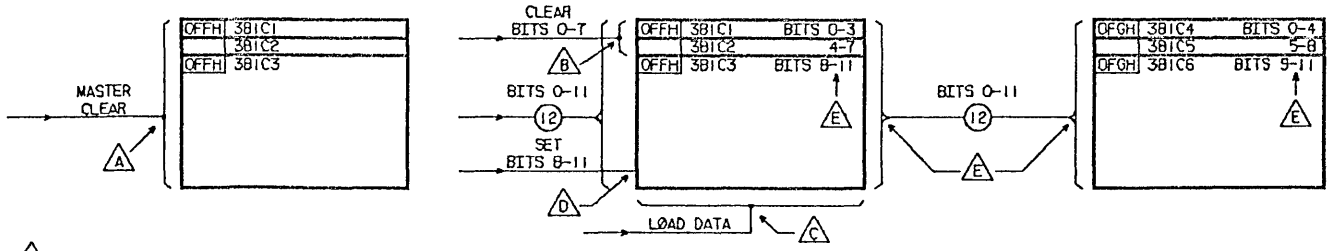
H DIAGRAM NUMBER.

J INDICATES CIO (C OR D PANEL) ORIGIN OR DESTINATION.

K EXTENDS SINGLE BIT INTO ADDITIONAL BIT POSITIONS.

L DIAGRAM BLOCK LETTER.

STACK I/O CONVENTIONS (LEVEL 2 DIAGRAMS)



A SOLDER-POINT CONNECTION TO A BRACKET INDICATES SIGNAL IS INPUT TO ALL BOARDS ADJACENT TO BRACKET.

B BRACKETS ARE NESTED WHEN CONNECTIONS TO ALL BOARDS ARE NOT IDENTICAL.

C BRACKETS ALONG TOP OR BOTTOM OF STACK ARE EQUIVALENT TO BRACKETS ADJACENT TO ALL BOARDS IN STACK.

D INPUT OR OUTPUT MAY ENTER OR LEAVE AN INDIVIDUAL BOARD WITHIN THE STACK THROUGH A BRACKET.

E INDIVIDUAL BOARDS SHOW THE DISTRIBUTION OF SIGNALS ENTERING OR LEAVING A STACK ALONG A COMMON PATH.

CONFIGURATION

The Input/Output Unit (IOU), figure 1-1, consists of a Nonconcurrent I/O (NIO) Subsystem and a Concurrent I/O (CIO) Subsystem. The NIO contains up to 20 peripheral processors (PPs) partitioned into four Barrels and Slots (BASs) of five PPs each. The four BASs (BAS 0 through 3) share access to a maximum of 24 I/O channels that support CYBER 170 peripheral equipment (channels 0 through 7, 11 through 13, 20 through 27, and 30 through 33). In addition, the NIO also has the following special I/O channels.

- Channel 10 may be connected to an optional internal Display Station Controller (DSC) that interfaces with a CC545 Display Station. If the DSC is not present, a CYBER 170 I/O channel may be installed in its place.
- Channel 14 connects to an internal Real Time Clock.
- Channel 15 connects to an internal Two-Port Mux (TPM) that initializes the IOU and provides two RS-232-C interfaces for CC634 Display Terminals or CC598 System Consoles.
- Channel 17 (the Maintenance Channel) connects to radial interfaces from which the IOU initializes the mainframe elements of the system. The I/O involved in this initialization, and in the gathering of system status, is handled by an internal Maintenance Access Control (MAC) unit.

The CIO contains up to 10 PPs partitioned into two BASs (BAS 0 and 1) of five PPs each. Each BAS in the CIO has five dedicated, direct-memory access (DMA), I/O channels (channels 0 through 4 for BAS 0; channels 5_8 through 11_8 for BAS 1). The DMA channels described in this discussion support disk storage equipment having an Intelligent Standard Interface (ISI). The DMA capability of these channels allows central memory (CM) references to be made during an I/O transfer without PP intervention. However, these transfers must be set up and initiated by a PP.

NIO UNITS

The next paragraphs briefly describe the functional units of the NIO.

CENTRAL MEMORY INTERFACE

The Central Memory Interface (CMI) exchanges CM data between the Assembly/Disassembly Units (ADUs) of the IOU and the Central Memory Control (CMC) unit of the computer system. This is done in synchronization with the CM clock. The CMI supports both 60-bit and 64-bit CM words. The CMI also exchanges CM data between the CMC and the ISI channels of the CIO during DMA transfers.

ASSEMBLY/DISASSEMBLY UNITS

Each BAS in the NIO has an associated ADU. In 170 operations, the ADU assembles five 12-bit PP words into a 60-bit CM word during a PP write and disassembles a 60-bit CM word into five 12-bit words during a PP read. In 180 operations, the ADU assembles four 16-bit PP words into a 64-bit CM word during a PP write and disassembles a 64-bit CM word into four 16-bit words during a PP read.

BARRELS AND SLOTS

Each BAS in the NIO contains the necessary circuits to execute the 170 PP instruction set and the 180 PP instruction set. The circuits in a BAS form barrels that perform specific functions. Each barrel contains five stages (ranks 0 through 4) for the holding and processing of instructions or data. A common 50-ns clock enters new or recycled information into the barrels each clock period and propagates the information through the barrels. The entering stage of a barrel is rank 0 and the slot (action) stage is rank 4. One major cycle through a barrel takes 250 ns. The five ranks of all barrels in a BAS collectively represent its five PPs.

The next paragraphs describe the barrels and PP memory (PPM) that are in a BAS.

A Barrel

The A barrel processes:

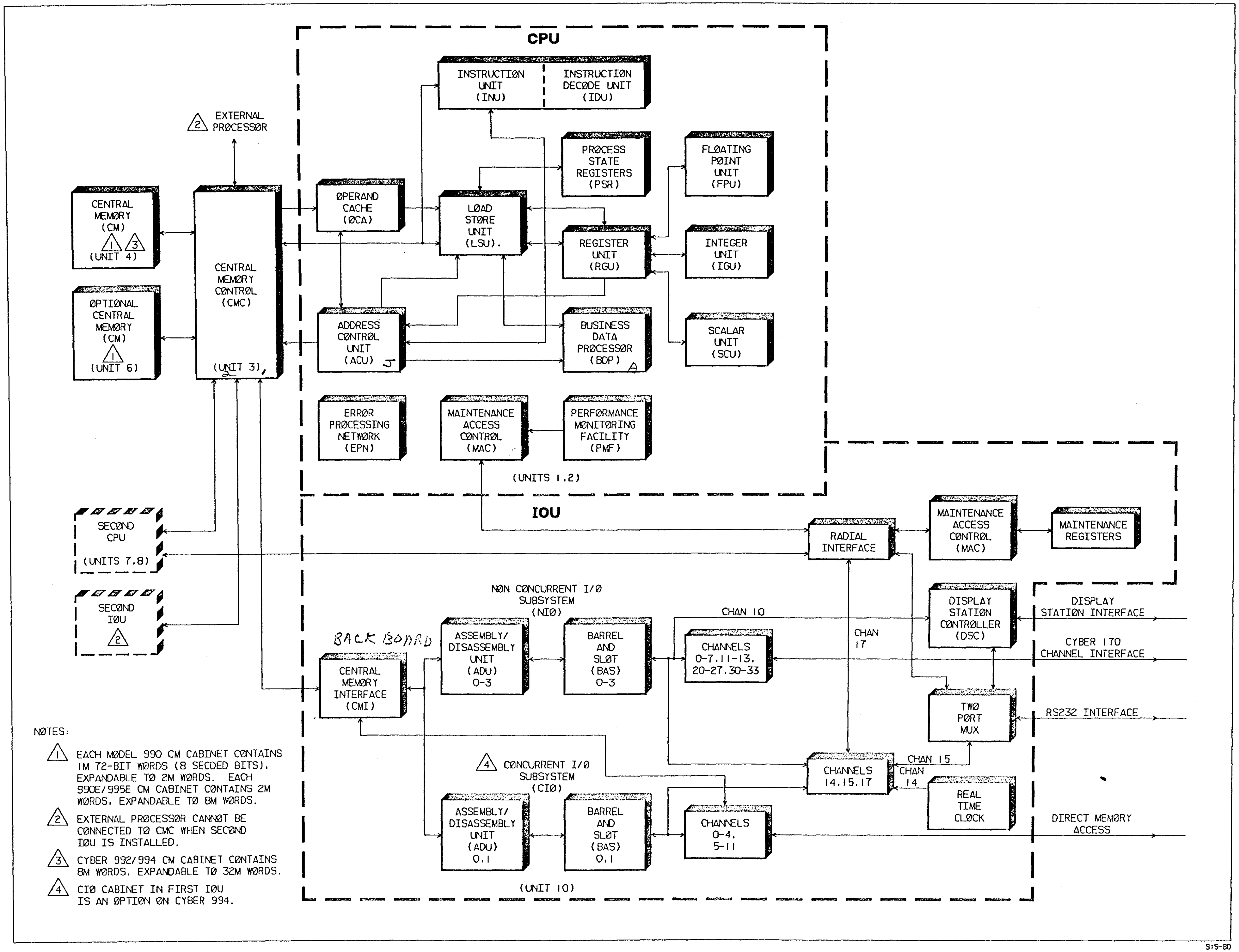
- Operands for arithmetic and logical operations
- CM addresses (part or all)
- I/O function or data words
- Word counts for block I/O operations

C Barrel

The C barrel performs word conversions for input-packed and output-packed I/O instructions. For input-packed instructions, the C barrel converts four words from an external device into three 16-bit words. For output-packed instructions, the C barrel converts three 16-bit words being output to an external device into four words.

K Barrel

The K barrel holds the instruction opcodes for the instructions in progress.


CPU
INSTRUCTION UNIT (INU)
INSTRUCTION DECODE UNIT (IDU)
2 EXTERNAL PROCESSOR
PROCESS STATE REGISTERS (PSR)
FLOATING POINT UNIT (FPU)
CENTRAL MEMORY (CM) 1 3 (UNIT 4)
OPERAND CACHE (OCA)
LOAD STORE UNIT (LSU).
REGISTER UNIT (RGU)
INTEGER UNIT (IGU)
CENTRAL MEMORY CONTROL (CMC)
OPTIONAL CENTRAL MEMORY (CM) 1 (UNIT 6)
ADDRESS CONTROL UNIT (ACU)
BUSINESS DATA PROCESSOR (BDP)
SCALAR UNIT (SCU)
(UNIT 3)
ERROR PROCESSING NETWORK (EPN)
MAINTENANCE ACCESS CONTROL (MAC)
PERFORMANCE MONITORING FACILITY (PMF)
(UNITS 1,2)
IOU
SECOND CPU (UNITS 7,8)
RADIAL INTERFACE
MAINTENANCE ACCESS CONTROL (MAC)
MAINTENANCE REGISTERS
SECOND IOU 2
NON CONCURRENT I/O SUBSYSTEM (NIO)
DISPLAY STATION CONTROLLER (DSC)
DISPLAY STATION INTERFACE
CHAN 10
CHAN 17
BACK BOARD
ASSEMBLY/ DISASSEMBLY UNIT (ADU) 0-3
BARREL AND SLOT (BAS) 0-3
CHANNELS 0-7,11-13, 20-27,30-33
CYBER 170 CHANNEL INTERFACE
CENTRAL MEMORY INTERFACE (CMI)
TWO PORT MUX
RS232 INTERFACE
4 CONCURRENT I/O SUBSYSTEM (CIO)
CHAN 15
CHANNELS 14,15,17
CHAN 14
REAL TIME CLOCK
ASSEMBLY/ DISASSEMBLY UNIT (ADU) 0,1
BARREL AND SLOT (BAS) 0,1
CHANNELS 0-4, 5-11
DIRECT MEMORY ACCESS
(UNIT 10)
STS-80

NOTES:

1. EACH MODEL 990 CM CABINET CONTAINS 1M 72-BIT WORDS (8 SECDED BITS). EXPANDABLE TO 2M WORDS. EACH 990E/995E CM CABINET CONTAINS 2M WORDS, EXPANDABLE TO 8M WORDS.
2. EXTERNAL PROCESSOR CANNOT BE CONNECTED TO CMC WHEN SECOND IOU IS INSTALLED.
3. CYBER 992/994 CM CABINET CONTAINS 8M WORDS, EXPANDABLE TO 32M WORDS.
4. CIO CABINET IN FIRST IOU IS AN OPTION ON CYBER 994.

Figure 1-1. Computer System Elements

P Barrel

The P barrel generates the program address that is to be read next in CM. For block I/O or block CM read/write instructions, the P barrel also generates the address that is to be accessed next in PPM.

Q Barrel

The Q barrel processes the:

- PPM addresses of operands for direct-address-mode, indirect-address-mode, and memory-address-mode instructions
- I/O channel numbers for I/O instructions
- PPM addresses for all jump instructions
- Word counts for block CM read/write instructions

R Barrel

The R barrel holds the starting boundary addresses for CM read/write and exchange operations.

PP Memory

The PPM in a BAS is used to store:

- PP instructions read from CM
- Operands
- Block I/O data or block CM read/write data

TWO-PORT MUX

The TPM contains two asynchronous I/O ports with RS-232-C interfaces for connecting CC634 Display Terminals or CC598 System Consoles. The TPM also contains a calender clock and is accessible to all BASs in the IOU. In addition, communication paths exist between the TPM, MAC, and DSC.

The TPM supports both local and remote deadstarts. During a system deadstart, the TPM initializes the IOU. Once the IOU is initialized, it initializes the remaining mainframe equipment in the system by accessing the storage device used to load software. During a deadstart, programs residing in read-only memory (ROM) and battery-backed random-access memory (RAM) within the TPM generate the required displays on the CC545 Display Station, CC634 Display Terminal, or CC598 System Console, and process the entries made at the console keyboard.

The operator initiating the deadstart may select either a short or long deadstart. With a short deadstart, the TPM master clears all the BASs in the IOU and loads the program displayed on the screen into the NIO BAS containing logical PP0. If a long deadstart is selected, the TPM generates a test that runs in this BAS for approximately 15 seconds before the loading of the displayed program occurs. However, if the test does not end successfully, no loading occurs and an error message is displayed instead.

MAINTENANCE ACCESS CONTROL

The MAC transfers data between the:

- IOU maintenance registers and BASs
- IOU maintenance registers and TPM
- BASs and MAC units in other mainframe elements

MAINTENANCE REGISTERS

Maintenance registers store fault status and environment information for each part of the IOU. Maintenance registers also store status summary information that indicates whether an error exists in any part of the mainframe. These registers are accessible to any BAS via the MAC.

DISPLAY STATION CONTROLLER

The optional DSC handles the I/O exchanges that occur between a CC545 Display Station and a NIO BAS or the TPM. In doing this, the DSC:

- Converts data going to the display station into video signals that control the station´s cathode-ray tube (CRT) beam.
- Converts the keyboard generated codes from the display station into American Code for Information Interchange (ASCII) codes when operations are in 180 mode.

REAL TIME CLOCK

The Real Time Clock is a free-running counter that increments every microsecond. The Real Time Clock is accessible to any BAS.

CIO UNITS

The next paragraphs briefly describe the functional units of the CIO.

ASSEMBLY/DISASSEMBLY UNITS

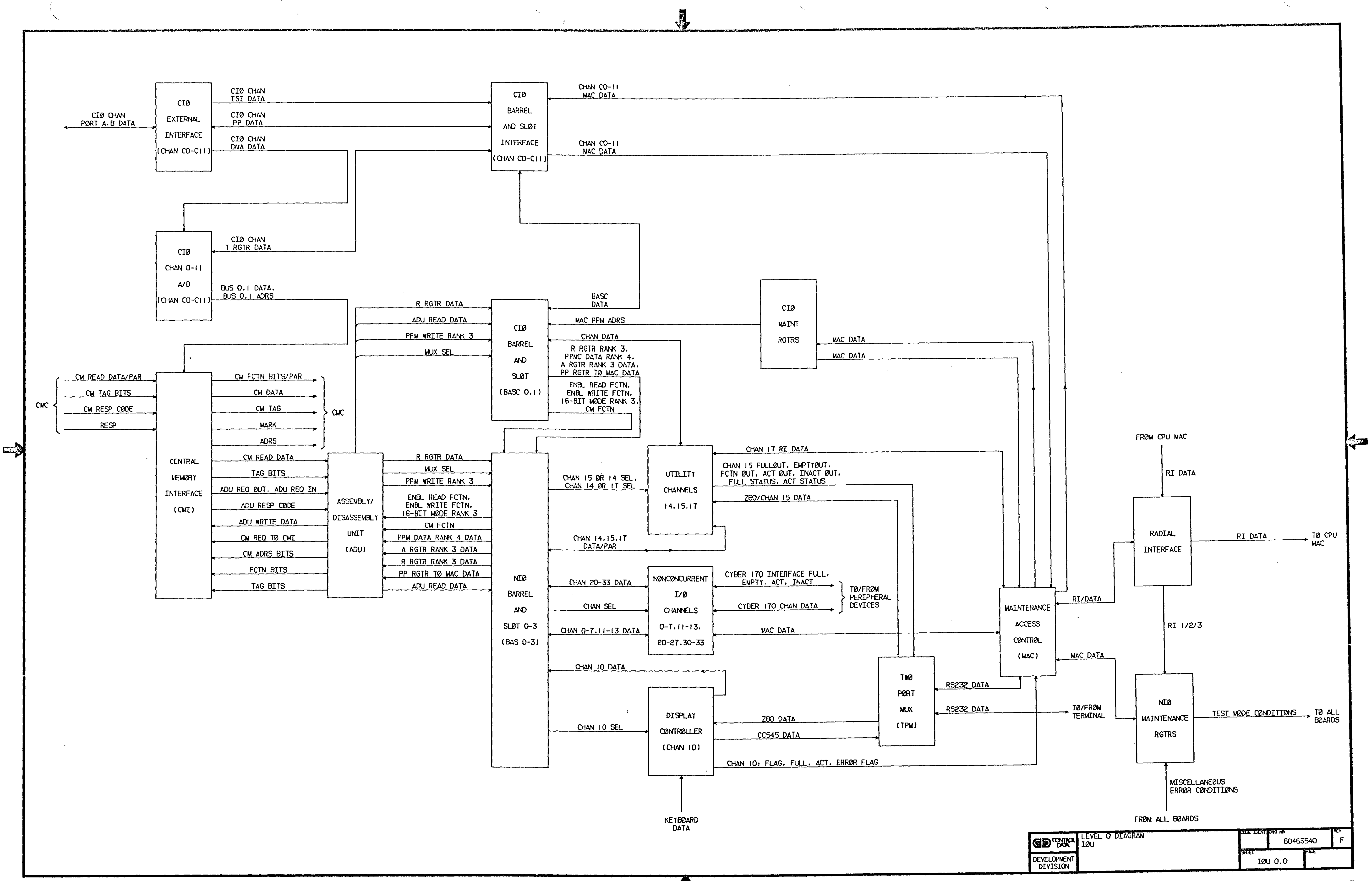
The ADUs in the CIO operate the same as their counterparts in the NIO.

BARRELS AND SLOTS and ISI CHANNEL ADAPTERS

The BASs in the CIO are identical to those in the NIO. However, each CIO BAS interacts with five ISI channel adapters for communications with external devices. Each channel adapter is assigned an I/O channel number by which it is addressed by the PPs of the associated BAS. The channel adapters are totally controlled by the PPs through the issuance of function codes. These function codes are generated using standard PP I/O instructions.

The function code from a PP may direct a channel adapter to transfer data between the PP and the ISI channel that the adapter is servicing, or the function code may direct the adapter to perform a DMA data transfer. With a DMA transfer, the PP sets up and initiates the transfer and the channel adapter independently performs the transfer between the CMI and the ISI channel. This frees the PP for other processing. The assembly/disassembly of CM words in a DMA transfer is done by the channel adapter.

Function codes also control the signal interchange that occurs between a channel adapter and the peripheral controllers connected to ISI channel. These ISI signals are described in the applicable Virtual State Hardware Reference Manual, Volume 2 (listed in the system publication index in the preface).


CIØ CHAN PORT A,B DATA
CIØ EXTERNAL INTERFACE (CHAN C0-C11)
CIØ CHAN ISI DATA
CIØ CHAN PP DATA
CIØ CHAN DMA DATA
CIØ BARREL AND SLØT INTERFACE (CHAN C0-C11)
CHAN C0-11 MAC DATA
CHAN C0-11 MAC DATA
CIØ CHAN 0-11 A/D (CHAN C0-C11)
CIØ CHAN T RGTR DATA
BUS 0,1 DATA, BUS 0,1 ADRS
BASC DATA
R RGTR DATA
ADU READ DATA
PPM WRITE RANK 3
MUX SEL
CIØ BARREL AND SLØT (BASC 0,1)
MAC PPM ADRS
CHAN DATA
R RGTR RANK 3, PPMC DATA RANK 4, A RGTR RANK 3 DATA, PP RGTR TØ MAC DATA
ENBL READ FCTN, ENBL WRITE FCTN, 16-BIT MØDE RANK 3, CM FCTN
CIØ MAINT RGTRS
MAC DATA
MAC DATA
CMC
CM READ DATA/PAR
CM TAG BITS
CM RESP CØDE
RESP
CENTRAL MEMØRY INTERFACE (CMI)
CM FCTN BITS/PAR
CM DATA
CM TAG
MARK
ADRS
CMC
CM READ DATA
TAG BITS
ADU REQ ØUT, ADU REQ IN
ADU RESP CØDE
ADU WRITE DATA
CM REQ TØ CMI
CM ADRS BITS
FCTN BITS
TAG BITS
ASSEMBLY/ DISASSEMBLY UNIT (ADU)
R RGTR DATA
MUX SEL
PPM WRITE RANK 3
ENBL READ FCTN, ENBL WRITE FCTN, 16-BIT MØDE RANK 3
CM FCTN
PPM DATA RANK 4 DATA
A RGTR RANK 3 DATA
R RGTR RANK 3 DATA
PP RGTR TØ MAC DATA
ADU READ DATA
NIØ BARREL AND SLØT 0-3 (BAS 0-3)
CHAN 15 ØR 14 SEL, CHAN 14 ØR 17 SEL
UTILITY CHANNELS 14,15,17
CHAN 17 RI DATA
CHAN 15 FULLØUT, EMPTYØUT, FCTN ØUT, ACT ØUT, INACT ØUT, FULL STATUS, ACT STATUS
Z80/CHAN 15 DATA
CHAN 14,15,17 DATA/PAR
CHAN 20-33 DATA
CHAN SEL
CHAN 0-7,11-13 DATA
NØNCØNCURRENT I/Ø CHANNELS 0-7,11-13, 20-27,30-33
CYBER 170 INTERFACE FULL, EMPTY, ACT, INACT
CYBER 170 CHAN DATA
TØ/FRØM PERIPHERAL DEVICES
MAC DATA
CHAN 10 DATA
CHAN 10 SEL
DISPLAY CØNTRØLLER (CHAN 10)
Z80 DATA
CC545 DATA
CHAN 10: FLAG, FULL, ACT, ERRØR FLAG
KEYBØARD DATA
TWØ PØRT MUX (TPM)
RS232 DATA
RS232 DATA
TØ/FRØM TERMINAL
MAINTENANCE ACCESS CØNTRØL (MAC)
RI/DATA
MAC DATA
FRØM CPU MAC
RI DATA
RADIAL INTERFACE
RI DATA
TØ CPU MAC
RI 1/2/3
NIØ MAINTENANCE RGTRS
TEST MØDE CØNDITIØNS
TØ ALL BØARDS
MISCELLANEØUS ERRØR CØNDITIØNS
FRØM ALL BØARDS
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 0 DIAGRAM IØU
60463540
F
IØU 0.0

The logic circuits shown on this diagram are located on the ADU read (JF) board, the CMI control (JG) board, and the CMI data (JH) board.

CMI READ DATA

The CMI receives CM data from the CMC in the form of 64-bit words plus 8 parity bits. In addition, for each 64-bit word received, the CMI receives returned tag bits from the CMC (1.1). These tag bits identify the type of CM request that was made and the requesting unit. The decoding of this information is handled by the Tag Bits In F/O circuits (1.1) and the CMI Input Buffer Address Decoder and F/O circuits. The bits generated by the CMI Input Buffer Address Decoder and F/O circuits select the appropriate path through the IOU for the data from CM.

PP READ DATA PATH

The path for CM data going to one of the PPs is through the ADU CT Macro Cell Input Data and ADU Data Out circuits of the JH board and into the Data In Buffer of the JF board. From there, the 64-bit data word goes to the ADU associated with the BAS indicated in the returned tag bits.

The Disassembly Register of an ADU consists of memory circuits that hold up to ten 64-bit words. This allows two CM words (identified as odd and even) to be held per PP while disassembly is occurring.

The loading of one of these locations in the Disassembly Register results in an odd/even flag being set and a Data Ready signal being sent to the associated BAS. The BAS then sends three microcode bits that control the disassembly of the word.

The 16-bit PP words formed by the disassembly process propagate through the Rank 1 and Rank 2 Data Out Registers where they are aligned with an IOU internal 50-nanosecond clock. The transfer of CM read/write data between the CMI and CMC occurs in line with an external 64-nanosecond clock. From the Rank 2 Data Out Register, the 16-bit words go to the Y Mux of the associated BAS (1.8 for NIO; 1.26 for CIO).

ISI CHANNEL READ DATA PATH

The path for CM data going to the ISI channels in the CIO is through the Bus 0 or Bus 1 circuits of the JH board. The Bus 0 path applies to data destined for ISI Channels 0 through 4. The Bus 1 path applies to data destined for ISI Channels 5_8 through 11_8. From the Bus 0 or Bus 1 circuits, the CM data goes directly to the CIO for disassembly (1.22).

The ISI channel that requested the read data is indicated in the tag bits returned from the CMC.

CMI WRITE DATA

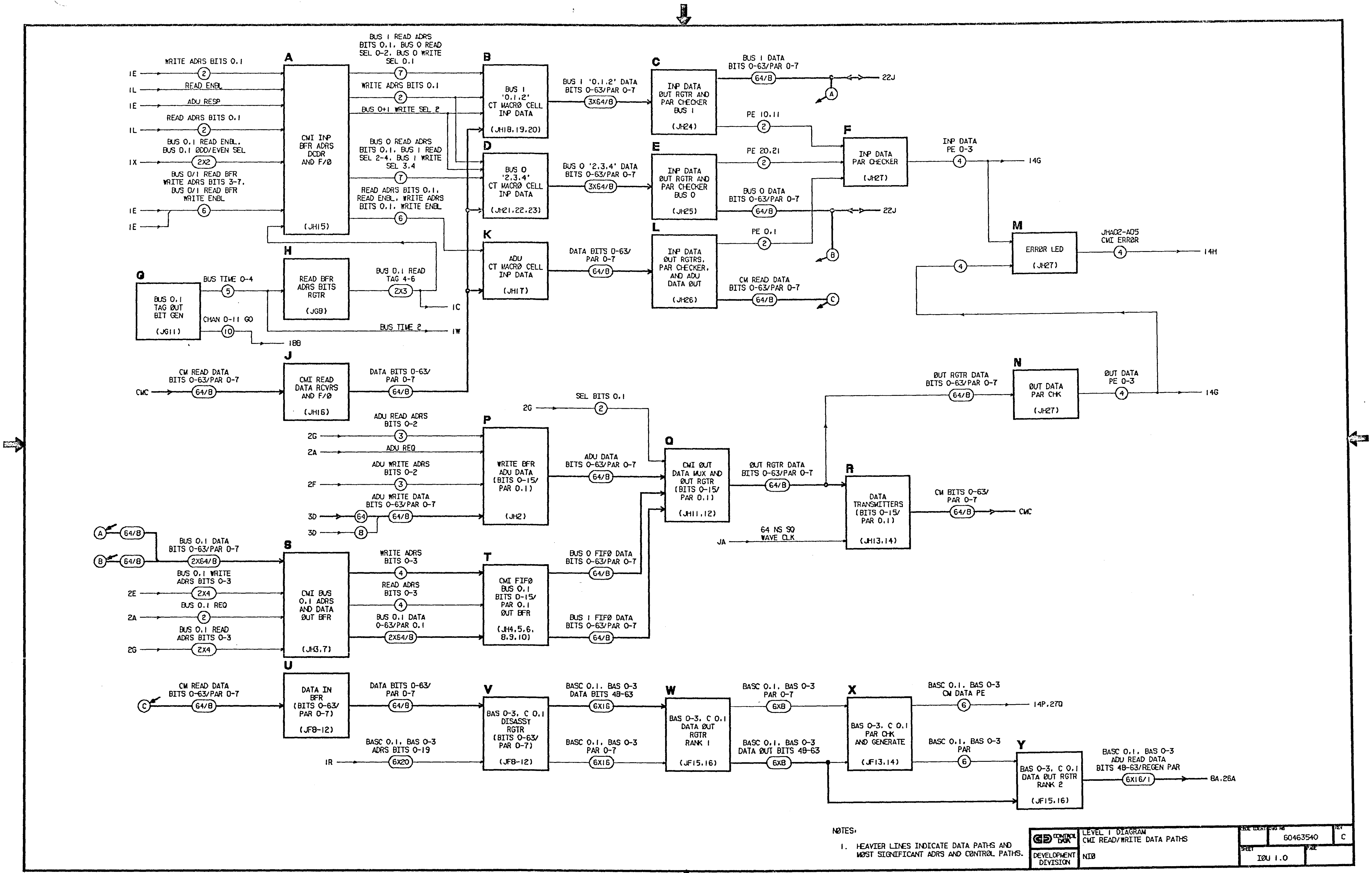
Data to be written into CM enters the CMI in the form of 64-bit words with 8 parity bits. When the CMI transmits a word to the CMC, the CMI also transmits CM Tag Bits 0 through 7 (1.2) that indicate the type of write request being made and the requesting unit.

PP WRITE DATA PATH

PP data to be written into CM comes from the requesting ADU that has assembled the word. This data enters the CMI through the ADU Data Write Buffer, which has eight locations for word storage. From there, the data goes through the CMI Out Data Mux and Out Register and into the Data Transmitters. The Data Transmitters pass the data to the CMC in synchronization with the external 64-nanosecond clock.

ISI CHANNEL WRITE DATA PATH

Data to be written into CM from an ISI channel propagates through the CMI Bus 0/1 Address and Data Out Buffer and enters the CMI FIFO Bus 0/1 Out Buffer. This latter buffer provides both Bus 0 and Bus 1 with 16 words of storage. From the CMI FIFO Bus 0/1 Out Buffer, the data goes through the CMI Out Data Mux and Out Register and into the Data Transmitters.


A
CMI INP BFR ADRS DCDR AND F/Ø (JH15)
1E WRITE ADRS BITS 0.1 ②
1L READ ENBL
1E ADU RESP
1L READ ADRS BITS 0.1 ②
1X BUS 0.1 READ ENBL. BUS 0.1 ØDD/EVEN SEL 2X2
1E 1E BUS 0/1 READ BFR WRITE ADRS BITS 3-7. BUS 0/1 READ BFR WRITE ENBL ⑥
BUS 1 READ ADRS BITS 0.1. BUS 0 READ SEL 0-2. BUS 0 WRITE SEL 0.1 ⑦
WRITE ADRS BITS 0.1 ②
BUS 0+1 WRITE SEL 2
BUS 0 READ ADRS BITS 0.1. BUS 1 READ SEL 2-4. BUS 1 WRITE SEL 3.4 ⑦
READ ADRS BITS 0.1. READ ENBL. WRITE ADRS BITS 0.1. WRITE ENBL ⑥
B
BUS 1 '0.1.2' CT MACRØ CELL INP DATA (JH18.19.20)
BUS 1 '0.1.2' DATA BITS 0-63/PAR 0-7 3X64/8
C
INP DATA ØUT RGTR AND PAR CHECKER BUS 1 (JH24)
BUS 1 DATA BITS 0-63/PAR 0-7 64/8
22J
A
PE 10.11 ②
D
BUS 0 '2.3.4' CT MACRØ CELL INP DATA (JH21.22.23)
BUS 0 '2.3.4' DATA BITS 0-63/PAR 0-7 3X64/8
E
INP DATA ØUT RGTR AND PAR CHECKER BUS 0 (JH25)
PE 20.21 ②
BUS 0 DATA BITS 0-63/PAR 0-7 64/8
22J
F
INP DATA PAR CHECKER (JH27)
INP DATA PE 0-3 ④
14G
K
ADU CT MACRØ CELL INP DATA (JH17)
DATA BITS 0-63/ PAR 0-7 64/8
L
INP DATA ØUT RGTRS. PAR CHECKER. AND ADU DATA ØUT (JH26)
PE 0.1 ②
B
CM READ DATA BITS 0-63/PAR 0-7 64/8
C
M
ERRØR LED (JH27)
JHA02-A05 CMI ERRØR ④
14H
④
G
BUS 0.1 TAG ØUT BIT GEN (JG11)
BUS TIME 0-4 ⑤
CHAN 0-11 GO ⑩
18B
H
READ BFR ADRS BITS RGTR (JG8)
BUS 0.1 READ TAG 4-6 2X3
1C
BUS TIME 2
1W
J
CMI READ DATA RCVRS AND F/Ø (JH16)
CMC CM READ DATA BITS 0-63/PAR 0-7 64/8
DATA BITS 0-63/ PAR 0-7 64/8
N
ØUT DATA PAR CHK (JH27)
ØUT RGTR DATA BITS 0-63/PAR 0-7 64/8
ØUT DATA PE 0-3 ④
14G
P
WRITE BFR ADU DATA (BITS 0-15/ PAR 0.1) (JH2)
2G ADU READ ADRS BITS 0-2 ③
2A ADU REQ
2F ADU WRITE ADRS BITS 0-2 ③
3D 64 ADU WRITE DATA BITS 0-63/PAR 0-7 64/8
3D 8
2G SEL BITS 0.1 ②
ADU DATA BITS 0-63/PAR 0-7 64/8
Q
CMI ØUT DATA MUX AND ØUT RGTR (BITS 0-15/ PAR 0.1) (JH11.12)
ØUT RGTR DATA BITS 0-63/PAR 0-7 64/8
R
DATA TRANSMITTERS (BITS 0-15/ PAR 0.1) (JH13.14)
JA 64 NS SQ WAVE CLK
CM BITS 0-63/ PAR 0-7 64/8
CMC
A 64/8
B 64/8
S
CMI BUS 0.1 ADRS AND DATA ØUT BFR (JH3.7)
BUS 0.1 DATA BITS 0-63/PAR 0-7 2X64/8
2E BUS 0.1 WRITE ADRS BITS 0-3 2X4
2A BUS 0.1 REQ ②
2G BUS 0.1 READ ADRS BITS 0-3 2X4
WRITE ADRS BITS 0-3 ④
READ ADRS BITS 0-3 ④
BUS 0.1 DATA 0-63/PAR 0.1 2X64/8
T
CMI FIFØ BUS 0.1 BITS 0-15/ PAR 0.1 ØUT BFR (JH4.5.6. 8.9.10)
BUS 0 FIFØ DATA BITS 0-63/PAR 0-7 64/8
BUS 1 FIFØ DATA BITS 0-63/PAR 0-7 64/8
U
DATA IN BFR (BITS 0-63/ PAR 0-7) (JF8-12)
C CM READ DATA BITS 0-63/PAR 0-7 64/8
DATA BITS 0-63/ PAR 0-7 64/8
1R BASC 0.1. BAS 0-3 ADRS BITS 0-19 6X20
V
BAS 0-3. C 0.1 DISASSY RGTR (BITS 0-63/ PAR 0-7) (JF8-12)
BASC 0.1. BAS 0-3 DATA BITS 48-63 6X16
BASC 0.1. BAS 0-3 PAR 0-7 6X16
W
BAS 0-3. C 0.1 DATA ØUT RGTR RANK 1 (JF15.16)
BASC 0.1. BAS 0-3 PAR 0-7 6X8
BASC 0.1. BAS 0-3 DATA ØUT BITS 48-63 6X8
X
BAS 0-3. C 0.1 PAR CHK AND GENERATE (JF13.14)
BASC 0.1. BAS 0-3 CM DATA PE ⑥
14P.27D
BASC 0.1. BAS 0-3 PAR ⑥
Y
BAS 0-3. C 0.1 DATA ØUT RGTR RANK 2 (JF15.16)
BASC 0.1. BAS 0-3 ADU READ DATA BITS 48-63/REGEN PAR 6X16/1
8A.26A

NØTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM CMI READ/WRITE DATA PATHS	60463540	C
DEVELOPMENT DIVISION	NIØ	IØU 1.0	

CM RESPONSE AND CM TAG (NIO) (IOU 1.1)

The logic circuits shown on this diagram are located on the ADU control (JD) board, the ADU read (JF) board, the CMI control (JG) board, and the CMI address (JJ) board.

The returned tag bits for an ADU request also go through the 8-bit to 9-bit conversion listed in table 1-1.

TAG IN CIRCUITS

The circuits shown at the upper left of the diagram latch the returned tag bits and distribute them for decoding to determine which unit will receive the CMC response. When the CMC sends a response code for a request, it returns the tag bits that accompanied the request and generates the CMC Response signal. Several copies of tag bits are then decoded in parallel to determine whether the response is for an ADU serving a BAS or an ISI channel of the CIO (Bus 0 of 1). Further decoding then occurs to determine the exact unit, whether the response is for CM read data and whether the read data, is for the odd or even portion of a Disassembly Register.

CM RESPONSE CIRCUITS

The Response Code Deskew and ADU Input Buffer circuits align the CMC response bits with the internal 50-nanosecond clock of the IOU and store the response bits if they are for an ADU request. If the response bits are for a Bus 0 or 1 request, the bits are stored in the Bus 0/1 Response Code Memory. The response bits remain stored until the response is synchronized with the operation of the requesting unit.

The response bits are then decoded to determine whether they represent an incorrect response (decoding for Bus 0 or 1 is done by the CM Response Code Translator on 1.18). If the response is incorrect, it is reported in fault status (1.14).

DATA READY CIRCUITS

The data ready circuits set a Data Ready Rank 4 signal at slot time when the associated BAS is to receive CM read data. This indicates that part of the disassembled CM word requested is ready for transfer into PPM.

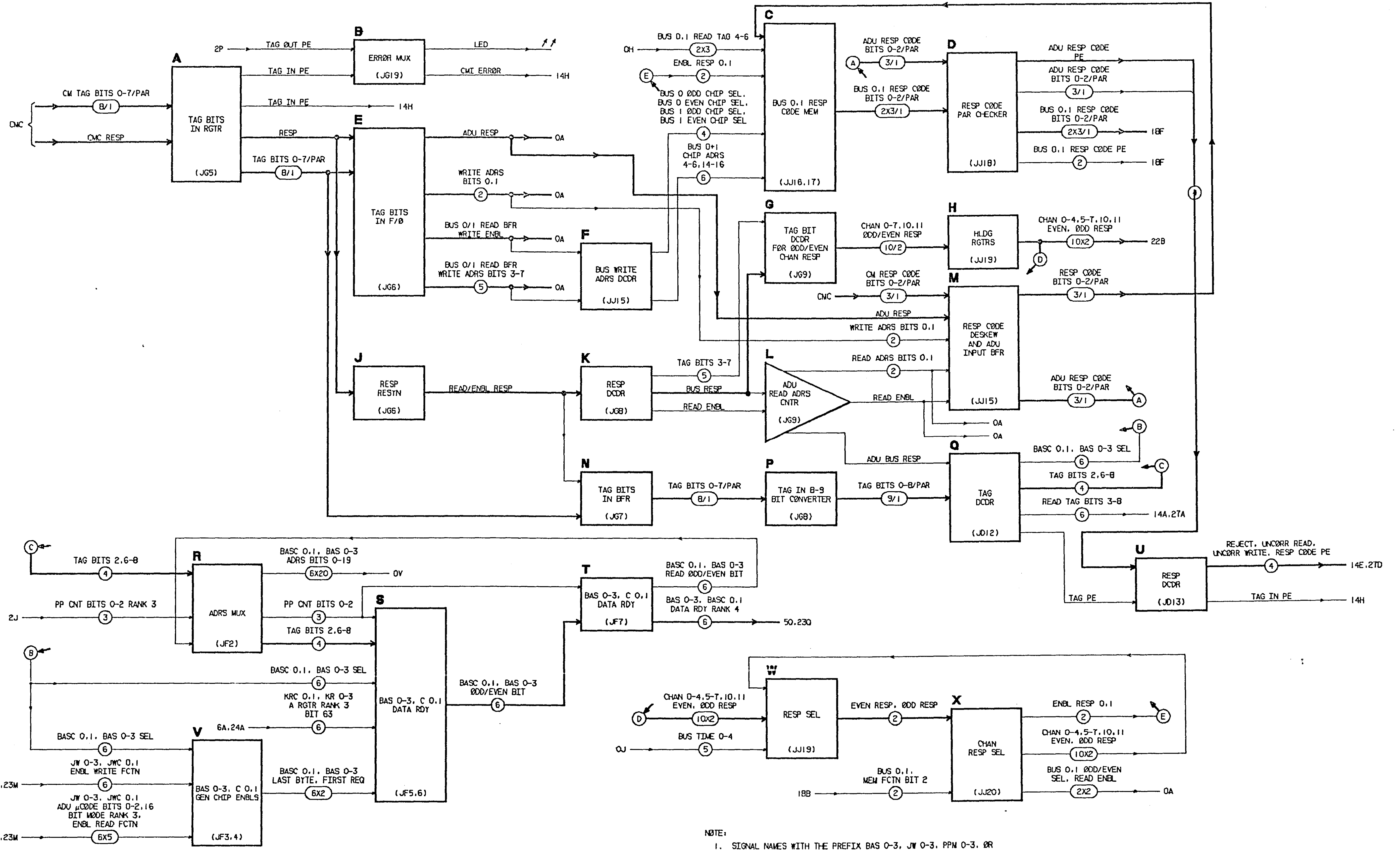
ADDRESS MUX

This ADU multiplexer provides write and read addresses to the associated Disassembly Register (1.0). The state of returned tag bit 2 determines whether the odd or even portion of the Disassembly Register is addressed. During the write of a CM word into the Disassembly Register, the address gated by this multiplexer is based on Tag In Bits 6 through 8 and Tag In Bit 2. During the disassembly of the CM word, the address gated is based on PP Count Bits 0 through 2 (PP in the slot) and Tag In Bit 2.

Table 1-1. 8-Bit to 9-Bit Tag Conversion

BAS†	PP	8-Bit Tag Bits 3 though 7 (Octal)	9-Bit Tag Bits 3 through 8 (Octal)
0	0	0	0
0	1	1	1
0	2	2	2
0	3	3	3
0	4	4	4
1	0	10	10
1	1	11	11
1	2	12	12
1	3	13	13
1	4	14	14
2	0	20	20
2	1	21	21
2	2	22	22
2	3	23	23
2	4	24	24
3	0	30	30
3	1	31	31
3	2	32	32
3	3	33	33
3	4	34	34
4	0	7	40
4	1	6	41
4	2	27	42
4	3	26	43
4	4	5	44
5	0	17	50
5	1	16	51
5	2	37	52
5	3	36	53
5	4	15	54

†Numbers 0 through 5 are the logical BAS numbers for an IOU having 20 PPs in the NIO and 10 PPs in the CIO.


A
TAG BITS IN RGTR (JG5)
CMC
CM TAG BITS 0-7/PAR
8/1
CMC RESP
2P
TAG ØUT PE
B
ERRØR MUX (JG19)
LED
TAG IN PE
CMI ERRØR
14H
TAG IN PE
14H
RESP
TAG BITS 0-7/PAR
8/1
E
TAG BITS IN F/Ø (JG6)
ADU RESP
0A
WRITE ADRS BITS 0.1
2
0A
BUS 0/1 READ BFR WRITE ENBL
0A
BUS 0/1 READ BFR WRITE ADRS BITS 3-7
5
0A
F
BUS WRITE ADRS DCDR (JJ15)
C
BUS 0.1 RESP CØDE MEM (JJ16.17)
0H
BUS 0.1 READ TAG 4-6
2X3
E
ENBL RESP 0.1
2
BUS 0 ØDD CHIP SEL. BUS 0 EVEN CHIP SEL. BUS 1 ØDD CHIP SEL. BUS 1 EVEN CHIP SEL
4
BUS 0+1 CHIP ADRS 4-6.14-16
6
A
ADU RESP CØDE BITS 0-2/PAR
3/1
BUS 0.1 RESP CØDE BITS 0-2/PAR
2X3/1
D
RESP CØDE PAR CHECKER (JJ18)
ADU RESP CØDE PE
ADU RESP CØDE BITS 0-2/PAR
3/1
BUS 0.1 RESP CØDE BITS 0-2/PAR
2X3/1
18F
BUS 0.1 RESP CØDE PE
2
18F
G
TAG BIT DCDR FØR ØDD/EVEN CHAN RESP (JG9)
CHAN 0-7.10.11 ØDD/EVEN RESP
10/2
H
HLDG RGTRS (JJ19)
CHAN 0-4.5-7.10.11 EVEN. ØDD RESP
10X2
22B
D
M
RESP CØDE DESKEW AND ADU INPUT BFR (JJ15)
CM RESP CØDE BITS 0-2/PAR
3/1
CMC
ADU RESP
WRITE ADRS BITS 0.1
2
READ ADRS BITS 0.1
2
RESP CØDE BITS 0-2/PAR
3/1
ADU RESP CØDE BITS 0-2/PAR
3/1
A
J
RESP RESYN (JG6)
READ/ENBL RESP
K
RESP DCDR (JG8)
TAG BITS 3-7
5
BUS RESP
READ ENBL
L
ADU READ ADRS CNTR (JG9)
READ ENBL
0A
0A
B
C
ADU BUS RESP
Q
TAG DCDR (JD12)
BASC 0.1. BAS 0-3 SEL
6
TAG BITS 2.6-8
4
READ TAG BITS 3-8
6
14A.27A
N
TAG BITS IN BFR (JG7)
TAG BITS 0-7/PAR
8/1
P
TAG IN 8-9 BIT CØNVERTER (JG8)
TAG BITS 0-8/PAR
9/1
U
RESP DCDR (JD13)
REJECT. UNCØRR READ. UNCØRR WRITE. RESP CØDE PE
4
14E.27D
TAG PE
TAG IN PE
14H
C
TAG BITS 2.6-8
4
R
ADRS MUX (JF2)
2J
PP CNT BITS 0-2 RANK 3
3
BASC 0.1. BAS 0-3 ADRS BITS 0-19
6X20
0V
PP CNT BITS 0-2
3
TAG BITS 2.6-8
4
S
BAS 0-3. C 0.1 DATA RDY (JF5.6)
T
BAS 0-3. C 0.1 DATA RDY (JF7)
BASC 0.1. BAS 0-3 READ ØDD/EVEN BIT
6
BAS 0-3. BASC 0.1 DATA RDY RANK 4
6
50.23Q
B
BASC 0.1. BAS 0-3 SEL
6
KRC 0.1. KR 0-3 A RGTR RANK 3 BIT 63
6
6A.24A
BASC 0.1. BAS 0-3 ØDD/EVEN BIT
6
BASC 0.1. BAS 0-3 SEL
6
V
BAS 0-3. C 0.1 GEN CHIP ENBLS (JF3.4)
JW 0-3. JWC 0.1 ENBL WRITE FCTN
6
5N.23M
JW 0-3. JWC 0.1 ADU μCØDE BITS 0-2.16 BIT MØDE RANK 3. ENBL READ FCTN
6X5
5N.23M
BASC 0.1. BAS 0-3 LAST BYTE. FIRST REQ
6X2
W
RESP SEL (JJ19)
D
CHAN 0-4.5-7.10.11 EVEN. ØDD RESP
10X2
0J
BUS TIME 0-4
5
EVEN RESP. ØDD RESP
2
X
CHAN RESP SEL (JJ20)
18B
BUS 0.1. MEM FCTN BIT 2
2
ENBL RESP 0.1
2
E
CHAN 0-4.5-7.10.11 EVEN. ØDD RESP
10X2
BUS 0.1 ØDD/EVEN SEL. READ ENBL
2X2
0A

NØTE:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, ØR KR 0-3 HAVE ØRIGINS ØR DESTINATIØNS IN THE NIØ (A & B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0.1. JWC 0.1. PPMC 0.1 ØR KRC 0.1 HAVE ØRIGINS ØR DESTINATIØNS IN THE CIØ (C & D PANELS).
2. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM CM RESPØNSE AND CM TAG	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	NIØ	SHEET IØU 1.1	PAGE	

This diagram shows the CMI control (JG) board and ADU control (JD) board circuits.

REQUEST CONTROL AND RESYNC

The CMI circuits at the top of this diagram control the CM requests from the units within the IOU and resynchronize the requests to conform with CMC timing. These requests come from the ADUs that serve the BASs and from Bus 0 and Bus 1 that carry the DMA transfers for the ISI channels of the CIO. These internal requests are made independently and may occur simultaneously. However, a maximum of only one CM Request can be sent to the CMC each external clock period. To compensate for this, the internal requests are honored on a priority basis.

ADU requests have priority every other internal clock period, and Bus 0 and Bus 1 requests share the alternate internal clock period. If no ADU requests are present, priority alternates between Bus 0 and Bus 1 requests.

Once a request is honored, a pair of bits (Bits 0 and 1) are written into the Request Resync Buffer. These bits identify whether the request is an ADU, a Bus 0, or a Bus 1 request. If the CMC is not busy, these bits are read from the Request Resync Buffer at the next external clock period. These bits are then distributed to select the tag information, CM address, and function code from the unit that made the request. In addition, the bits read from the Request Resync Buffer cause the appropriate Address Counter for Data Output Buffers to decrement and select the data from the unit that made the request. This selection occurs at the CMI Output Data Mux and Output Register (1.0). The tag information sent is selected by the Tag Bits Output Mux and Transmitters. The CM address and function code sent are selected by the CMI Data Mux and Output Register (1.4).

Instead, if the CMC is busy at the next external clock period, the pair of bits in the Request Resync Buffer for the honored request are kept from being read until an external clock period occurs and the CMC is not busy. The bits for four requests may be held in this manner with the first entered being the first read.

PP COUNTER

This counter on the ADU control board outputs bits that:

- Merge with returned tag bits 6 through 8 and are decoded to determine whether data required for a branch has been received.
- Form the address for writing PP data into the Assembly Registers.
- Are used by the PP Priority circuits to determine which PP of a BAS has filled the associated Assembly Register.
- Form tag bits 6 through 8, which identify the requesting PP.

BAS/PP PRIORITY

The BAS Priority Register determines which BAS in the IOU has priority for accessing CM. The need for BAS access to CM occurs when one of the PPs of a BAS has filled an Assembly Register for a CM write. When this occurs, the PP Priority circuits indicate the condition to the BAS Priority Register. If the condition applies only to one BAS, that BAS is selected by default and its associated ADU generates an ADU request to the CMC Request Control. If the condition applies to more than one BAS, the BAS with the highest priority is selected. The order of priority in effect immediately after an ADU master clear is listed below. After that, the order rotates.

- NIO BAS 0 (highest priority)
- NIO BAS 1
- NIO BAS 2
- NIO BAS 3
- CIO BAS 0
- CIO BAS 1 (lowest priority)

REQUEST COUNTER

The Request Counter keeps track of the outstanding ADU requests. If five outstanding ADU requests are present, the counter generates the CMI Busy signal until one ADU request is processed. While CMI Busy is active, further ADU requests are blocked.

TAG OUT BITS

The Tag Bits Out Mux and Transmitters send the tag bits to the CMC during each CM request made by the IOU. For Bus 0 or Bus 1 requests, tag bits 3 through 6 are generated by the Bus 0 and 1 Tag Out Bits Generator on the CMI control board. Tag bits 0 and 7 for Bus 0 and Bus 1 tags reflect the cache invalidate signal and the least significant CM address bit from the channels. Bits 1 and 2 for Bus 0 and Bus 1 tags are constant ones. Table 1-2 defines the coding of bits 3 through 7 of the Bus 0 and 1 tags. Table 1-3 defines the coding of bits 0 through 2, which applies to all IOU tags.

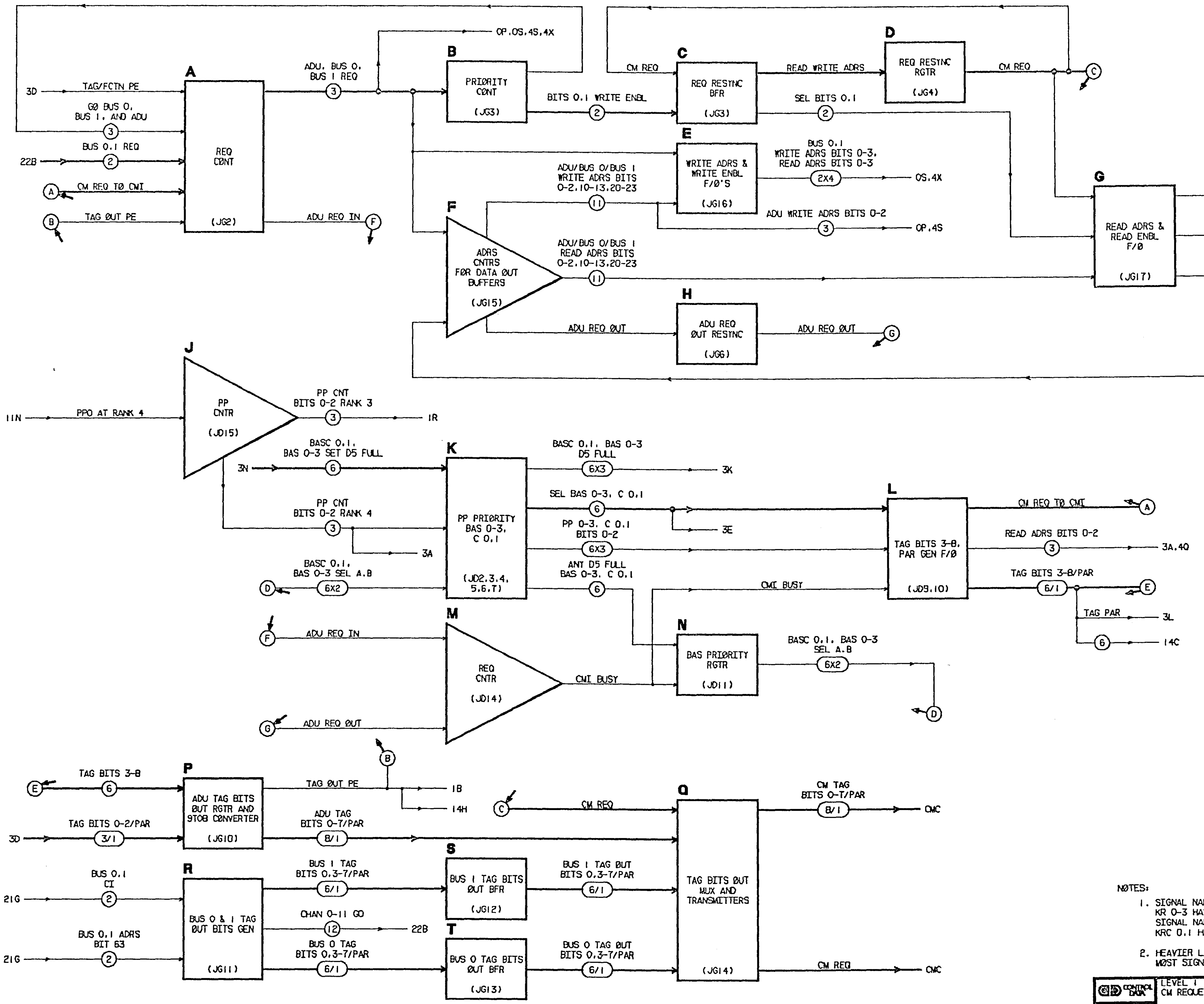
For ADU requests, tag bits 3 through 8 are generated by the Tag Bits 3 through 8 Generator and Fan Out circuit on the ADU control board. Tag bits 0 through 2 for ADU requests are generated by the BAS CP Function Bits circuit (1.3) on the ADU write board. The ADU Tag Bits Out Register and 9-to-8 Converter circuit on the CMI control board convert the nine ADU tag bits to eight bits. This conversion is the opposite of the 8-bit to 9-bit conversion described for diagram 1.1.

Table 1-2. Bus 0/1 Tag Bits 3 Through 7

Octal Value	Bus	ISI Channel
0	1	0
1	1	1
2	1	2
3	1	3
4	1	4
5	0	0
6	0	1
7	0	2
10	0	3
11	0	4

Table 1-3. Tag Bits 0 Through 2

Binary Code	Type of Request	Basic Memory Operation
000	ADU even request	-
001	ADU odd request	-
010	ADU even request	-
011	DMA channel request	-
100	ADU exchange 2600	Read
100	ADU cache invalidate	Write
101	ADU exchange 2601	Read
101	ADU cache invalidate	Write
110	ADU exchange 2602	Read
110	ADU cache invalidate	Write
111	DMA request	Read
111	DMA cache invalidate	Write



NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A & B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0.1, JWC 0.1, PPMC 0.1 OR KRC 0.1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C & D PANELS).

2. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM
CM REQUEST AND TAG OUT BITS
NIO
CODE IDENT DWG NO 60463540
REV C
SHEET IOU 1.2
PAGE

This diagram shows circuits of the ADU control (JD) board and the ADU write (JE) board that serve the BASs of the NIO and CIO.

ADU WRITE DATA TO CM

Data to be written into CM is assembled into 64-bit words in the Bits 0 through 63 Assembly Register. One of these registers exist for each BAS. These registers consist of memory chips that hold PP data until a CM word is formed. In 170 operations, a CM word is formed by combining five 12-bit PP words with four zeros. In 180 operations, a CM word is formed by combining four 16-bit PP words. All five PPs of a BAS may be assembling CM words during their slots.

The internal address used to write PP data into the Bits 0 through 63 Assembly Register originates from the PP Counter (1.2). After a CM word has been assembled and the respective BAS is selected, the internal address used to read the assembled CM word originates from the PP Counter (1.2). This address is the number of the PP (0 through 4) that finished assembly first.

ADU TAG AND FUNCTION CODE OUTPUT

The Function and Tag Assembly Register operates similarly to the Bits 0 through 63 Assembly Register. The Function and Tag Assembly Register holds Function Bits 0 through 3, Tag Bits 0 through 2, and Data Parity Bits 0 through 4 for an assembled word in the Bits 0 through 63 Assembly Register. The coding of Tag Bits 0 through 2 is defined in the discussion of diagram 1.2. The coding of Function Bits 0 through 3 is defined in table 1-4.

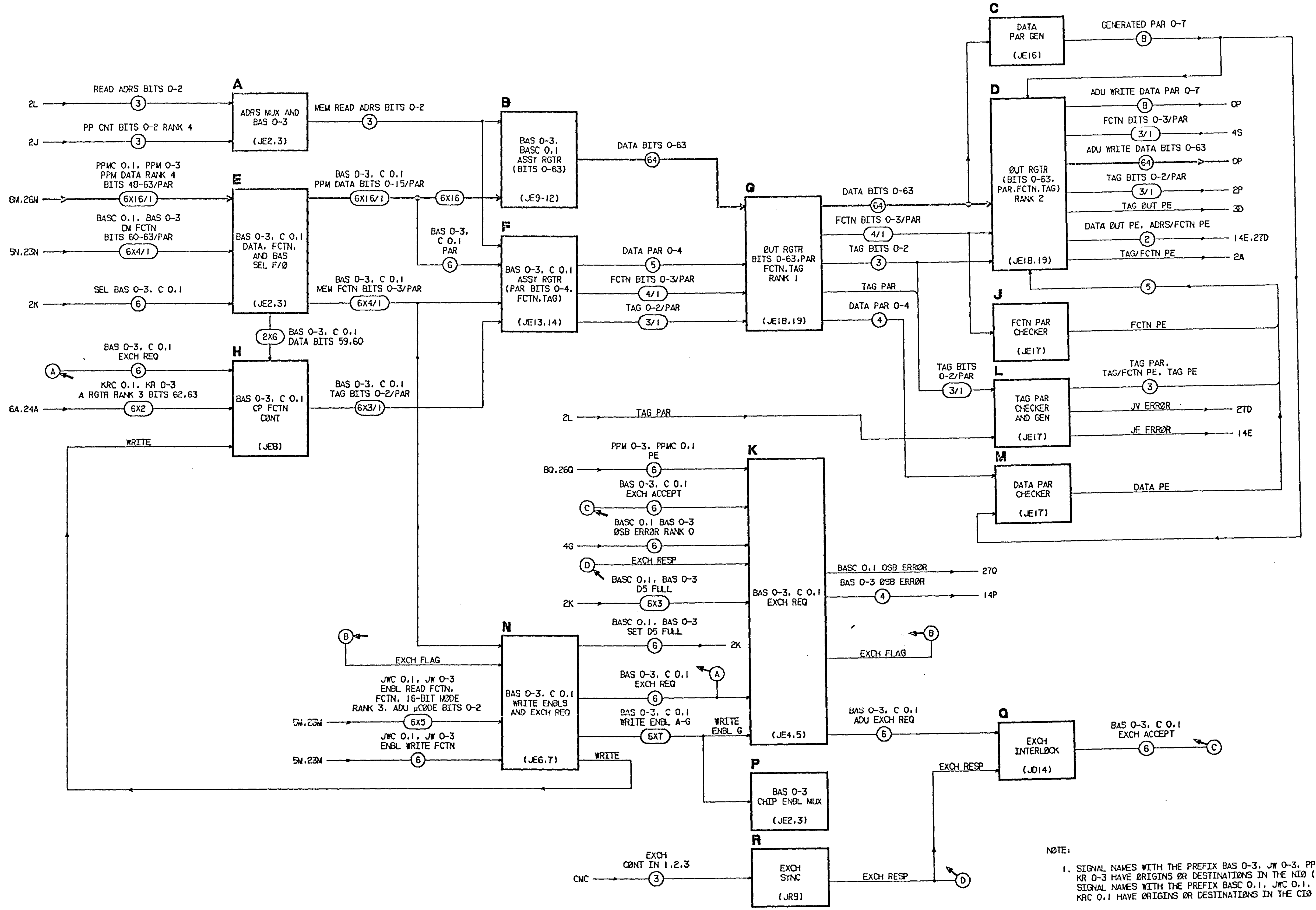
ADU EXCHANGE CONTROL

PP instructions 2600 through 2602 provide the IOU with the capability of initiating an exchange jump to place the associated CPU into 170 mode. When such an instruction is present, the Write Enables and Exchange Request circuits receive notification via Microcode Bits 0 through 2 from the BAS with the requesting PP. This sets an exchange busy flip-flop (FF) for requesting BAS in the Exchange Request logic, enables the appropriate tag bits, and generates an exchange request to the Exchange Interlock logic.

The Exchange Interlock logic selects one exchange request and disregards any others until the selected exchange request has been accepted by the Central Processor Unit (CPU). The selected exchange request and exchange jump address then go to the CMC when the requesting PP reaches the slot again. This request is defined in the tag bits sent to the CMC.

Table 1-4. Function Bits 0 Through 3

Binary Code	Desired CMC Operation
0000	Read from CM.
0010	Write to CM.
0100	Read and set lock - Assembled word from the IOU is ORed by the CMC with a word read from CM and the result is written into CM. In addition, the original word read from CM is sent to the IOU.
0101	Read and clear lock - Same as a read and set lock operation except that the CMC ANDs the words.
1100	Interrupt - The CMC sends an interrupt to the CPU that is specified by the IOU.


A
ADRS MUX AND BAS 0-3 (JE2,3)
READ ADRS BITS 0-2
3
2L
PP CNT BITS 0-2 RANK 4
3
2J
MEM READ ADRS BITS 0-2
3
B
BAS 0-3, BASC 0,1 ASSY RGTR (BITS 0-63) (JE9-12)
DATA BITS 0-63
64
E
BAS 0-3, C 0,1 DATA, FCTN, AND BAS SEL F/O (JE2,3)
PPMC 0,1, PPM 0-3 PPM DATA RANK 4 BITS 48-63/PAR
6X16/1
6W,26W
BASC 0,1, BAS 0-3 CW FCTN BITS 60-63/PAR
6X4/1
5N,23N
SEL BAS 0-3, C 0,1
6
2K
BAS 0-3, C 0,1 PPM DATA BITS 0-15/PAR
6X16/1
6X16
BAS 0-3, C 0,1 PAR
6
F
BAS 0-3, C 0,1 ASSY RGTR (PAR BITS 0-4, FCTN,TAG) (JE13,14)
BAS 0-3, C 0,1 MEM FCTN BITS 0-3/PAR
6X4/1
DATA PAR 0-4
5
FCTN BITS 0-3/PAR
4/1
TAG 0-2/PAR
3/1
G
OUT RGTR BITS 0-63,PAR FCTN,TAG RANK 1 (JE18,19)
DATA BITS 0-63
64
FCTN BITS 0-3/PAR
4/1
TAG BITS 0-2
3
TAG PAR
DATA PAR 0-4
4
2X6
BAS 0-3, C 0,1 DATA BITS 59,60
H
BAS 0-3, C 0,1 CP FCTN CONT (JE8)
BAS 0-3, C 0,1 EXCH REQ
6
A
KRC 0,1, KR 0-3 A RGTR RANK 3 BITS 62,63
6X2
6A,24A
BAS 0-3, C 0,1 TAG BITS 0-2/PAR
6X3/1
WRITE
C
DATA PAR GEN (JE16)
GENERATED PAR 0-7
8
D
OUT RGTR (BITS 0-63, PAR,FCTN,TAG) RANK 2 (JE18,19)
ADU WRITE DATA PAR 0-7
8
OP
FCTN BITS 0-3/PAR
3/1
4S
ADU WRITE DATA BITS 0-63
64
OP
TAG BITS 0-2/PAR
3/1
2P
TAG OUT PE
3D
DATA OUT PE, ADRS/FCTN PE
2
14E,27D
TAG/FCTN PE
2A
5
J
FCTN PAR CHECKER (JE17)
FCTN PE
L
TAG BITS 0-2/PAR
3/1
TAG PAR CHECKER AND GEN (JE17)
TAG PAR, TAG/FCTN PE, TAG PE
3
JV ERROR
27D
JE ERROR
14E
2L
TAG PAR
M
DATA PAR CHECKER (JE17)
DATA PE
K
BAS 0-3, C 0,1 EXCH REQ (JE4,5)
PPM 0-3, PPMC 0,1 PE
6
BQ,26Q
BAS 0-3, C 0,1 EXCH ACCEPT
6
C
BASC 0,1 BAS 0-3 OSB ERROR RANK 0
6
4G
EXCH RESP
D
BASC 0,1, BAS 0-3 D5 FULL
6X3
2K
BASC 0,1, BAS 0-3 SET D5 FULL
6
2K
BASC 0,1 OSB ERROR
27Q
BAS 0-3 OSB ERROR
4
14P
B
EXCH FLAG
N
BAS 0-3, C 0,1 WRITE ENBLS AND EXCH REQ (JE6,7)
B
EXCH FLAG
JWC 0,1, JW 0-3 ENBL READ FCTN, FCTN, 16-BIT MODE RANK 3, ADU μCODE BITS 0-2
6X5
5W,23W
JWC 0,1, JW 0-3 ENBL WRITE FCTN
6
5W,23W
BAS 0-3, C 0,1 EXCH REQ
6
A
BAS 0-3, C 0,1 WRITE ENBL A-G
6X7
WRITE ENBL G
WRITE
BAS 0-3, C 0,1 ADU EXCH REQ
6
Q
EXCH INTERLOCK (JD14)
BAS 0-3, C 0,1 EXCH ACCEPT
6
C
EXCH RESP
P
BAS 0-3 CHIP ENBL MUX (JE2,3)
R
EXCH SYNC (JR9)
EXCH CONT IN 1,2,3
3
CNC
EXCH RESP
D

NOTE:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A & B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0,1, JWC 0,1, PPMC 0,1 OR KRC 0,1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C & D PANELS).

CONTROL DATA	LEVEL 1 DIAGRAM ASSEMBLY	60463540	C
DEVELOPMENT DIVISION	NIO	IOU 1.3	

This diagram shows circuits of the R+A (JC) board and the CMI address (JJ) board. The JC board is part of each BAS.

BAS FORMATION OF CM ADDRESSES

The CM address used by a BAS when executing a CM read/write is formed from the contents of its R Register Rank 4 and/or A Register Rank 4. The CM address used is a real rather than a virtual memory address. If bit 46 of the A Register Rank 4 is not set, bits 47 through 63 of the A Register Rank 4 make up the CM address; or if bit 46 is set, the contents of the R Register Rank 4 are also used with the A Register Rank 4 bits to form a relocation address.

The R Register Rank 4 contains the starting boundary address for CM access. When a relocation address is to be formed, the R + A Adders:

- Perform a twos complement of bits 47 through 63 from the A Register Rank 4 with the contents of the R Register Rank 4.
- Add six zeros to the rightmost end.

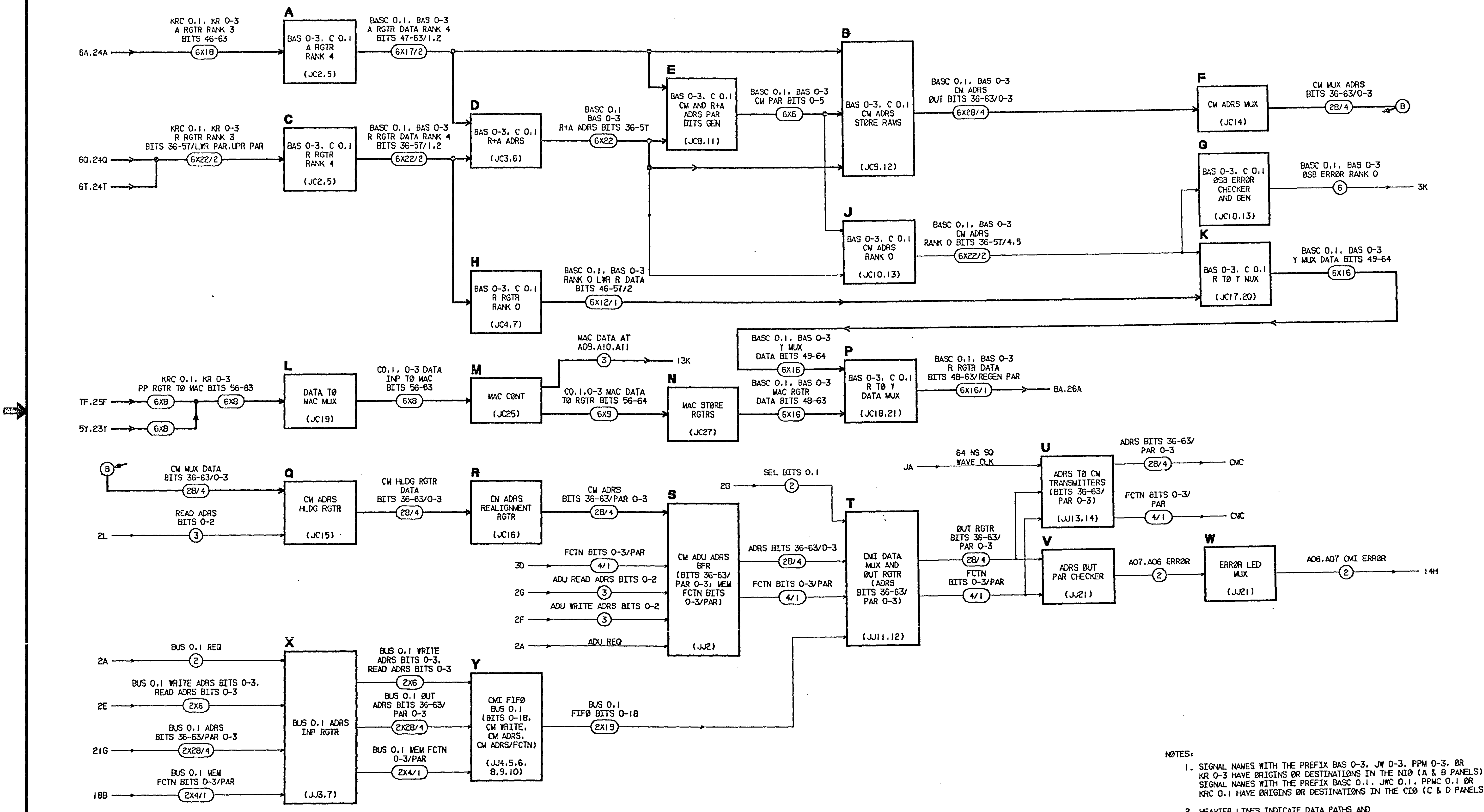
The formed address then enters the CM Address Store RAMs for holding until any existing PP conflict is resolved.

R-TO-Y DATA MUX

This circuit gates data to the Y Mux of the associated BAS (1.8 for NIO; 1.26 for CIO) for entry into the PPM or a functional register. Depending on the type of PP instruction being executed, this data may be a CM address from the R + A Adders, the contents of the R Register Rank 0, or data from the MAC (1.13).

CMI HANDLING OF CM ADDRESSES

The CMI buffers CM addresses originating from the ISI channels of the CIO and the BASs until the associated CM request is sent to the CMC. When the CMI sends the request, it also sends the associated CM address, tag information, and function code.



NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS O-3, JW O-3, PPM O-3, OR KR O-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A & B PANELS). SIGNAL NAMES WITH THE PREFIX BASC O.1, JWC O.1, PPMC O.1 OR KRC O.1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C & D PANELS).

2. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM
A4, R4, CM ADRS, R DATA
NIO
CODE IDENT
DWG NO 60463540
REV C
SHEET IOU 1.4
PAGE

This diagram shows circuits of the microcode (JW) board. The JW board is the major portion of each BAS. This diagram shows the JW board in use in the NIO, while diagram 1.23 shows its use in the CIO.

PPM DATA REGISTERS

A set of Rank 2, 3, 4, and 0 PPM Data Registers exist in each BAS. The data propagating through these registers has been read from the respective PPM (1.8) and is destined to the MAC, TPM, DSC, or a respective 170 I/O channel or the C or K barrel of the BAS.

K BARREL

The K barrel contains copies of the opcodes of the PP instructions being executed in the respective BAS. The current opcode or other portions of the current instruction word may be read by the MAC via the JW MAC Mux (1.4).

I BARREL AND INSTRUCTION DECODING CIRCUITS

The instruction decoding and execution control of each BAS is handled by the microcode residing in its Microcode Decoders. This microcode decodes the instruction opcode read from the respective PPM or the bits from the respective I barrel and generates the micrand bits needed to execute the instruction. The first micrand generated for an instruction is based on its opcode read from the PPM. If the instruction requires further micrands for completion, they are based on the bits from the I barrel. The multiplex of opcodes and I barrel bits is done by the New Function Select Register.

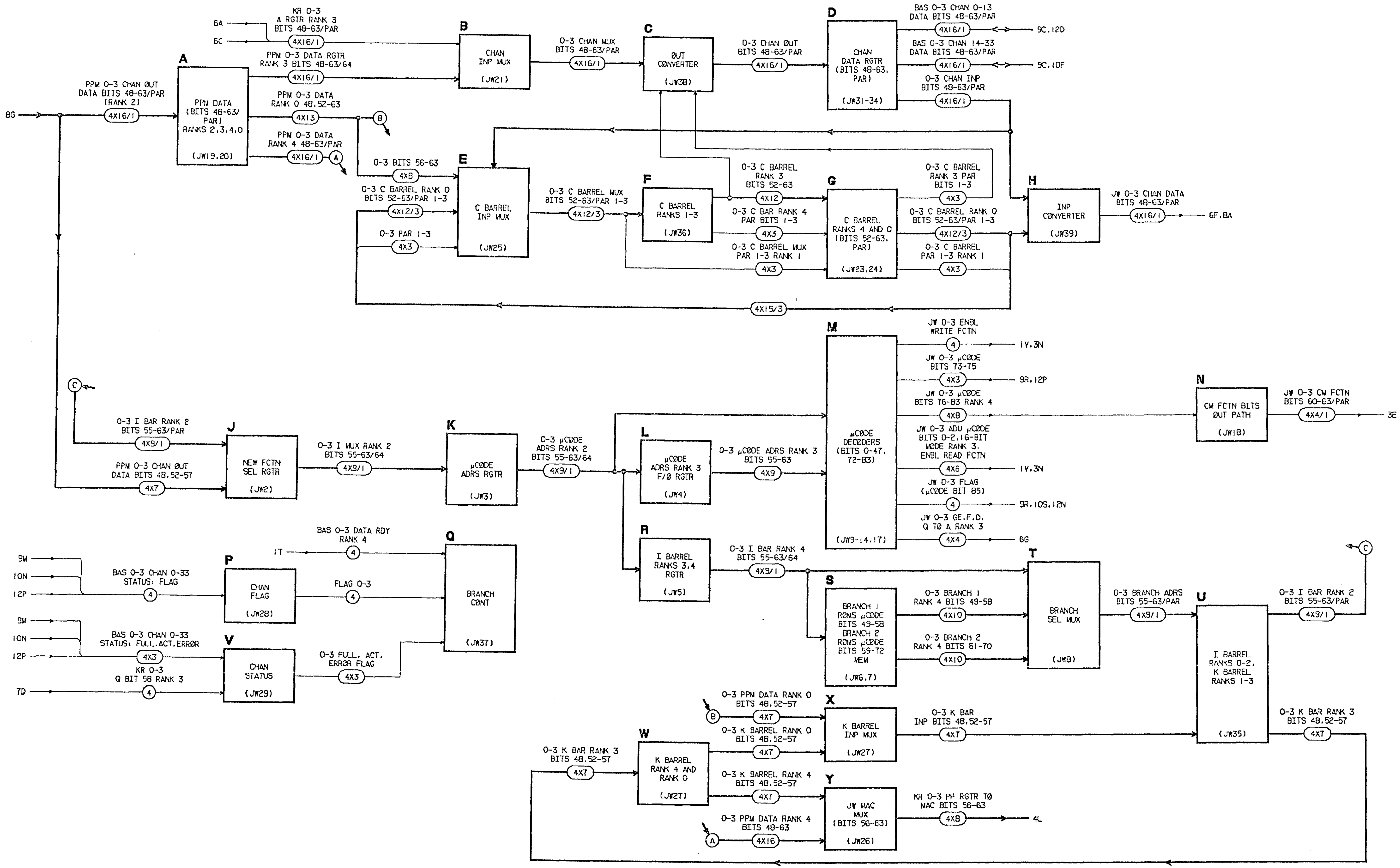
The bits from the I barrel reflect either a modified instruction opcode or a branch address. The Branch 1 ROM and Branch 2 ROM in the I barrel decode the modified opcode for branch conditions and generate a branch address as needed. The branch address or modified opcode then propagates into the Microcode Decoders at the next slot time for the associated instruction. This generates another set of micrand bits one major cycle (250 nanoseconds) after the previous associated set was generated. However, some instructions only require one set of micrand bits for execution and, therefore, complete in one major cycle.

C BARREL

As applicable, the C barrel of a BAS holds the least significant 12 bits of the previous word read from the PPM or received by the I/O channel for each PP. The C barrel uses this to perform input-packed and output-packed I/O instructions.

For an input-packed I/O instruction, the C barrel converts four I/O channel words into three 16-bit words for the PPM. In doing this, bits 48 through 51 in the original four words are omitted. The I/O channel words to be converted are received by the C barrel via the Channel Data Register. The input-packed conversion allows 16-bit PPM words to be read from 12-bit external devices.

For an output-packed I/O instruction, the C barrel performs just the opposite conversion. Instead of converting four words into three, it converts three PPM words into four I/O channel words. Bits 48 through 51 of the channel words are zeros.



NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM C BARREL, I BARREL, K BARREL	CODE IDENT / DWG NO 60463540	REV C
DEVELOPMENT DIVISION	NIO	SHEET IOU 1.5	PAGE

This diagram shows register (KR) board circuits in a BAS of the NIO. Diagram 1.24 shows the same circuits in a BAS of the CIO.

A BARREL

The A barrel of a BAS holds:

- Arithmetic or logical operands
- CM addresses (part or all depending on bit 46)
- I/O function or data words
- Word counts for block I/O instructions

The A Barrel Ranks 1 through 3 latch the previously specified information at rank 1 from the Shifter Y-to-A Mux and propagate the information to rank 3. At rank 3, the information is made available for possible I/O channel transmission (1.5) or for use as, or developing, a CM address (1.4). At rank 4, the A Register Rank 4 latches the information and makes it available to the A Adder for a possible arithmetic or logical operation. At rank 0, the A Bypass Register latches the information for possible return to the A barrel or possible storage in the PPM (1.8).

A ADDER

The A Adder performs ones complement addition or logical operation for instructions that use the contents of A Register Rank 4 and the selected output of the A Adder B Operand Mux as integer operands. The operand from the A Adder B Operand Mux depends on the instruction and may be from the PPM or the Q barrel (1.7) or a set of biased bits.

The result of the addition or logical operation, along with any pending shifts, cycles back through the A barrel to replace the original information for that slot.

SHIFTER Y-TO-A MUX

This circuit performs left circular shifts or right end-off shifts on A data for shift instructions. The result of the shift then cycles back through the A barrel. This circuit also provides the A barrel with input from the C barrel (1.5).

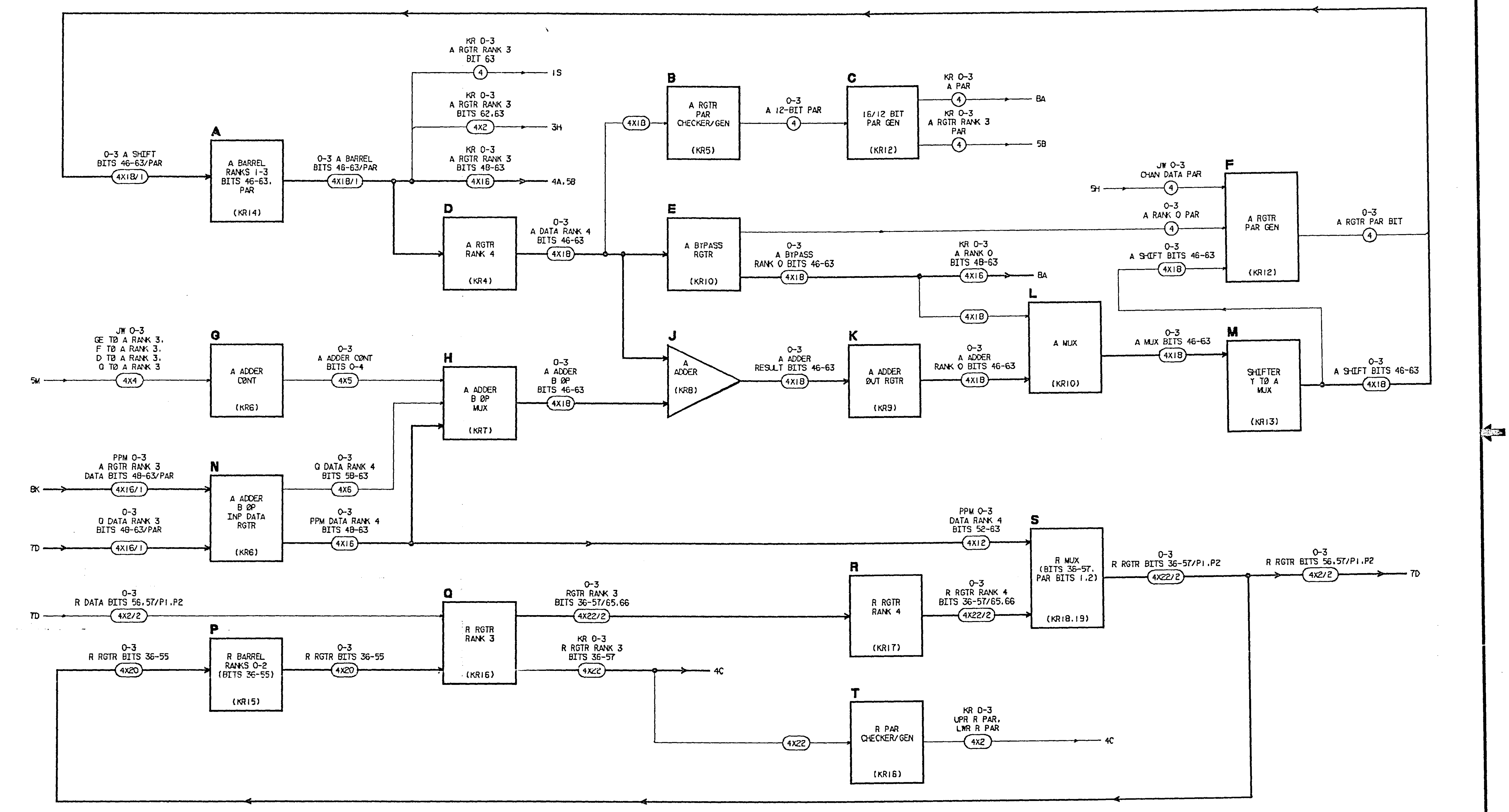
A BARREL PARITY CHECKING

The A Register Parity Generator regenerates parity after addition or a right end-off shift has been performed to A-barrel information. In addition, this circuit generates parity for new inputs from the C barrel.

When information reaches A Register Rank 4 in the barrel, the parity is checked. In addition, separate parity is generated in case the information is going to the PPM or an I/O channel. This parity is based on a 12- or 16-bit word, as applicable.

R BARREL

The R barrel holds the starting boundary addresses for CM read/write and exchange operations being performed in a BAS. Before such an operation, a starting boundary address is loaded into the R barrel through the R Mux by a load R instruction. At slot time, the boundary address is made available to the R+A Address Counter (1.4) for possible formation of a relocation address.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM
A BARREL, R BARREL
NIO

CODE IDENT | DWG NO 60463540 | REV C
SHEET IOU 1.6 | PAGE

P BARREL, Q BARREL (NIO) (IOU 1.7)

This diagram shows register (KR) board circuits in a BAS of the NIO. Diagram 1.25 shows the same circuits in a BAS of the CIO.

P BARREL AND P SLOT CIRCUITS

These circuits provide the PPM address where the next PP instruction is located (PPM is on 1.8). In addition, when a block I/O instruction or block CM read/write instruction is executed, these circuits also provide the PPM address for the next data transfer. With such block instructions, the following occurs.

1. The PPM address in the P Slot at the time of the block instruction is replaced with the starting PPM address for the data to be transferred in the block operation. The PPM address that was replaced is stored in the PPM at address 0.
2. The PPM address for the data transfer is incremented by 1 each time that a PPM word is written/read in the block operation.
3. After the block operation is completed, the PPM address stored in the PPM at address 0 is reinserted in its original position in the P barrel and its value is incremented by 1.

With instruction addresses, the P Slot increments or decrements them by 1 when they reach slot time. This provides instruction sequencing and is done using twos complement arithmetic. The incremented/decremented addresses then cycle back through the P barrel after being passed to the PPM.

Q BARREL AND Q SLOT CIRCUITS

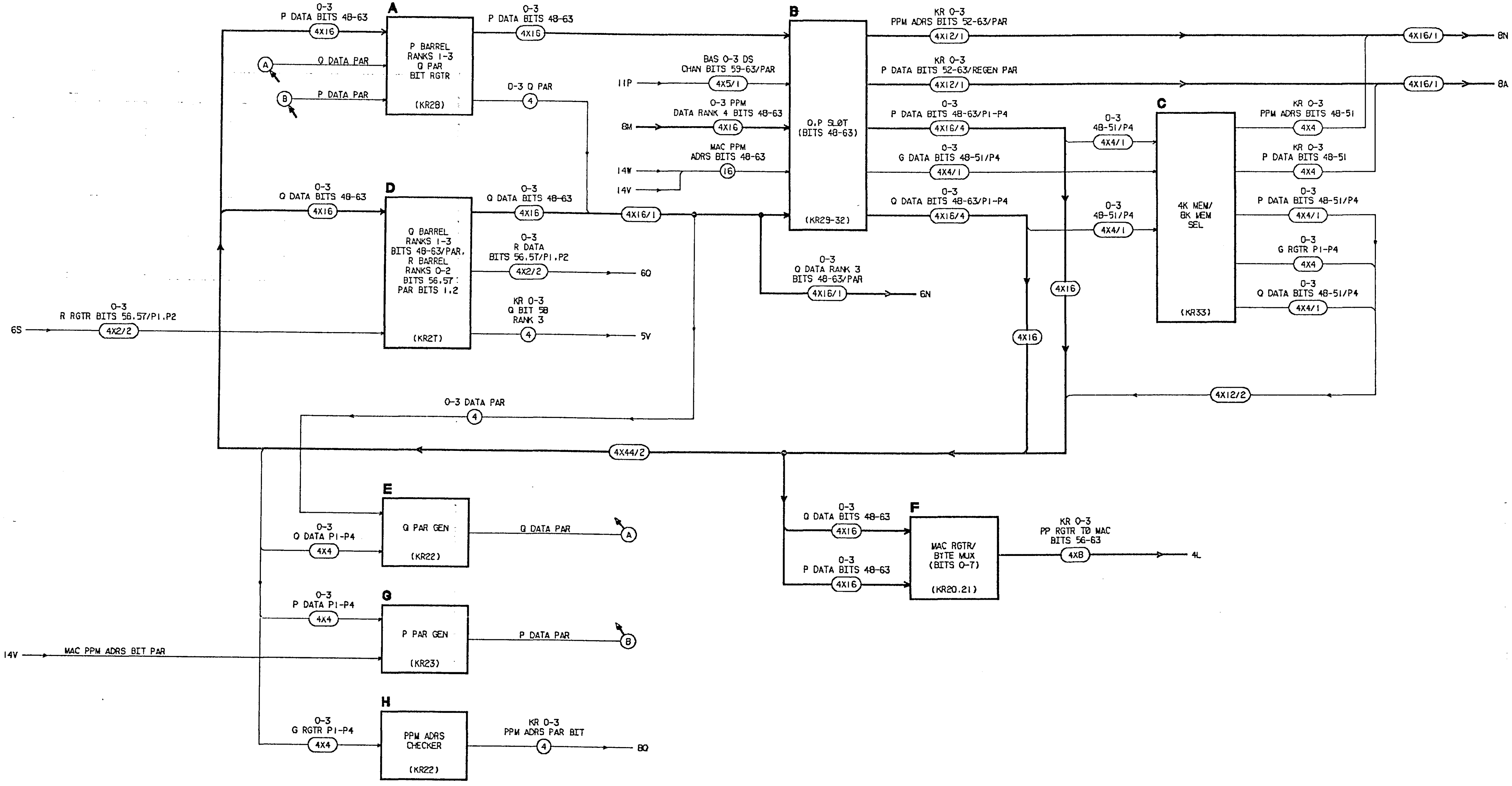
The Q barrel and Q Slot circuits of a BAS provide the following.

- The PPM address of an operand when the instruction being executed uses direct-mode, indirect-mode, or memory-mode addressing for operands.
- The PPM address when a jump instruction is being executed.
- The word count (number of CM words remaining to be transferred) when a block CM read/write is being executed.
- The number of the addressed channel when an I/O instruction is being executed.

The adder in the Q Slot is a ones complement adder. In block CM read/write operations, the number of CM words to be transferred are loaded in the Q barrel and the Q Slot decrements the number by 1 each time a CM word is transferred. The result of this is made available to the A adder input circuits (1.6) each slot time. This is done for possible logical or arithmetic manipulations.

4K/8K MEMORY SELECT CIRCUITS

In the NIO, diagnostics can switch the PPM from its normal 4K operation to 8K operation. This is selectable via Environment Control Register Bit 32 (1.15). When diagnostics select 8K mode, the 4K/8K Memory Select circuits provide the PPM with the extra address bits needed for 8K operation. In addition, in 8K mode, the 4K/8K Memory Select circuits also provide the P and Q barrels with the extra data bits needed to correspond with the additional addressable PPM.



NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM P BARREL, R BARREL, Q BARREL NIO	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION		SHEET IOU 1.T		PAGE

This diagram shows PPM (KB) board circuits in a BAS of the NIO. Diagram 1.26 shows the same circuits in a BAS of the CIO.

PPM FUNCTIONS

The PPM provides storage for PP instructions, operands, and I/O data.

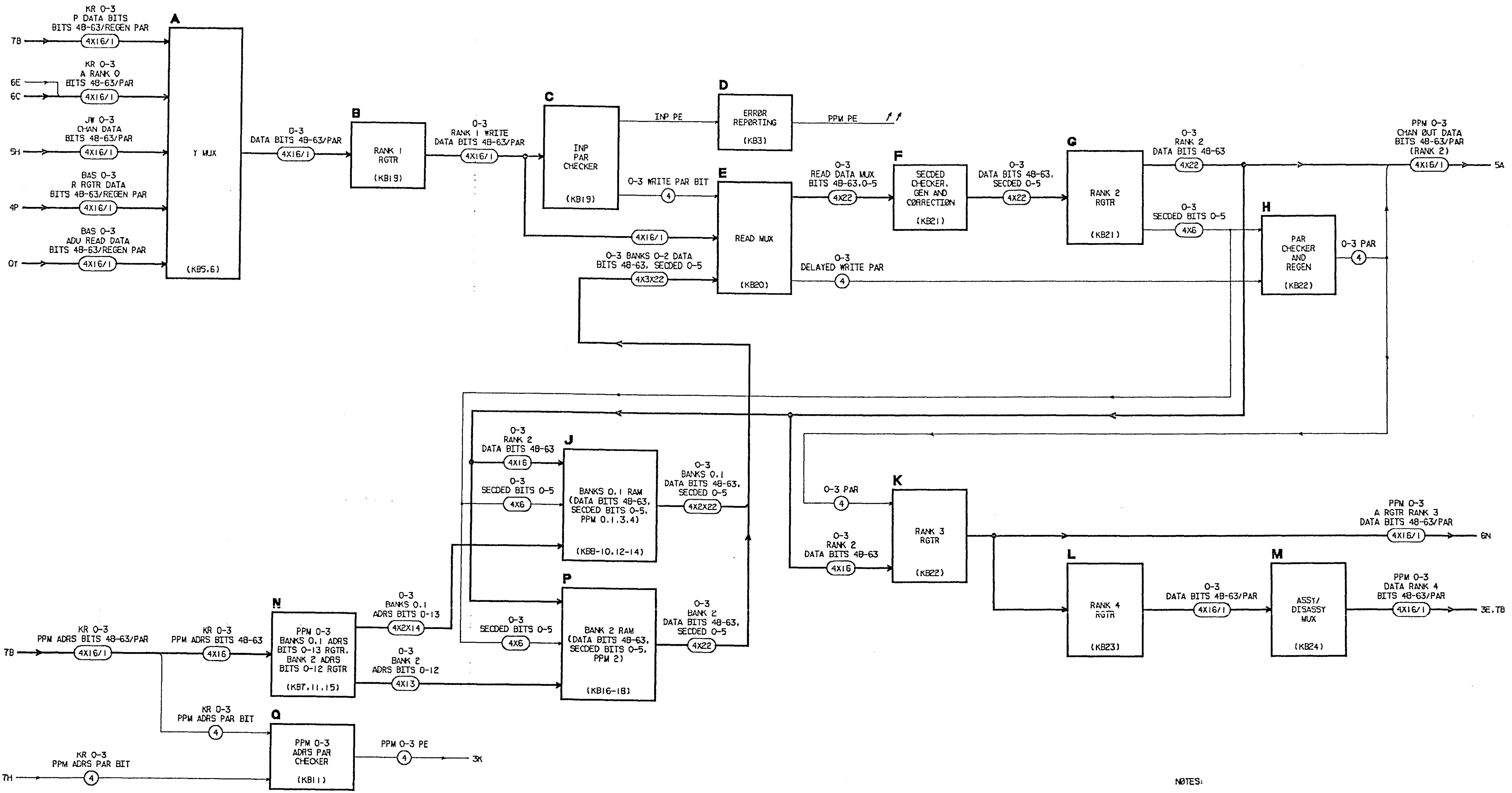
PPM CONFIGURATION

Each BAS has three banks (0, 1, and 2) of RAM for PPM. Each bank contains 16 384 x 22 bits of storage [16 384 x 6 bits of RAM is for single-error correction/double-error detection (SECDED) code]. PPs 0 and 3 share bank 0, PPs 1 and 4 share bank 1, and PP 2 has sole use of bank 2. This provides each PP with 8792 words of storage in 8K mode or 4096 words in normal 4K mode.

The banks of RAM are interconnected with a set of Rank 1 through 4 Registers that hold the information propagating to/from the RAM.

PPM ERROR CHECKING

Each word to be entered into the PPM is checked for correct parity at rank 1 before its parity bits are replaced with six SECDED code bits. As each word leaves the PPM, its SECDED code bits are replaced with two parity bits at rank 2.



NØTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM PP MEMØRY	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	NIØ	SHEET IØU 1.8	PAGE	

This diagram shows the 170-channel (JL) board circuits of the NIO.

CHANNEL SELECTION

All PPs of the NIO have equal access to I/O channels 0 through 13_8 and 20_8 through 33_8. The number of the I/O channel for an I/O instruction is indicated by the value in the Q barrel.

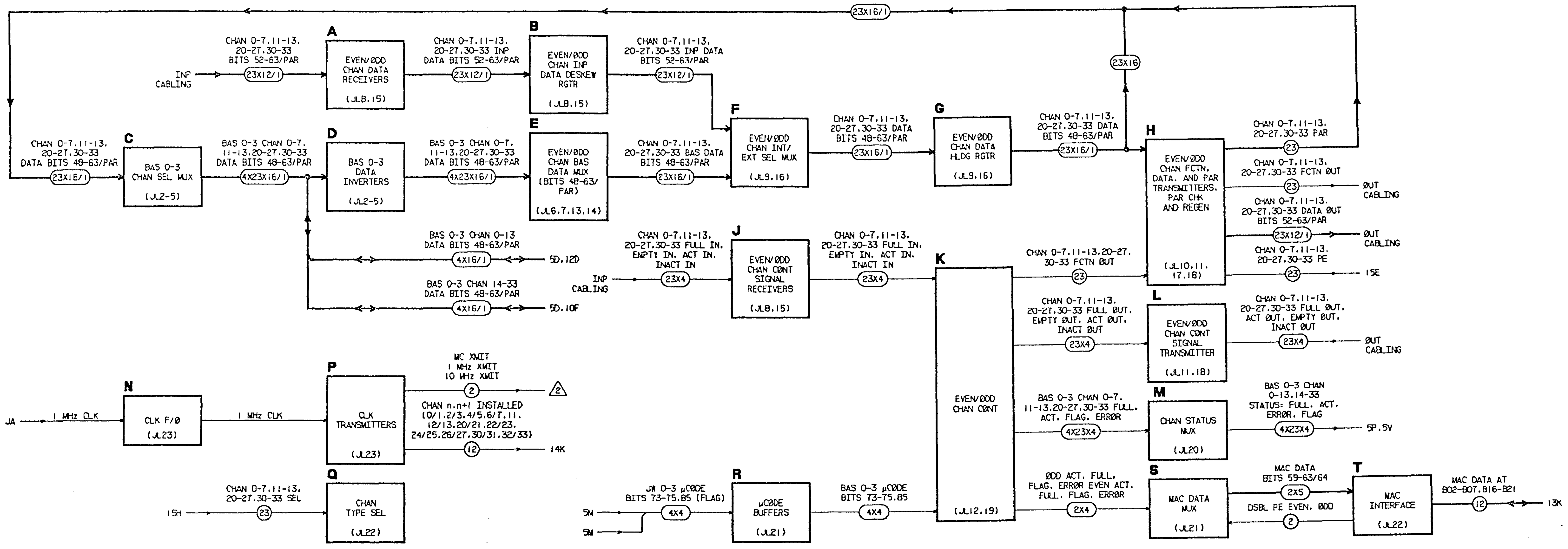
EVEN/ODD CHANNEL CONTROL

The control for the I/O channels is provided by the Even Channel Control circuits and the Odd Channel Control circuits. These control circuits are driven by microcode bits from the BASs. The control circuits keep track of whether channels are active, full, empty, transmitting a function code, or have an error. The control circuits also set/clear channel flags. Each I/O channel has a flag that is used by the software to indicate a jump condition.

I/O DATA

Depending on the I/O instruction being executed, output data to an external device may come from the C or A barrel of a BAS or its PPM. These same sources may also be the destination for data received from an external device.

Data transferred over the I/O channels consists of 12-bit words with 1 parity bit.


A
EVEN/ODD CHAN DATA RECEIVERS (JL8.15)
B
EVEN/ODD CHAN INP DATA DESKEW RGTR (JL8.15)
C
BAS 0-3 CHAN SEL MUX (JL2-5)
D
BAS 0-3 DATA INVERTERS (JL2-5)
E
EVEN/ODD CHAN BAS DATA MUX (BITS 48-63/PAR) (JL6.7.13.14)
F
EVEN/ODD CHAN INT/EXT SEL MUX (JL9.16)
G
EVEN/ODD CHAN DATA HLDG RGTR (JL9.16)
H
EVEN/ODD CHAN FCTN, DATA, AND PAR TRANSMITTERS, PAR CHK AND REGEN (JL10.11. 17.18)
J
EVEN/ODD CHAN CONT SIGNAL RECEIVERS (JL8.15)
K
EVEN/ODD CHAN CONT (JL12.19)
L
EVEN/ODD CHAN CONT SIGNAL TRANSMITTER (JL11.18)
M
CHAN STATUS MUX (JL20)
N
CLK F/O (JL23)
P
CLK TRANSMITTERS (JL23)
Q
CHAN TYPE SEL (JL22)
R
µCODE BUFFERS (JL21)
S
MAC DATA MUX (JL21)
T
MAC INTERFACE (JL22)
23X16/1
23X16
INP CABLING
CHAN 0-7.11-13, 20-27.30-33 BITS 52-63/PAR
23X12/1
CHAN 0-7.11-13, 20-27.30-33 INP DATA BITS 52-63/PAR
23X12/1
CHAN 0-7.11-13, 20-27.30-33 INP DATA BITS 52-63/PAR
23X12/1
CHAN 0-7.11-13, 20-27.30-33 DATA BITS 48-63/PAR
23X16/1
BAS 0-3 CHAN 0-7, 11-13.20-27.30-33 DATA BITS 48-63/PAR
4X23X16/1
BAS 0-3 CHAN 0-7, 11-13.20-27.30-33 DATA BITS 48-63/PAR
4X23X16/1
CHAN 0-7.11-13, 20-27.30-33 BAS DATA BITS 48-63/PAR
23X16/1
BAS 0-3 CHAN 0-13 DATA BITS 48-63/PAR
4X16/1
5D.12D
BAS 0-3 CHAN 14-33 DATA BITS 48-63/PAR
4X16/1
5D.10F
CHAN 0-7.11-13, 20-27.30-33 DATA BITS 48-63/PAR
23X16/1
CHAN 0-7.11-13, 20-27.30-33 DATA BITS 48-63/PAR
23X16/1
CHAN 0-7.11-13, 20-27.30-33 PAR
23
CHAN 0-7.11-13, 20-27.30-33 FCTN OUT
23
OUT CABLING
CHAN 0-7.11-13, 20-27.30-33 DATA OUT BITS 52-63/PAR
23X12/1
OUT CABLING
CHAN 0-7.11-13, 20-27.30-33 PE
23
15E
INP CABLING
CHAN 0-7.11-13, 20-27.30-33 FULL IN, EMPTY IN, ACT IN, INACT IN
23X4
CHAN 0-7.11-13, 20-27.30-33 FULL IN, EMPTY IN, ACT IN, INACT IN
23X4
CHAN 0-7.11-13.20-27, 30-33 FCTN OUT
23
CHAN 0-7.11-13, 20-27.30-33 FULL OUT, EMPTY OUT, ACT OUT, INACT OUT
23X4
CHAN 0-7.11-13, 20-27.30-33 FULL OUT, ACT OUT, EMPTY OUT, INACT OUT
23X4
OUT CABLING
BAS 0-3 CHAN 0-7, 11-13.20-27.30-33 FULL, ACT, FLAG, ERROR
4X23X4
BAS 0-3 CHAN 0-13.14-33 STATUS: FULL, ACT, ERROR, FLAG
4X23X4
5P.5V
JA
1 MHz CLK
1 MHz CLK
MC XMIT
1 MHz XMIT
10 MHz XMIT
2
2
CHAN n,n+1 INSTALLED (0/1.2/3.4/5.6/7.11, 12/13.20/21.22/23, 24/25.26/27.30/31.32/33)
12
14K
15H
CHAN 0-7.11-13, 20-27.30-33 SEL
23
5N
5N
JW 0-3 µCODE BITS 73-75.85 (FLAG)
4X4
BAS 0-3 µCODE BITS 73-75.85
4X4
ODD ACT, FULL, FLAG, ERROR EVEN ACT, FULL, FLAG, ERROR
2X4
MAC DATA BITS 59-63/64
2X5
DSBL PE EVEN, ODD
2
MAC DATA AT B02-B07.B16-B21
12
13K

NOTE:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

⚠2 CLOCK SIGNALS ARE USED THROUGHOUT THE IOU.

CONTROL DATA	LEVEL 1 DIAGRAM IOU CHANNELS 0-7.11-13.20-27.30-33 NIB	60463540	C
DEVELOPMENT DIVISION		SHEET IOU 1.9	PAGE

This diagram shows mostly utility (JM) board circuits. The utility channels these circuits form are accessible to the BASs of either the NIO or CIO. Such access is obtained through I/O instructions that address a utility channel by number.

CHANNEL 14

Channel 14 provides BAS access to read the Real Time Clock. The Real Time Clock is a free-running counter that increments every microsecond. The Real Time Clock has a 12-bit output.

CHANNEL 15

Channel 15 connects to the TPM (1.11). The TPM initializes the IOU during a deadstart and provides a serial, asynchronous communication link for CC634 Display Terminals or CC598 System Consoles. Such a link allows:

- The system to be deadstarted by keyboard entries at a local CC634 terminal or CC598 console.
- The system to be deadstarted by keyboard entries at a remote CC634 terminal.
- I/O instructions to be performed over channel 15.
- BAS access to a calendar clock on the TPM.

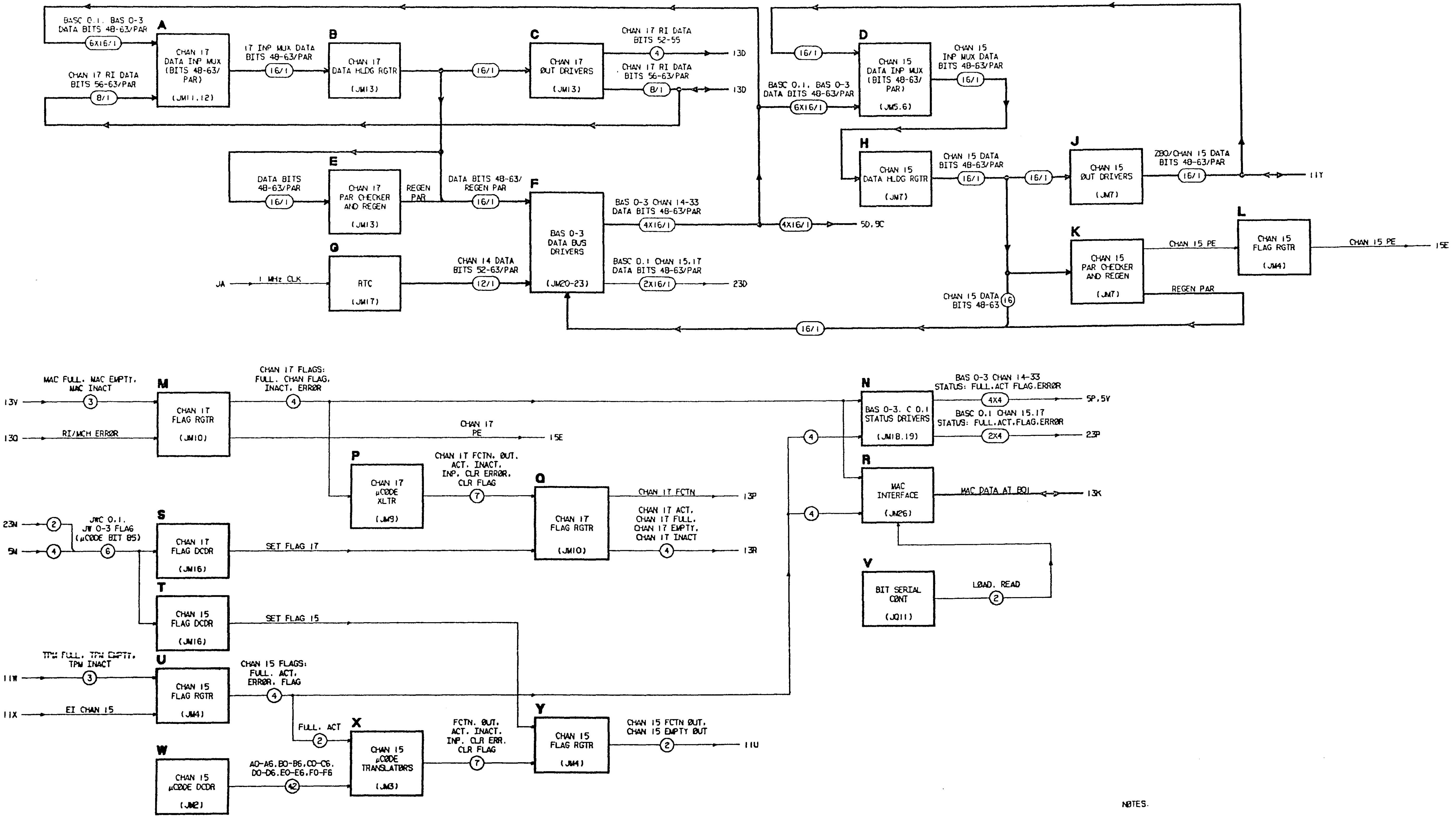
I/O operations over channel 15 are controlled by microcode bits and function codes from the BASs. The Channel 15 Microcode Decoder determines from the BAS microcode for what purpose the TPM has been selected. The purpose may be to:

- Send a function code
- Activate channel 15
- Set channel 15 full
- Set channel 15 empty
- Inactivate channel 15
- Clear an error
- Clear the channel 15 flag

If the microcode indicates that a function code is being sent, the TPM Function Decoder (1.11) determines what function the TPM is to perform.

CHANNEL 17

Channel 17 is the maintenance channel. It connects to the radial interfaces of the IOU (1.13) and IOU MAC (1.13). The radial interfaces carry communications to/from the MAC units for the system CPU and CM. This allows the operating conditions of the CPU and CM to be monitored and controlled by IOU I/O instructions. Such control is used to initialize the CPU and CM elements during a deadstart.



NØTES.

1. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM
CHANNEL 14 (REAL TIME CLK)
CHANNEL 15. CHANNEL 17
NIØ

DWG NO 60463540
REV C
SHEET IØU 1.10

This diagram shows the TPM (JK) board circuits. The TPM is accessible to all the BASs via channel 15. In addition, data paths exist between the TPM, MAC, and DSC.

Z80 MICROPROCESSOR

The Z80 CPU and Bus Drivers (shown at the upper left) are the heart of the TPM. All data that comes into or leaves the TPM passes through the Z80. The bus drivers are needed because the Z80 does not have enough current drive capability to feed all of the chips on the address bus. The TPM Reset circuit initiates the Z80 to start executing its initialization routine at address 0 whenever power is applied or a deadstart is initiated. Switch Drivers convert the ground or +5-volt level coming from the TPM Switch Panel into the tri-state level used on the data bus.

RS232 Drivers convert the transistor-transistor-logic (TTL) signals from the Universal Asynchronous Receiver/Transmitter (UART) to RS232-level signals and the RS232 Receivers do vice versa. The UART assembles the asynchronous serial-bit stream into bytes and transfers them in parallel form to the Z80.

EPROM

The erasable programmable read-only memory (EPROMs) contain the microcode for the Z80 microprocessor. This microcode allows the Z80 to operate either in deadstart or TPM mode. In deadstart mode, the main responsibility of the Z80 is to interpret and execute deadstart display commands entered at the keyboard of a CC634 Display Terminal, CC598 System Console, or CC545 Display Station. In TPM mode, the main responsibility of the Z80 is to interpret function codes from channel 15 and relay data between channel 15 and ports 0 and 1.

CHANNEL 15 INTERFACE

The channel 15 interface is shown at the bottom. Channel 15 Input Port FIFO Buffers store all data coming from channel 15 except function codes. Each port has an 8-bit wide by 64-word deep FIFO buffer. Function codes from a PP take the path that bypasses the FIFO buffers. This allows the Z80 to read the 12-bit function code instead of the 8-bit FIFO data.

Table 1-5 defines the function codes for the TPM.

FUNCTION DATA OUTPUT PORTS

The Function and Data Output Ports are shown at the upper right. Function and output data have separate ports. Function data goes to the Z80 Function Converter and TTL Decoder that controls the interface of channels 10, 15, and 17. This decoder also controls various functions within the TPM. The output data goes either to the DSC, MAC, or channel 15. If the data is going to channel 15, it goes through the Holding Registers one byte at a time. If the data is from port 0 or 1, two status bits accompany the data byte.

PP AND DEADSTART NUMBER COUNTERS

These free-running counters are shown at the right. When the Deadstart Master Clear signal (not shown) occurs during a deadstart, it gates the numbers being generated by the Deadstart Number Counters to the Q barrels in the NIO BASs. This informs the PPs which channel they should do an input on. The Deadstart Channel Number Mux is needed because there are different combinations of Deadstart Number Counter bits that can be generated depending on the reconfiguration of the system. The multiplexer produces the proper combination of counter bits depending on the reconfiguration.

DATA TRANSFERS

The following paragraphs describe the data transfers performed by the TPM.

CC634 DISPLAY TERMINAL OR CC598 SYSTEM CONSOLE TO CHANNEL 15

Data received from a terminal or console comes in serially in an asynchronous RS-232-C format and is converted into a parallel data byte by the UART. The receipt of a byte by the UART interrupts the Z80. After determining which port generated the interrupt, the Z80 reads the byte from the UART of that port. The Z80 then stores any byte going to channel 15 into a soft FIFO buffer in RAM or directly into a Holding Register if it is not full.

The RAM contains a separate soft FIFO buffer for port 0 and 1. Each buffer holds up to four 10-bit port data words. In the microcode′s main loop, the Z80 checks the buffers for data. When a byte is found, the Z80 checks whether the associated Holding Register is empty. If so, the Z80 sends the byte through the Data Output Port and issues function bits that enter the byte into the Holding Register for port 0 or 1. If the Holding Register is full, no transfer occurs from the soft FIFO buffer.

When a byte is transferred into a Holding Register, a status bit is generated to indicate that the register is full. The PP monitoring channel 15 is responsible for detecting the full Holding Register and gating the data. If this is not done in a timely manner, an overrun may occur in the associated soft FIFO buffer; because the Z80 does not load a new byte into a Holding Register until the previous byte has been input. Such an overrun is indicated in a status bit, and the last byte received is the one that is overwritten in the soft FIFO buffer by the next incoming byte.

Table 1-5. TPM Function Codes (Sheet 1 of 2)

Octal Code†	TPM Function
7xx0	Select port 0 - Connects TPM port 0 to channel 15.
7xx1	Select port 1 - Connects TPM port 1 to channel 15.
6xxx	Deselect port 0 or port 1 - Disconnects both TPM ports from channel 15 but does not affect communications between the TPM and an external device.
1x02	Read deadstart terminal - TPM identifies which terminal initiated a short deadstart by returning a word of 000 for the CC545 Display Station, 021_{16} for a CC634 Display Terminal on port 0, 022_{16} for a CC634 Display Terminal on port 1, 031_{16} for a CC598 System Console on port 0, or 032_{16} for a CC598 System Console on port 1.
1x04	Read calendar clock - TPM returns eight words of calendar clock data.
1x05	Write calendar clock - TPM writes the six words that follow on channel 15 into the calendar clock.
1x20-1x26	Read predeadstart copies of P, Q, K, and A barrels - TPM returns the barrel values that it stored in RAM prior to the deadstart. The function code indicates which BAS the TPM is to return the values for: 1x20 = NIO BAS 0 1x21 = NIO BAS 1 1x22 = NIO BAS 2 1x23 = NIO BAS 3 1x24 = CIO BAS 0 1x25 = CIO BAS 1 1x26 = ALL BASs
1x27	Read predeadstart copies of channel status - TPM returns the values for NIO and CIO channel status that it stored in RAM prior to the deadstart.
1x36††	Read System Console System Information - PP reads System Console system information stored in TPM on the selected port.
1x52††	Read Packet Status - PP reads TPM packet buffer status on the selected port.
1x53††	Write Packet - PP writes output packet buffer in TPM on the selected port.
1x54††	Read Packet - PP reads input packet buffer in TPM on the selected port.
1x55††	Clear Packets - PP clears output and input packet buffers in TPM on the selected port.

Table 1-5. TPM Function Codes (Sheet 2 of 2)

Octal Code†	TPM Function
00xx	Read TPM status - TPM returns a word that indicates the status of the selected port. Bit — Meaning When Set 52-58 — Not used 59 — Output buffer not full 60 — Input data ready 61 — Carrier On signal being received 62 — Data Set Ready signal being received 63 — Ring Indicator signal being received
01xx	Read port data - TPM returns a word that contains data received by the selected port plus port status information. Bit — Contents 52 — Data Set Ready indicator 53 — Data Set Ready and Carrier On indicator 54 — Data-in overrun indicator 55 — Data-in framing error or parity error indicator 56-63 — Received data
02xx	Write port data - Precedes data from channel 15 that is to be transmitted by the selected port.
03xx	Set TPM operating mode - Bits 58 through 63 of the 03xx function code specify the type parity and word format to be used on ports 0 and 1 and whether the TPM is to loop data back from channel 15.
04x0	Clears the Data Terminal Ready signal on the selected port.
04x1	Sets the Data Terminal Ready signal on the selected port.
05x0	Clears the Request to Send signal on the selected port.
05x1	Sets the Request to Send signal on the selected port.
07xx	Clears the output and input buffers for the selected port.

† The decoding of the least significant octal digit of function codes 04x0, 04x1, 05x0, 05x1, 7xx0, and 7xx1 is based on bit 63 only. Bits 62 and 61 are disregarded.

††Applies to systems with CC598 System Console only.

CHANNEL 15 TO CC634 DISPLAY TERMINAL OR CC598 SYSTEM CONSOLE

Channel 15 can write data to a terminal or console via either port 0 or 1. This type transfer is initiated by channel 15 issuing an octal 02xx function code, which goes to the TPM Function Decoder for decoding. Only one port can be selected for a transfer at a time. If the hardware FIFO buffer for the selected port is not full, the TPM returns an Empty signal back to channel 15 to indicate that the transfer may proceed; or if the FIFO buffer is full, the TPM returns an Inactive signal.

With an Empty signal returned, channel 15 transfers a data byte consisting of the least significant eight bits. The byte enters the appropriate Channel Input Port FIFO Buffer where it takes about 16 microseconds to propagate through the buffer. When the byte reaches the output of the buffer, a control signal is set that makes the Z80 read the byte through the Data Input Port. The Z80 then sends the byte to the UART for conversion to RS232-C serial data before being transmitted to the terminal or console.

PACKET DATA (CC598 System Console Only)

Some of the data transfers the TPM performs involve data formatted into packets. A packet is a sequence of bytes formatted such that the sequence is treated as a block of data. Some packet transfers occur between a PP on channel 15 and the system console. In this case, the TPM simply passes the packet through. Other packet transfers occur between the TPM and the system console; channel 15 is not involved.

Packet Read Data

When packet data is sent from the system console to either the TPM or the PP, the packet first arrives at the TPM´s UART on one of the ports. From there it transfers to the RAM. If the transfer is between the system console and the TPM, the packet transfer is complete. However, if the transfer is between the system console and a PP on channel 15, the PP must issue a read packet function on channel 15 and input the packet data from the RAM. The TPM transfers this data to the non-RS232 holding register one byte at a time until the entire packet has been transferred to the PP.

Packet Write Data

The PP on channel 15 sends packet data to the system console by first issuing a write packet function. The PP then writes packet data into the TPM´s RAM. After the data is in RAM and channel 15 is disconnected, the TPM sends the packet to the system console through the UART on the selected port.

TRANSFERRING OF MAC DATA

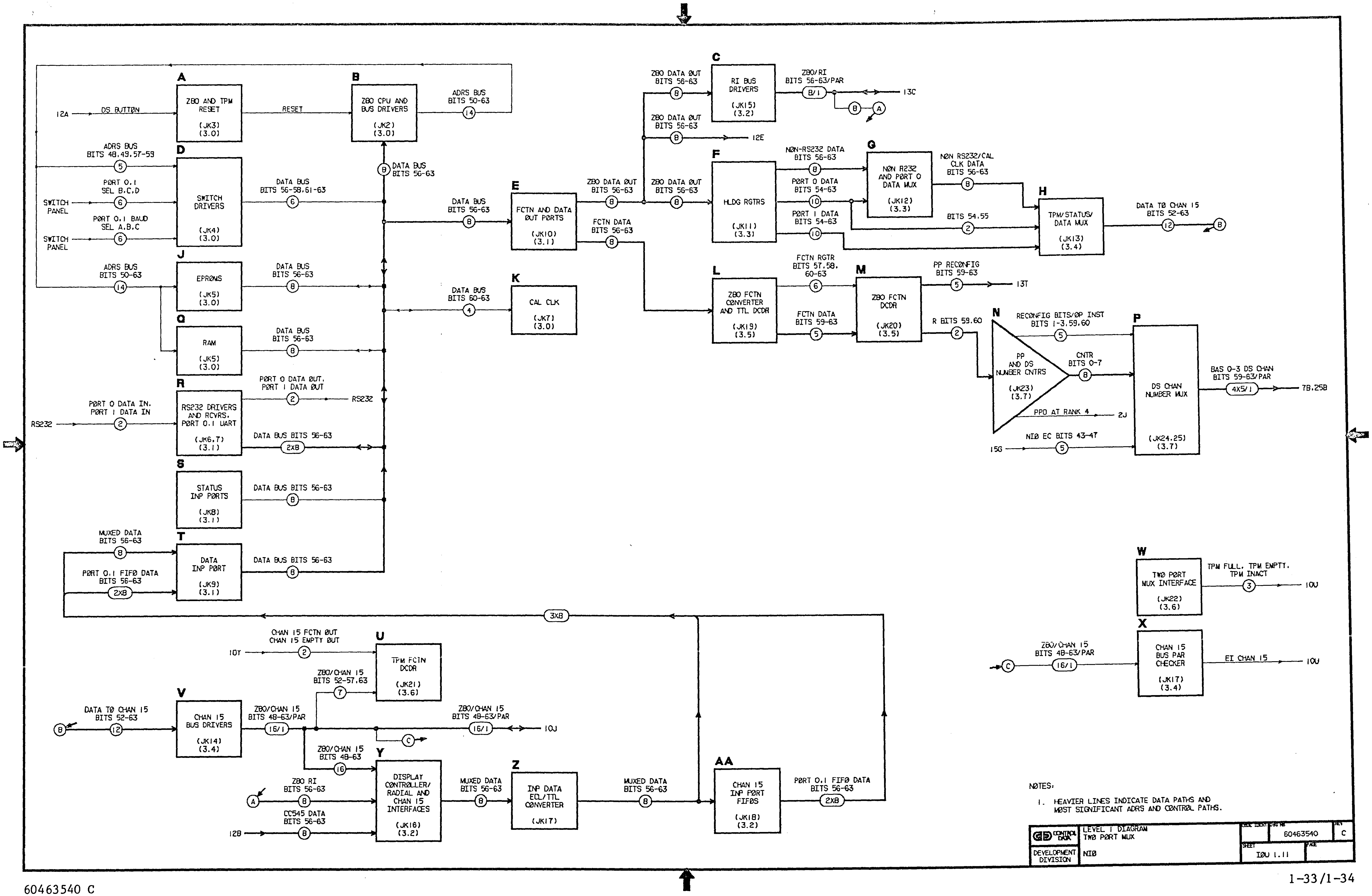
The Z80 can either read from or write to the MAC. Data read from the MAC comes in on the bidirectional data line shown to the right of the RI Bus Drivers. This data is gated through a multiplexer in the Display Controller/Radial and Channel 15 Interfaces and goes through the Input Data ECL/TTL Converter. The Input Data ECL/TTL Converter changes the negative signal levels that are sent from channel 17 into the TTL levels which the Z80 uses. The data (Muxed Data Bits 56 through 63) then goes through the Data Input Port and into the Z80.

The Z80 converts the data to ASCII code and generates display headings and screen coordinates. If the transfer is to the CC634 terminal or CC598 console, the Z80 sends the byte to the UART. If the transfer is to the DSC, the Z80 sends the byte through the Data Output Port.

Data written to the MAC goes from the Z80 through the Data Output Port and out the RI Bus Drivers.

TRANSFERRING OF DSC DATA

Data from the Z80 to the DSC passes through the Data Output Port. Data from the DSC to the Z80 (CC545 Data Bits 55 through 63) goes through the Input Data ECL/TTL converter, passes through the Data Input Port, and into the Z80. When keys are being pressed at the CC545, the Z80 reads the key characters one at a time and assembles them in a buffer contained in the RAM. In most cases, the Z80 assembles the characters until a carriage return occurs and then decodes the character string into a Z80 command. However, the Z80 recognizes some single-character commands before any carriage return.


A
Z80 AND TPM RESET (JK3) (3.0)
B
Z80 CPU AND BUS DRIVERS (JK2) (3.0)
C
RI BUS DRIVERS (JK15) (3.2)
D
SWITCH DRIVERS (JK4) (3.0)
E
FCTN AND DATA OUT PORTS (JK10) (3.1)
F
HLDG RGTRS (JK11) (3.3)
G
NON R232 AND PORT 0 DATA MUX (JK12) (3.3)
H
TPM/STATUS/ DATA MUX (JK13) (3.4)
J
EPROMS (JK5) (3.0)
K
CAL CLK (JK7) (3.0)
L
Z80 FCTN CONVERTER AND TTL DCDR (JK19) (3.5)
M
Z80 FCTN DCDR (JK20) (3.5)
N
PP AND DS NUMBER CNTRS (JK23) (3.7)
P
DS CHAN NUMBER MUX (JK24,25) (3.7)
Q
RAM (JK5) (3.0)
R
RS232 DRIVERS AND RCVRS, PORT 0,1 UART (JK6,7) (3.1)
S
STATUS INP PORTS (JK8) (3.1)
T
DATA INP PORT (JK9) (3.1)
U
TPM FCTN DCDR (JK21) (3.6)
V
CHAN 15 BUS DRIVERS (JK14) (3.4)
W
TWO PORT MUX INTERFACE (JK22) (3.6)
X
CHAN 15 BUS PAR CHECKER (JK17) (3.4)
Y
DISPLAY CONTROLLER/ RADIAL AND CHAN 15 INTERFACES (JK16) (3.2)
Z
INP DATA ECL/TTL CONVERTER (JK17)
AA
CHAN 15 INP PORT FIFOS (JK18) (3.2)
12A
DS BUTTON
RESET
ADRS BUS BITS 50-63
14
ADRS BUS BITS 48,49,57-59
5
SWITCH PANEL
PORT 0,1 SEL B,C,D
6
PORT 0,1 BAUD SEL A,B,C
6
SWITCH PANEL
DATA BUS BITS 56-58,61-63
6
DATA BUS BITS 56-63
8
ADRS BUS BITS 50-63
14
DATA BUS BITS 56-63
8
DATA BUS BITS 56-63
8
DATA BUS BITS 56-63
8
DATA BUS BITS 60-63
4
PORT 0 DATA OUT, PORT 1 DATA OUT
2
RS232
RS232
PORT 0 DATA IN, PORT 1 DATA IN
2
DATA BUS BITS 56-63
2X8
DATA BUS BITS 56-63
8
MUXED DATA BITS 56-63
8
PORT 0,1 FIFO DATA BITS 56-63
2X8
DATA BUS BITS 56-63
8
3X8
Z80 DATA OUT BITS 56-63
8
Z80 DATA OUT BITS 56-63
8
12E
Z80 DATA OUT BITS 56-63
8
Z80 DATA OUT BITS 56-63
8
FCTN DATA BITS 56-63
8
Z80/RI BITS 56-63/PAR
8/1
13C
8
A
NON-RS232 DATA BITS 56-63
8
PORT 0 DATA BITS 54-63
10
PORT 1 DATA BITS 54-63
10
NON RS232/CAL CLK DATA BITS 56-63
8
BITS 54,55
2
DATA TO CHAN 15 BITS 52-63
12
B
FCTN RGTR BITS 57,58, 60-63
6
FCTN DATA BITS 59-63
5
PP RECONFIG BITS 59-63
5
13T
R BITS 59,60
2
RECONFIG BITS/OP INST BITS 1-3,59,60
5
CNTR BITS 0-7
8
PPO AT RANK 4
2J
15G
NIO EC BITS 43-47
5
BAS 0-3 DS CHAN BITS 59-63/PAR
4X5/1
7B,25B
TPM FULL, TPM EMPTY, TPM INACT
3
10U
C
Z80/CHAN 15 BITS 48-63/PAR
16/1
EI CHAN 15
10U
10T
CHAN 15 FCTN OUT CHAN 15 EMPTY OUT
2
Z80/CHAN 15 BITS 52-57,63
7
B
DATA TO CHAN 15 BITS 52-63
12
Z80/CHAN 15 BITS 48-63/PAR
16/1
Z80/CHAN 15 BITS 48-63/PAR
16/1
10J
C
Z80/CHAN 15 BITS 48-63
16
A
Z80 RI BITS 56-63
8
CC545 DATA BITS 56-63
8
12B
MUXED DATA BITS 56-63
8
MUXED DATA BITS 56-63
8
PORT 0,1 FIFO DATA BITS 56-63
2X8

NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM TWO PORT MUX	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	NIO	SHEET IOU 1.11	PAGE

This diagram shows the optional DSC. When installed, the DSC is connected to I/O channel 10. This channel is only accessible to the BASs in the N10. The TPM also has access to the DSC.

DSC FUNCTIONS

The DSC handles the I/O exchanges that occur between a CC545 Display Station and a BAS or the TPM. In doing this, the DSC converts:

- The data going to the display station into coordinate, unblank, and movement signals for the station's CRT beam.
- The code generated from a pressed display station key into an ASCII code. However, this only applies to 180-mode and TPM operations. No key code conversions are done in 170-mode operations.

DSC OPERATIONS

The DSC operations done over channel 10 are described in the following text. After that, the DSC operations with the TPM are described.

OPERATIONS DONE OVER CHANNEL 10

The DSC operations done over channel 10 are controlled by the function words sent by the BASs in the NIO. These function words are defined in table 1-6.

The decoding of the DSC function words is done by the Display Controller Input Mux circuits. Once a selection is made, the DSC handles subsequent data in a similar manner until another function word changes the selection.

Character Mode

When the DSC is in character mode, it processes data from channel 10 in the following manner:

- The rightmost nine bits of words of $6xxx_8$ in 170 mode or Cxx_{16} or Dxx_{16} in 180 mode are sent to the display station as X Data Bits 55 through 63. These bits specify the horizontal X coordinate for the CRT beam. The displayable area of the CRT screen is divided into 512 horizontal lines. Each horizontal line has 512 dot positions. Each dot position is defined by its unique horizontal and vertical coordinates within the 512-by-512 matrix.
- The rightmost nine bits of words of $7xxx_8$ in 170 mode or Exx_{16} or Fxx_{16} in 180 mode are sent to the display station as Y Data Bits 55 through 63. These bits specify the vertical Y coordinate for the CRT beam.

Table 1-6. DSC Function Words

Function	Code		Description
	170 Mode (Octal)	180 Mode (Hex)	
Equipment select	7xxx	Exx	Connects the DSC to channel 10.
Screen select	70xx	E0x	Selects left display screen.
	71xx	E4x	Selects right display screen.
	74xx	F0x	Selects both screens.
DSC mode select	7x0x	E04	Selects character mode.
	7x1x	Ex8	Selects dot mode.
	7x2x	E14	Selects keyboard input mode.
Display character size select	7x00	E04	Selects small (64-characters per line) size.
	7x01	E05	Selects medium (32-characters per line) size.
	7x02	E06	Selects large (16-characters per line) size.

- Data words not conforming to either of the preceding conditions are interpreted as containing character codes. The left-half bits of such words form one character code and the right-half bits form another. The left-half character code is gated by the Character Code Select Mux and is presented to the ASCII-to-Display Code Converter. This converter changes ASCII codes to display codes during 180-mode operations. The original or converted code is then used to select the starting address in the Unblank and Beam Movement ROMs for that particular character. These ROMs contain the instructions for forming the selected character on the screen. These instructions, stepped through by the action of the Paint Character Count bits, cause the CRT beam to move from its starting point on through to the last formation point for the character. As this is being done, the beam is unblanked at each formation point to light a dot. The beam is then positioned at the starting point for the next character, and the process is repeated for the right-half code.

The formation of display characters in character mode is done within an 8-by-8 dot matrix for small size characters, a 16-by-16 dot matrix for medium size characters, and a 32-by-32 dot matrix for large characters. These various size characters are possible primarily due to the operation of the Beam Movement ROM circuits. These circuits generate the H (horizontal) and V (vertical) control signals defined in table 1-7.

Table 1-7. Horizontal and Vertical Control Signals

Signals				
H1	H2	V1	V2	Resulting Beam Movement
Active	Inactive	Inactive	Inactive	Horizontally one increment
Inactive	Active	Inactive	Inactive	Horizontally two increments
Active	Active	Inactive	Inactive	Reverses horizontal direction
Inactive	Inactive	Active	Inactive	Vertically one increment
Inactive	Inactive	Inactive	Active	Vertically two increments
Inactive	Inactive	Active	Active	Reverses vertical direction

Dot Mode

In dot mode, the DSC unblanks only defined dot positions on the CRT screen and does not respond to data words containing character codes. In dot mode, the DSC automatically unblanks the dot position after moving the CRT beam to a given X-and-Y coordinate. This mode is used for graphic displays.

Keyboard Input Mode

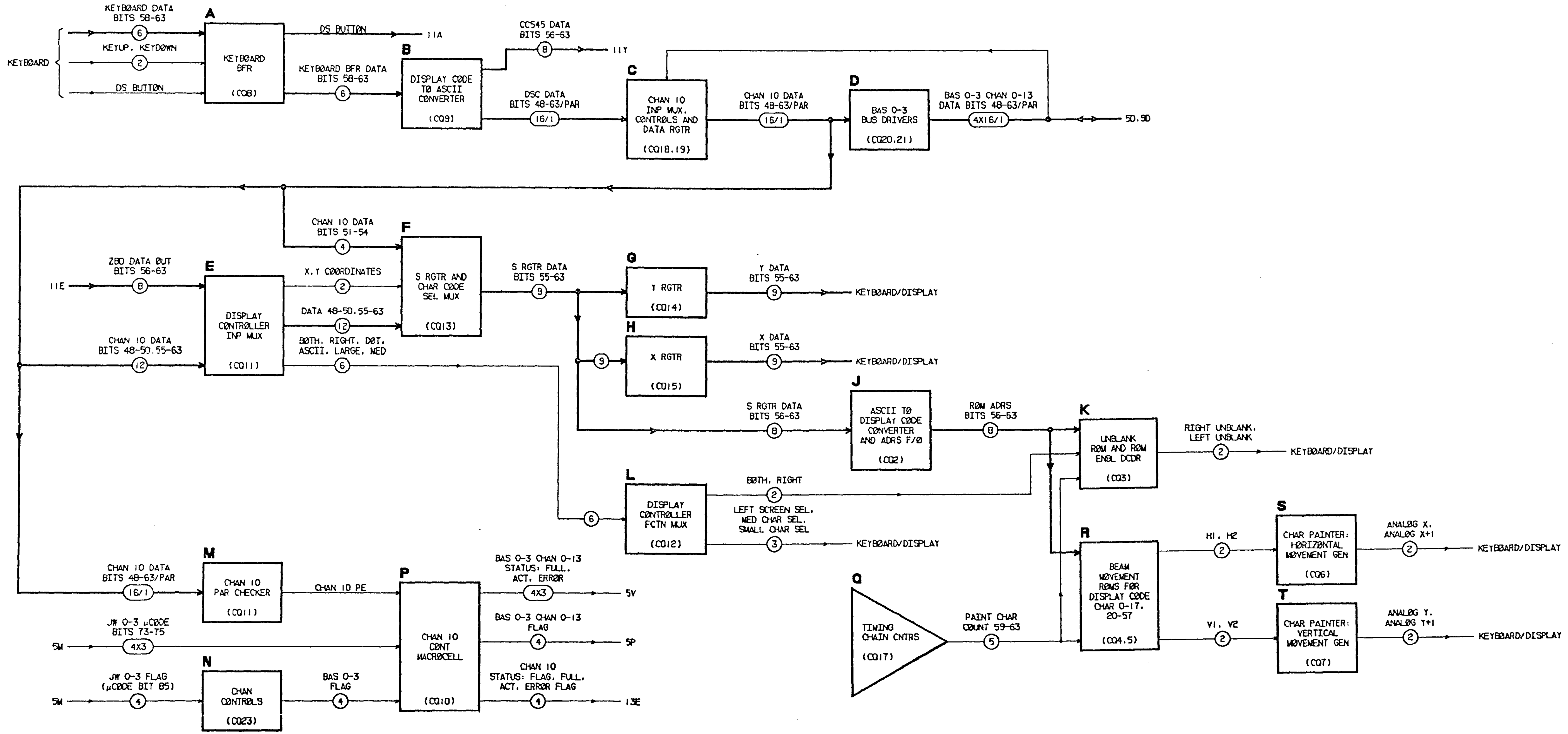
In keyboard input mode, the DSC inputs the keyboard data it is holding. The DSC holds the code from a pressed key (Keydown signal active) in its Keyboard Buffer. Placing the DSC in keyboard input mode then results in a Channel 10 Full indication to set and the keyboard data to be sent. Upon the completion of sending the keyboard data, the DSC clears the Channel 10 Full indication.

If operations are in 180 mode, the DSC converts the keyboard code to ASCII code before sending it in a word over channel 10. The left-half of the word sent contains zeros. This applies in either 170 or 180 mode.

OPERATIONS WITH TPM

DSC operations with the TPM are limited to character mode displays and keyboard input. Before either type operation, the TPM activates the Z80 Select CC545 signal to establish the data path between it and the DSC. The Z80 Select CC545 signal also disables communications from occurring with the DSC over channel 10 and sets up the DSC for generating a character mode display using small or medium size display characters. Medium size characters apply when the TPM activates the Z80 Medium Character Select signal. Character code data from the TPM is always ASCII encoded and, therefore, goes through the ASCII-to-Display Code Converter before being processed for display.

When the TPM is to input keyboard data, it activates the Z80 Select CC545 signal and the Keyboard Select signal. The Keyboard Select signal creates a fake keyboard buffer full condition within the DSC. This gates the contents from the Keyboard Buffer into the Display Code-to-ASCII Converter logic where it can be read by the TPM. The TPM determines whether a display station key was pressed by checking the data itself.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM
DISPLAY STATION CONTROL
NIB

60463540 C
IOU 1.12

This diagram shows MAC (JQ) board circuits and RI (HR/JR) board circuits. The MAC and radial interface (RI) are accessible to the BASs of either the NIO or CIO. This access is via channel 17. The TPM (1.11) also has access to the MAC.

MAC FUNCTIONS

The primary function of the IOU MAC is to transfer data between the IOU maintenance registers and the BASs or TPM. These I/O transfers allow the IOU software to monitor and set IOU operating conditions. In addition to the transferring that the MAC does, it assembles and disassembles the data bytes from and to the maintenance registers. The mode of data transfer for most IOU maintenance registers is bit serial transmission, because it saves backpanel space. For example, if a maintenance register exists on another board, a twisted pair of wires are used to transfer the eight bits of data serially from board to board rather than using parallel lines for data bits plus a parity bit. The required assembly/disassembly of maintenance register data is done by the Serial/Parallel Shifter Register and Pak Select circuits.

The MAC also performs IOU master clear, ADU master clear, and clear light-emitting diodes (LED) functions.

ERROR DETECTOR CIRCUIT

The Error Detector circuit summarizes the error detection for the MAC. Here, parity is checked on all data transfers to the MAC. In addition, monitoring is done for nanocode parity errors and channel 17 parity errors. Nanocode sequences the MAC during the transferring of maintenance register data.

FUNCTION WORD DECODING

The MAC responds to function words (figure 1-2) much the same as any channel device does. Organization of the function word is such that a 4-bit field in the function word includes the connect code. That field determines the particular RI with which communications takes place. The connect codes used are:

- Zero - connects channel 17 to the IOU MAC.
- One - connects channel 17 to either the MAC for system memory or CP-0.
- Three - connects channel 17 to the MAC of the CP-1.

Following the 4-bit connect code field is the 4-bit opcode field. That field determines the particular type of operation to be performed, such as clear LEDs, read, write, master clear, clear fault status registers, etc. When the function word contains a connect code other than 0, the IOU MAC passes the word to the appropriate RI. It is the responsibility of the connected system element that receives the data to process it in the order that is expected.

The third 4-bit field in the function word is the type code. It is an additional level of device selection used to obtain data or respond by sending data (based on the function requested). For example, a type code of 0 is used for the processor and a type code of an A is used to access the memory element. A type code of 0 also applies to the IOU MAC.

BITS	48 - - - 51	52 - - - 55	56 - - - 59	60 - - - 63
	NOT USED	CONNECT CODE	OPCODE	TYPE CODE

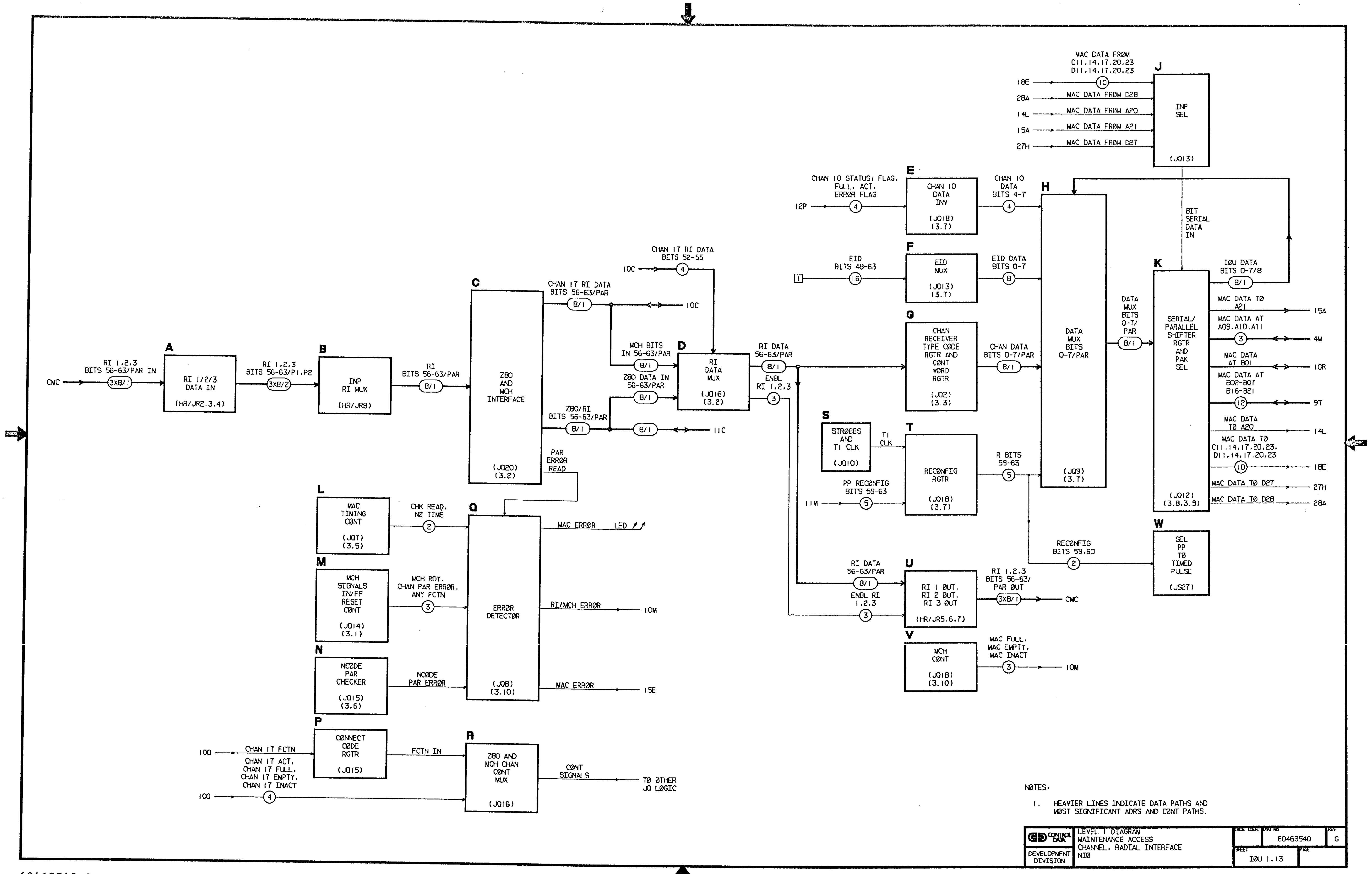
Figure 1-2. Function Word Format

SERIAL/PARALLEL SHIFTER REGISTER AND PAK SELECTOR

This MAC logic accesses the maintenance registers in the IOU. Maintenance registers are contained on the JS, JT, JC, and JL boards of the IOU. The maintenance register(s) to be accessed are specified by a BAS or the TPM after connecting to the IOU MAC. Data is then passed back and forth through the bit serial shifter, which selects the specific pack and enables the appropriate serial data line. Only one of these lines is enabled at any given time. The data transfer therefore takes place only between the register on the selected board and the MAC, whether the operation is a read or a write.

RI FUNCTIONS

RIs 1 through 3 provide access to the MAC units in other elements of the system. Communications with the selected element occurs in parallel transfers of eight data bits plus parity.


CMC
RI 1,2,3 BITS 56-63/PAR IN
3X8/1
A
RI 1/2/3 DATA IN (HR/JR2,3,4)
RI 1,2,3 BITS 56-63/P1,P2
3X8/2
B
INP RI MUX (HR/JR8)
RI BITS 56-63/PAR
8/1
C
Z80 AND MCH INTERFACE (JQ20) (3.2)
CHAN 17 RI DATA BITS 56-63/PAR
8/1
10C
CHAN 17 RI DATA BITS 52-55
4
10C
MCH BITS IN 56-63/PAR
8/1
Z80 DATA IN 56-63/PAR
8/1
Z80/RI BITS 56-63/PAR
8/1
8/1
11C
D
RI DATA MUX (JQ16) (3.2)
RI DATA 56-63/PAR
8/1
ENBL RI 1,2,3
3
PAR ERROR READ
L
MAC TIMING CONT (JQ7) (3.5)
CHK READ, N2 TIME
2
M
MCH SIGNALS IN/FF RESET CONT (JQ14) (3.1)
MCH RDY, CHAN PAR ERROR, ANY FCTN
3
N
NCODE PAR CHECKER (JQ15) (3.6)
NCODE PAR ERROR
Q
ERROR DETECTOR (JQ8) (3.10)
MAC ERROR
LED
RI/MCH ERROR
10M
MAC ERROR
15E
P
CONNECT CODE RGTR (JQ15)
10Q
CHAN 17 FCTN
CHAN 17 ACT, CHAN 17 FULL, CHAN 17 EMPTY, CHAN 17 INACT
10Q
4
FCTN IN
R
Z80 AND MCH CHAN CONT MUX (JQ16)
CONT SIGNALS
TO OTHER JQ LOGIC
CHAN 10 STATUS; FLAG, FULL, ACT, ERROR FLAG
12P
4
E
CHAN 10 DATA INV (JQ18) (3.7)
CHAN 10 DATA BITS 4-7
4
EID BITS 48-63
1
16
F
EID MUX (JQ13) (3.7)
EID DATA BITS 0-7
8
G
CHAN RECEIVER TYPE CODE RGTR AND CONT WORD RGTR (JQ2) (3.3)
CHAN DATA BITS 0-7/PAR
8/1
S
STROBES AND T1 CLK (JQ10)
T1 CLK
T
RECONFIG RGTR (JQ18) (3.7)
PP RECONFIG BITS 59-63
11M
5
R BITS 59-63
5
RI DATA 56-63/PAR
8/1
ENBL RI 1,2,3
3
U
RI 1 OUT, RI 2 OUT, RI 3 OUT (HR/JR5,6,7)
RI 1,2,3 BITS 56-63/PAR OUT
3X8/1
CMC
V
MCH CONT (JQ18) (3.10)
MAC FULL, MAC EMPTY, MAC INACT
3
10M
H
DATA MUX BITS 0-7/PAR (JQ9) (3.7)
DATA MUX BITS 0-7/PAR
8/1
RECONFIG BITS 59,60
2
W
SEL PP TO TIMED PULSE (JS27)
MAC DATA FROM C11,14,17,20,23 D11,14,17,20,23
18E
10
28A
MAC DATA FROM D28
14L
MAC DATA FROM A20
15A
MAC DATA FROM A21
27H
MAC DATA FROM D27
J
INP SEL (JQ13)
BIT SERIAL DATA IN
K
SERIAL/PARALLEL SHIFTER RGTR AND PAK SEL (JQ12) (3.8,3.9)
IOU DATA BITS 0-7/8
8/1
MAC DATA TO A21
15A
MAC DATA AT A09,A10,A11
3
4M
MAC DATA AT B01
10R
MAC DATA AT B02-B07 B16-B21
12
9T
MAC DATA TO A20
14L
MAC DATA TO C11,14,17,20,23, D11,14,17,20,23
10
18E
MAC DATA TO D27
27H
MAC DATA TO D28
28A

NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONT PATHS.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM
MAINTENANCE ACCESS
CHANNEL, RADIAL INTERFACE
NIO
60463540
G
IOU 1.13

The majority of the circuits shown on this diagram are maintenance register A (JS) board circuits. These JS board circuits assemble and mask fault status 1 information for the NIO. Another JS (1.27) board performs similar functions for the CIO.

NIO FAULT STATUS 1 INFORMATION

Bytes of NIO fault status 1 information are read/written serially by the MAC (1.13) through the MAC interface on line A20. Table 1-8 defines this information.

Table 1-8. NIO Fault Status 1 Information (Sheet 1 of 2)

Byte	Bits	Error Indication When Set
0	0-2	Not used
	3	BAS 0, PP4 error
	4	BAS 0, PP3 error
	5	BAS 0, PP2 error
	6	BAS 0, PP1 error
	7	BAS 0, PP0 error
1	8-10	Not used
	11	BAS 1, PP4 error
	12	BAS 1, PP3 error
	13	BAS 1, PP2 error
	14	BAS 1, PP1 error
	15	BAS 1, PP0 error
2	16-18	Not used
	19	BAS 2, PP4 error
	20	BAS 2, PP3 error
	21	BAS 2, PP2 error
	22	BAS 2, PP1 error
	23	BAS 2, PP0 error
3	24-26	Not used
	27	BAS 3, PP4 error
	28	BAS 3, PP3 error
	29	BAS 3, PP2 error
	30	BAS 3, PP1 error
	31	BAS 3, PP0 error
4	32	Error detected on JW board
	33	Error detected on KR board
	34	Error detected on JA board
	35	Error detected on KB board
	36	Error detected on JC board
	37	Error detected on JD board
	38	Error detected on JE board
	39	Error detected on JF board
5	40	SECDED error, BAS 0
	41	SECDED error, BAS 1
	42	SECDED error, BAS 2

Table 1-8. NIO Fault Status 1 Information (Sheet 2 of 2)

Byte	Bits	Error Indication When Set
	43	SECDED error, BAS 3
	44	12/16-conversion error
	45	OS bounds violation
	46	OS boundary address parity error
	47	Firmware error
6	48	Response code error
	49	Uncorrected CM read error
	50	Uncorrected CM write error
	51	CM reject
	52	Data-in error - CMI/ADU
	53	Tag-in error - CMI/ADU
	54	Data-out error - CMI/ADU
	55	Address/function error - CMI/ADU/BAS
7	56	Tag-out error - CMI/ADU
	57	CMI error - JJ board (A06)
	58	CMI error - JJ board (A07)
	59	CMI error - JG board (A08)
	60	CMI error - JH board (A02)
	61	CMI error - JH board (A03)
	62	CMI error - JH board (A04)
	63	CMI error - JH board (A05)

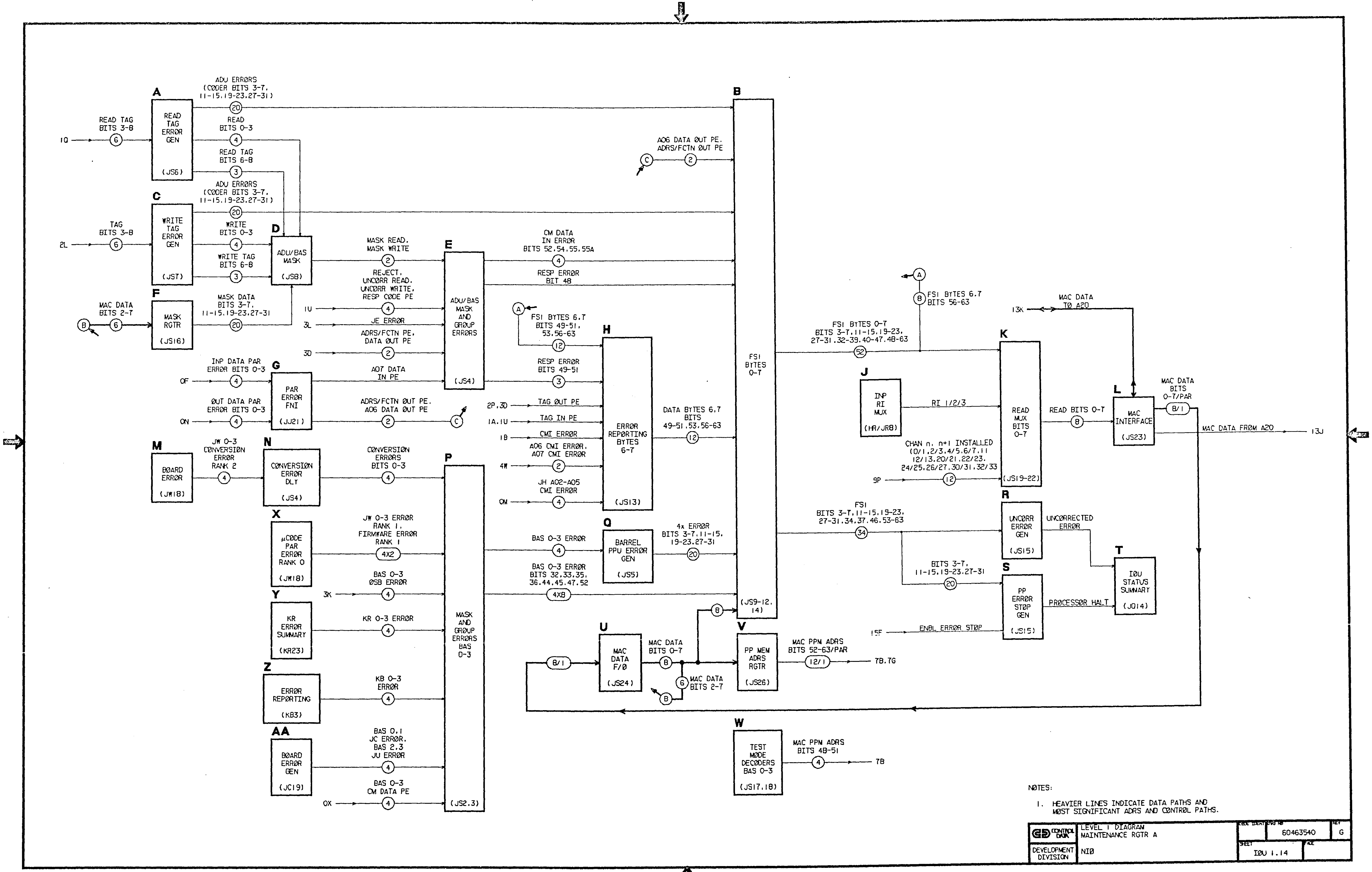
NIO STATUS SUMMARY INFORMATION

The MAC can also access NIO status summary information. This byte of information is assembled in the IOU Status Summary circuits. This information indicates:

- Summary status - Whether an error condition exists in the IOU or any other mainframe elements of the system.
- Processor halt - Whether a PP in the IOU is halted because of an error or is about to halt at the end of an instruction.
- Uncorrected error - Whether an uncorrected error occurred in the IOU.
- Corrected error - Whether a SECDED error condition occurred in the IOU.
- Physical environment monitor - Whether a long motor-generator warning is present.

ERROR MASKING

Error masking initiated by the software allows the reporting of certain IOU errors to be stopped. This allows the IOU to continue operations in a degraded mode, without the use of the BAS/ADU having the error. The error masking shown on this diagram is done in the fault status 1 information. This also masks the particular error from the status summary byte.


A
READ TAG ERROR GEN (JS6)
1Q
READ TAG BITS 3-8
6
ADU ERRORS (CODER BITS 3-7, 11-15,19-23,27-31)
20
READ BITS 0-3
4
READ TAG BITS 6-8
3
C
WRITE TAG ERROR GEN (JS7)
2L
TAG BITS 3-8
6
ADU ERRORS (CODER BITS 3-7, 11-15,19-23,27-31)
20
WRITE BITS 0-3
4
WRITE TAG BITS 6-8
3
D
ADU/BAS MASK (JS8)
F
MASK RGTR (JS16)
MAC DATA BITS 2-7
6
B
MASK DATA BITS 3-7, 11-15,19-23,27-31
20
MASK READ, MASK WRITE
2
E
ADU/BAS MASK AND GROUP ERRORS (JS4)
REJECT, UNCORR READ, UNCORR WRITE, RESP CODE PE
1U
4
3L
JE ERROR
ADRS/FCTN PE, DATA OUT PE
3D
2
G
PAR ERROR FNI (JJ21)
0F
INP DATA PAR ERROR BITS 0-3
4
A07 DATA IN PE
0N
OUT DATA PAR ERROR BITS 0-3
4
ADRS/FCTN OUT PE, A06 DATA OUT PE
2
C
M
BOARD ERROR (JW18)
JW 0-3 CONVERSION ERROR RANK 2
4
N
CONVERSION ERROR DLY (JS4)
CONVERSION ERRORS BITS 0-3
4
P
MASK AND GROUP ERRORS BAS 0-3 (JS2,3)
X
μCODE PAR ERROR RANK 0 (JW18)
JW 0-3 ERROR RANK 1, FIRMWARE ERROR RANK 1
4X2
BAS 0-3 OSB ERROR
3K
4
Y
KR ERROR SUMMARY (KR23)
KR 0-3 ERROR
4
Z
ERROR REPORTING (KB3)
KB 0-3 ERROR
4
AA
BOARD ERROR GEN (JC19)
BAS 0,1 JC ERROR, BAS 2,3 JU ERROR
4
BAS 0-3 CM DATA PE
0X
4
CM DATA IN ERROR BITS 52,54,55,55A
4
RESP ERROR BIT 48
A
FSI BYTES 6,7 BITS 49-51, 53,56-63
12
H
ERROR REPORTING BYTES 6-7 (JS13)
RESP ERROR BITS 49-51
3
2P,3D
TAG OUT PE
1A,1U
TAG IN PE
1B
CMI ERROR
4W
A06 CMI ERROR, A07 CMI ERROR
2
0M
JH A02-A05 CMI ERROR
4
Q
BARREL PPU ERROR GEN (JS5)
BAS 0-3 ERROR
4
BAS 0-3 ERROR BITS 32,33,35, 36,44,45,47,52
4X8
4x ERROR BITS 3-7,11-15, 19-23,27-31
20
DATA BYTES 6,7 BITS 49-51,53,56-63
12
C
A06 DATA OUT PE, ADRS/FCTN OUT PE
2
B
FSI BYTES 0-7 (JS9-12, 14)
U
MAC DATA F/0 (JS24)
8/1
MAC DATA BITS 0-7
8
8
MAC DATA BITS 2-7
6
B
V
PP MEM ADRS RGTR (JS26)
MAC PPM ADRS BITS 52-63/PAR
12/1
7B,7G
W
TEST MODE DECODERS BAS 0-3 (JS17,18)
MAC PPM ADRS BITS 48-51
4
7B
A
8
FSI BYTES 6,7 BITS 56-63
FSI BYTES 0-7 BITS 3-7,11-15,19-23, 27-31,32-39,40-47,48-63
52
J
INP RI MUX (HR/JR8)
RI 1/2/3
K
READ MUX BITS 0-7 (JS19-22)
CHAN n, n+1 INSTALLED (0/1,2/3,4/5,6/7,11 12/13,20/21,22/23, 24/25,26/27,30/31,32/33
9P
12
READ BITS 0-7
8
L
MAC INTERFACE (JS23)
13K
MAC DATA TO A20
MAC DATA BITS 0-7/PAR
8/1
MAC DATA FROM A20
13J
FSI BITS 3-7,11-15,19-23, 27-31,34,37,46,53-63
34
R
UNCORR ERROR GEN (JS15)
UNCORRECTED ERROR
BITS 3-7, 11-15,19-23,27-31
20
S
PP ERROR STOP GEN (JS15)
15F
ENBL ERROR STOP
PROCESSOR HALT
T
IOU STATUS SUMMARY (JO14)

NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM
MAINTENANCE RGTR A
NIO
60463540
G
IOU 1.14

MAINTENANCE REGISTER B (NIO) (IOU 1.15)

This diagram shows the maintenance register B (JT) board circuits for the NIO. These circuits assemble and mask fault status 2 information for the NIO and store its environment control (EC) bits. Another JT board (1.28) performs similar functions for the CIO.

NIO FAULT STATUS 2 INFORMATION

Bytes of NIO fault status 2 information are read/written serially by the MAC (1.13) through the MAC interface on line A21. This MAC interface also allows the MAC to write bytes into the Fault Status Mask Register when a NIO fault status 2 error indication is to be masked. The contents of the NIO fault status 2 information are listed in table 1-9.

Table 1-9. NIO Fault Status 2 Information (Sheet 1 of 2)

Byte	Bits	Error Indication When Set
0-3	0-31	Not used
4	32	Channel 7 error
	33	Channel 6 error
	34	Channel 5 error
	35	Channel 4 error
	36	Channel 3 error
	37	Channel 2 error
	38	Channel 1 error
	39	Channel 0 error
5	40	Channel 17 error
	41	Not used
	42	Channel 15 error
	43	Not used
	44	Channel 13 error
	45	Channel 12 error
	46	Channel 11 error
	47	Channel 10 error

Table 1-9. NIO Fault Status 2 Information (Sheet 2 of 2)

Byte	Bits	Error Indication When Set
6	48	Channel 27 error
	49	Channel 26 error
	50	Channel 25 error
	51	Channel 24 error
	52	Channel 23 error
	53	Channel 22 error
	54	Channel 21 error
	55	Channel 20 error
7	56	MAC error
	57	Not used
	58	Not used
	59	RI 1/2/3 error
	60	Channel 33 error
	61	Channel 32 error
	62	Channel 31 error
	63	Channel 30 error

NIO EC BITS

Line A21 also provides the MAC read/write path for EC bits for the NIO. These bits, which are generated by the software, specify deadstart, test, and clock parameters for the NIO. Table 1-10 defines these parameters.

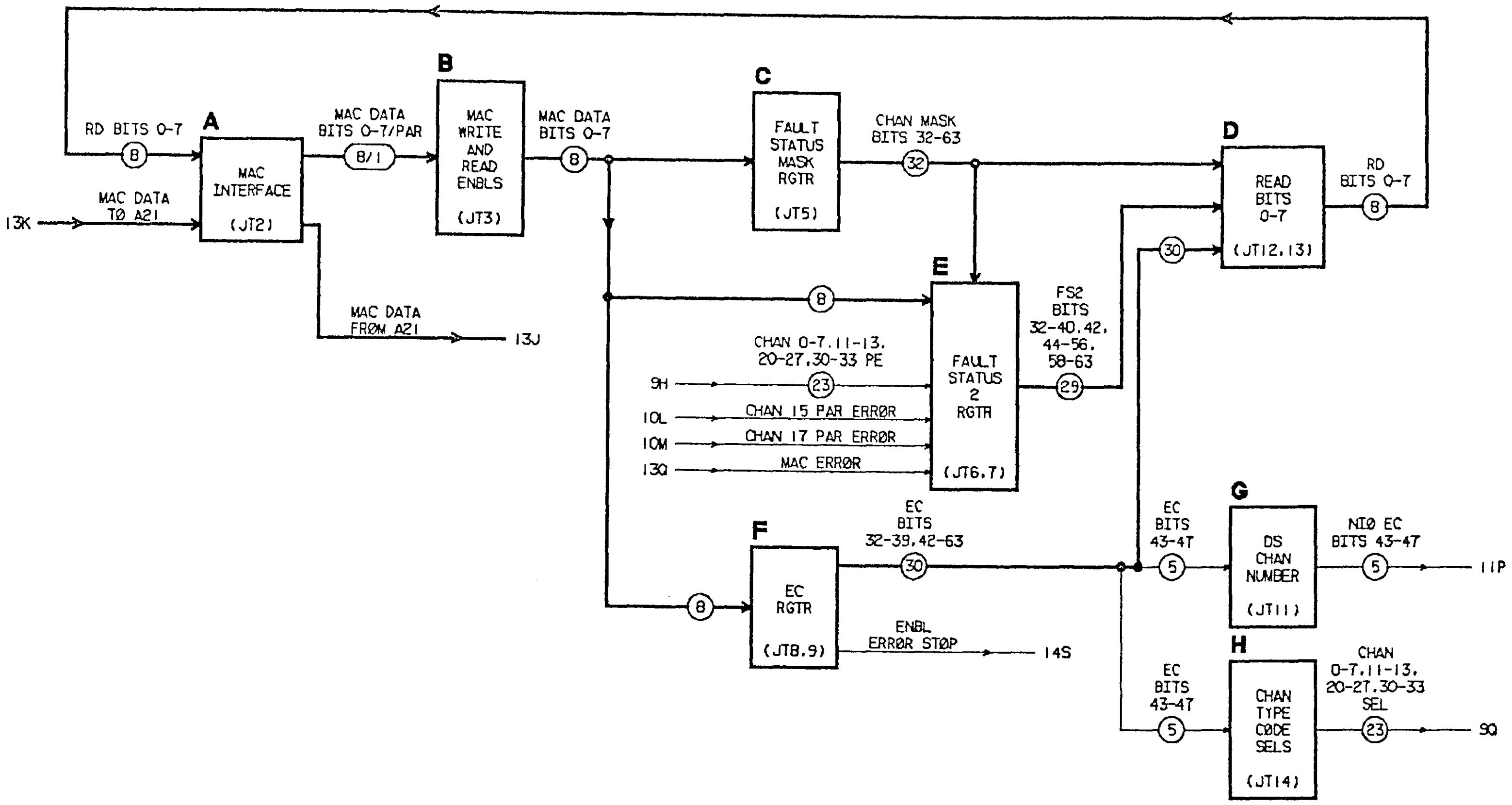
Table 1-10. NIO EC Bits (Sheet 1 of 2)

Byte	Bits	Parameter
0-3	0-31	Not used.
4	32	4K/8K PP memory - This bit is clear to select 4K PP memory operation except when diagnostics set it to select 8K PP memory operation.
	33	System initialized - This bit is cleared at power on and is set by software when the system has been initialized.
	34	Not used.
	35-39	PP number - These bits specify the logical number of the PP that is to do a load, dump, or idle operation during a deadstart (EC bit 58 set). When a deadstart is not being performed, these bits specify the PP that is to latch the contents of a selected register into a status register (EC bits 54 and 55 specify the selected register).†
5	40-42	Not used.
	43-47	Channel number - These bits specify the number of the channel over which a load or dump is to occur or which is to be master cleared via bit 62.
6	48-50	Not used.
	51	Load mode - This bit and bit 58 are set if the specified PP is to do a load during a deadstart.
	52	Dump mode - This bit and bit 58 are set if the specified PP is to do a dump during a deadstart.
	53	Idle mode - This bit and bit 58 are set if the specified PP is to go into idle mode during a deadstart.
	54,55	Register select - These bits specify the register (A, K, P, or Q) whose contents are to be latched into a status register.

†The status register referred to is not shown in the level 1 diagrams.

Table IOU 1-10. NIO EC Bits (Sheet 2 of 2)

Byte	Bits	Parameter
7	56	Wide clock select - When this bit is set, the 50-ns clock in the NIO is set to a pulse width of 11.5 ns.
	57	Narrow clock select - When this bit is set, the 50-ns clock in the NIO is set to a pulse width of 8.5 ns.
	58	Load/dump/idle enable - This bit sets during a deadstart to enable a load, dump, or idle to occur.
	59	Test mode enable - Enables the IOU parity checking circuits to be tested.
	60	OS bounds checking enable - When this bit is set, bounds violations are reported in the fault status 1 information and write or exchange requests to CM are blocked if a violation occurs.
	61	(R) + (A) to PP memory enable - When this bit is set, a store R-register (0025) instruction stores the result of the R+A adder instead of the R register (1.4). This applies to each BAS in the NIO. This feature allows the R+A adder to be tested without using CM.
	62	Individual channel master clear - When this bit is set, a master clear pulse is issued on the channel specified by bits 43 through 47.
	63	Error stop enable - When this bit is set, a PP in the NIO is halted if the PP has a recorded error.



NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM MAINTENANCE RGTR B	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	NIO	SHEET IOU 1.15		PAGE

This diagram through diagram 1.22 show the circuits of an ISI channel adapter. Each BAS in the CIO has five dedicated I/O channels, and each channel has an ISI channel adapter. An ISI channel adapter consists of a BASI (JX) board, a CIO channel (JY) board, and an ISI interface (JZ) board. This diagram shows JX board circuits. These circuits interact with the PPs of the associated BAS.

An adapter may be addressed by any PP of the associated BAS. An adapter is addressed via its I/O channel number. I/O channels 0 through 4 are dedicated to CIO BAS 0 and I/O channels 5_8 through 11_8 are dedicated to CIO BAS 1. Each adapter provides two ISI ports (A and B) for the connection of ISI peripheral devices. These ports are selectable through the PP issued function codes that control each adapter. Only one port of an adapter can be selected at a time.

ISI CHANNEL ADAPTER FUNCTIONS

An adapter operates in internal, PP, and DMA modes. An adapter enters internal mode when it performs an internal, interim operation. PP mode applies when a PP requests to communicate with an external ISI device. DMA mode applies when an adapter is performing a DMA transfer. With a DMA transfer, an adapter performs data transfers between the CMI and a peripheral controller without going through the associated BAS.

DMA transfers start by a PP issuing device control functions for the operation to the peripheral controller and issuing length/address pairs to the adapter. A length/address pair defines the word boundary and number of bytes to be accessed in CM. With this information, an adapter directs the data flow independently. However, the sectoring of data on disk media is controlled by a PP. If a length/pair exceeds sector boundaries, a PP issues multiple pairs that force the transfer to end at sector boundaries. In addition, a PP adds sector control words to the beginning of each sector written and verifies these words on each sector read.

BASI DATA FLOW

This data flow includes data coming from or going to a PP.

DATA FLOW FROM A PP

Data sent by a PP enters the adapter through the Channel Data Register. Copies of bits 52 through 55 and 63 of the PP data go to the Function Register for decoding when a PP issues a function code.

The data path from the Channel Data Register also leads to other registers in the adapter for loading. A PP may direct a load into the Control Registers, Flag Mask Register, or T Prime Register (1.18).

If the adapter is in PP mode, the data in the Channel Data Register goes through the Channel Data In and Out circuit to the Data Output Buffer (1.20). From there, the data goes into the Transmit Register and then to the Port A/B Transmitters for transmission to the external ISI unit selected by the PP. In PP mode, all data from a PP is transmitted to the selected ISI unit.

DATA FLOW TO A PP

A PP reads data from the adapter via the BAS Data In and Out circuit. The data requested by a PP via function code may be status or control information from a register within the adapter or data from an external ISI unit. In PP mode, all data that the adapter receives from the selected unit goes to the PP. The path this data takes is from the Port A/B Receivers (1.19) into the Input Data Mux. From there, the data goes to the Channel Data Register and then to the BAS Data In and Out circuit. When data reaches the Channel Data Register, a full indication is set to inform the PP that data is available.

Data originating from a register within the adapter also goes through the Input Data Mux, Channel Data Register, and BAS Data In and Out circuit. A PP may read the Control Registers, Flag Mask Register, T Register (1.21), Error Status Register (1.18), or Operational Status Register (1.17). When the adapter is in DMA mode, this read access allows a PP to monitor a DMA transfer and check for errors without interfering with the transfer.

FUNCTION DECODING

The Function Register and Function Decode PROMs decode the function codes received from a PP. Table 1-11 lists the codes and their functions.

Table 1-11. ISI Adapter Function Codes (Sheet 1 of 2)

Hex Code†	Function
x0x0	Master clear adapter.
x1x0	Read Control Registers.
x1x1	Write Control Registers.
x2x0	Read Flag Mask Register.
x2x1	Write Flag Mask Register.
x3x0	Read Error Status Register.
x4x0	Read Operational Status Register.
x5x0	Request ISI idle status (reads copy of ISI data bus).
x6x0	Read T Register.
x6x1	Write T Prime Register.
x7x0	Read test seed (initial test operand).
x7x1	Write test seed.
x8x0	Clear Select Hold signal (deselects previously selected ISI unit).
x8x1	Set Select Hold signal (begins select process on ISI port).
x9x0	Clear Command Sequence signal (places units on ISI port in idle mode).
x9x1	Set Command Sequence signal (removes units on ISI port from idle mode and places adapter in PP mode).
xAx0	Force Sync Out signal (requests a bit significant response on ISI port, or starts data transfer from selected unit and places adapter in PP mode).
xBx0	Set PP mode.††
xCx0	Clear DMA mode (inhibits any further adapter requests to CM).

† Any other hex codes are illegal. Hex codes are based on the 12 least significant bits of PP data with bits 48 through 51 and 56 through 62 disregarded.

†† If the adapter is in DMA mode when this function code is sent, the code stays in the Channel Data Register until the transfer in progress ends.

Table 1-11. ISI Adapter Function Codes (Sheet 2 of 2)

Hex Code†	Function
xCx1	Set DMA mode.
xDx0	Clear echo mode (echo mode is a test feature in adapter).
xDx1	Set echo mode (echos data within adapter).
xEx0	Clear T and T Prime Registers.

† Any other hex codes are illegal. Hex codes are based on the 12 least significant bits of PP data with bits 48 through 51 and 56 through 62 disregarded.

CONTROL REGISTERS

The Control Registers are accessed by a PP via function codes $x1x0_{16}$ and $x1x1_{16}$. The Control Registers hold bits that:

- Select either ISI port A or B for operations.
- Control whether a Cache Invalidate signal (1.21) is generated on every fourth and last CM write of a transfer
- Control whether an ISI 1-second timeout (1.19) is enabled or disabled.
- Enable test mode where an Operand Generator (1.19) simulates an external ISI unit.
- Control various test features of the adapter.

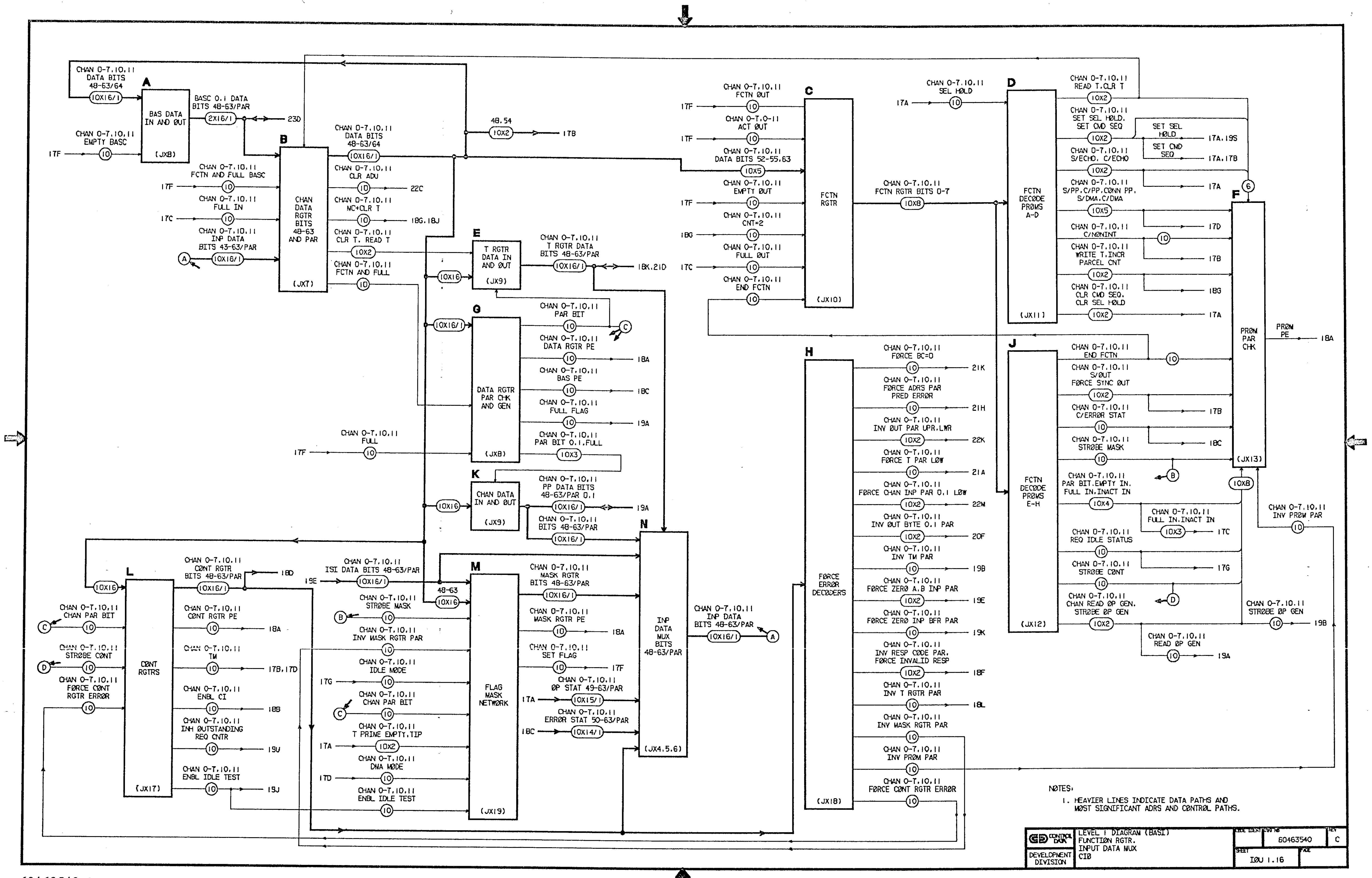
FORCE ERROR DECODERS

These decoders provide a means of testing the various parity checking networks in the adapter by forcing errors. When a PP enables such testing, error code bits that a PP loads into the Control Registers determine which errors are forced.

FLAG MASK NETWORK

This network contains the Flag Mask Register that is accessed by a PP via function codes $x2x0_{16}$ and $x2x1_{16}$. The Flag Mask Register sets a channel flag (1.17) when a condition specified by a PP occurs. The conditions that may be specified are:

- The completion of a DMA transfer.
- The T Prime Register being empty.
- The receipt of an Attention signal from a specified ISI unit during idle mode.


A
BAS DATA IN AND ØUT
(JX8)
CHAN 0-7,10,11 DATA BITS 48-63/64
10X16/1
BASC 0,1 DATA BITS 48-63/PAR
2X16/1
23D
CHAN 0-7,10,11 EMPTY BASC
17F
10
B
CHAN DATA RGTR BITS 48-63 AND PAR
(JX7)
CHAN 0-7,10,11 FCTN AND FULL BASC
CHAN 0-7,10,11 FULL IN
17C
CHAN 0-7,10,11 INP DATA BITS 43-63/PAR
10X16/1
CHAN 0-7,10,11 DATA BITS 48-63/64
CHAN 0-7,10,11 CLR ADU
22C
CHAN 0-7,10,11 MC+CLR T
18G,18J
CHAN 0-7,10,11 CLR T, READ T
10X2
CHAN 0-7,10,11 FCTN AND FULL
48,54
17B
E
T RGTR DATA IN AND ØUT
(JX9)
10X16
CHAN 0-7,10,11 T RGTR DATA BITS 48-63/PAR
18K,21D
G
DATA RGTR PAR CHK AND GEN
(JX8)
CHAN 0-7,10,11 PAR BIT
CHAN 0-7,10,11 DATA RGTR PE
18A
CHAN 0-7,10,11 BAS PE
18C
CHAN 0-7,10,11 FULL FLAG
19A
CHAN 0-7,10,11 PAR BIT 0,1,FULL
10X3
CHAN 0-7,10,11 FULL
K
CHAN DATA IN AND ØUT
(JX9)
CHAN 0-7,10,11 PP DATA BITS 48-63/PAR 0,1
CHAN 0-7,10,11 BITS 48-63/PAR
N
INP DATA MUX BITS 48-63/PAR
(JX4,5,6)
CHAN 0-7,10,11 INP DATA BITS 48-63/PAR
L
CØNT RGTRS
(JX17)
CHAN 0-7,10,11 CØNT RGTR BITS 48-63/PAR
18D
CHAN 0-7,10,11 CHAN PAR BIT
CHAN 0-7,10,11 CØNT RGTR PE
CHAN 0-7,10,11 STRØBE CØNT
CHAN 0-7,10,11 TM
17B,17D
CHAN 0-7,10,11 FØRCE CØNT RGTR ERRØR
CHAN 0-7,10,11 ENBL CI
18B
CHAN 0-7,10,11 INH ØUTSTANDING REQ CNTR
19U
CHAN 0-7,10,11 ENBL IDLE TEST
19J
M
FLAG MASK NETWØRK
(JX19)
19E
CHAN 0-7,10,11 ISI DATA BITS 48-63/PAR
48-63
CHAN 0-7,10,11 STRØBE MASK
CHAN 0-7,10,11 INV MASK RGTR PAR
CHAN 0-7,10,11 IDLE MØDE
17G
CHAN 0-7,10,11 CHAN PAR BIT
CHAN 0-7,10,11 T PRIME EMPTY,TIP
17A
CHAN 0-7,10,11 DMA MØDE
17D
CHAN 0-7,10,11 ENBL IDLE TEST
CHAN 0-7,10,11 MASK RGTR BITS 48-63/PAR
CHAN 0-7,10,11 MASK RGTR PE
CHAN 0-7,10,11 SET FLAG
17F
CHAN 0-7,10,11 ØP STAT 49-63/PAR
10X15/1
CHAN 0-7,10,11 ERRØR STAT 50-63/PAR
10X14/1
C
FCTN RGTR
(JX10)
CHAN 0-7,10,11 FCTN ØUT
CHAN 0-7,0-11 ACT ØUT
CHAN 0-7,10,11 DATA BITS 52-55,63
10X5
CHAN 0-7,10,11 EMPTY ØUT
CHAN 0-7,10,11 CNT=2
18G
CHAN 0-7,10,11 FULL ØUT
CHAN 0-7,10,11 END FCTN
CHAN 0-7,10,11 FCTN RGTR BITS 0-7
10X8
D
FCTN DECØDE PRØMS A-D
(JX11)
CHAN 0-7,10,11 SEL HØLD
CHAN 0-7,10,11 READ T,CLR T
CHAN 0-7,10,11 SET SEL HØLD, SET CMD SEQ
SET SEL HØLD
17A,19S
SET CMD SEQ
17A,17B
CHAN 0-7,10,11 S/ECHØ, C/ECHØ
CHAN 0-7,10,11 S/PP,C/PP,CØNN PP, S/DMA,C/DMA
CHAN 0-7,10,11 C/NØNINT
CHAN 0-7,10,11 WRITE T,INCR PARCEL CNT
CHAN 0-7,10,11 CLR CMD SEQ, CLR SEL HØLD
F
PRØM PAR CHK
(JX13)
PRØM PE
6
H
FØRCE ERRØR DECØDERS
(JX18)
CHAN 0-7,10,11 FØRCE BC=0
21K
CHAN 0-7,10,11 FØRCE ADRS PAR PRED ERRØR
21H
CHAN 0-7,10,11 INV ØUT PAR UPR,LWR
22K
CHAN 0-7,10,11 FØRCE T PAR LØW
21A
CHAN 0-7,10,11 FØRCE CHAN INP PAR 0,1 LØW
22M
CHAN 0-7,10,11 INV ØUT BYTE 0,1 PAR
20F
CHAN 0-7,10,11 INV TM PAR
19B
CHAN 0-7,10,11 FØRCE ZERØ A,B INP PAR
CHAN 0-7,10,11 FØRCE ZERØ INP BFR PAR
19K
CHAN 0-7,10,11 INV RESP CØDE PAR, FØRCE INVALID RESP
18F
CHAN 0-7,10,11 INV T RGTR PAR
18L
CHAN 0-7,10,11 INV MASK RGTR PAR
CHAN 0-7,10,11 INV PRØM PAR
CHAN 0-7,10,11 FØRCE CØNT RGTR ERRØR
J
FCTN DECØDE PRØMS E-H
(JX12)
CHAN 0-7,10,11 END FCTN
CHAN 0-7,10,11 S/ØUT FØRCE SYNC ØUT
CHAN 0-7,10,11 C/ERRØR STAT
CHAN 0-7,10,11 STRØBE MASK
CHAN 0-7,10,11 PAR BIT,EMPTY IN, FULL IN,INACT IN
10X4
CHAN 0-7,10,11 FULL IN,INACT IN
17C
CHAN 0-7,10,11 REQ IDLE STATUS
CHAN 0-7,10,11 STRØBE CØNT
CHAN 0-7,10,11 CHAN READ ØP GEN, STRØBE ØP GEN
CHAN 0-7,10,11 READ ØP GEN
CHAN 0-7,10,11 INV PRØM PAR
CHAN 0-7,10,11 STRØBE ØP GEN
10X8

NØTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM (BASI)
FUNCTIØN RGTR,
INPUT DATA MUX
CIØ
60463540
REV C
SHEET IØU 1.16

This is the second in the series of diagrams 1.16 through 1.22 that show portions of an ISI channel adapter. This diagram shows more JX board circuits.

OPERATIONAL STATUS NETWORK

The Operational Status Register in this network may be read by a PP via function code $x4x0_{16}$. This register provides the information that a PP needs to control the adapter. This information reflects whether:

- The Data Input Buffer (1.19) of the adapter is full. This condition only applies during diagnostic tests. At other times, the Outstanding Request Counter (1.19) of the adapter prevents more than 16 outstanding requests from being issued on an ISI port, thus preventing the possibility of buffer overflow.
- A Select Active signal is being received on the selected ISI port (external unit acknowledging being selected).
- The selected external ISI unit is sending a Pause signal (unit cannot temporarily perform issued function) or a Sync In signal (unit is acknowledging data receipt or is validating data being sent).
- The adapter is sending a Sync Out, Command Sequence, or a Select Hold signal on the selected ISI port.
- The adapter is in echo, PP, or DMA mode.
- Data is being sent from the selected ISI port (data flow from either a PP or DMA transfer to an external unit).
- Data transfers on the selected ISI port are occurring in interlocked mode (direct Sync Out and Sync In signal interchange between adapter and external unit) or in noninterlocked mode.
- The T Prime Register is empty or not.
- The adapter has issued a request to CM or from the selected ISI port and has not received a response back.

ADAPTER PP/DMA MODE REGISTERS

These registers determine when the adapter goes into PP or DMA mode. These registers place the adapter in PP mode when the Function Decode PROMs (1.16) decode one of the following function codes.

- $xBx0_{16}$ (Set PP mode).
- $x9x1_{16}$ (Set Command Sequence signal).
- $xAx0_{16}$ (Force Sync Out signal).
- $xDx1_{16}$ (Set echo mode).

Receipt of any function code other than the preceding clears PP mode.

The registers place the adapter in DMA mode when a $xCx1_{16}$ (Set DMA mode) function code is decoded. However, a PP must specify the guidelines for the DMA transfer before sending this function code. Otherwise, DMA mode does not go into effect until the ISI unit selected for the transfer returns a Sync In signal for the transfer function word. The transfer function word specifies the guidelines for the subsequent data transfer. The adapter relays this word to the selected unit after the unit select word. Both words originate from the PP.

ADAPTER INTERLOCK OUTPUT MODE REGISTERS

These registers set the output mode of the selected ISI port. The ISI ports operate in either interlock mode or noninterlock mode. These modes refer to the way the Sync Out and Sync In signal interchange occurs between the adapter and selected unit. In interlock mode, the adapter waits for a Sync In signal from the unit before transmitting another data word and the Strobe Out signal. This allows the unit to control the transfer rate.

In noninterlock mode, the adapter does not wait for the Strobe In signal from the unit before transmitting another word and the Strobe Out signal. In this mode, the adapter may transmit up to 16 words before stopping and waiting for a Strobe In signal. The adapter counts the Strobe Out and Strobe In signals separately to guard against overrun. Noninterlock mode is only supported in DMA transfers.

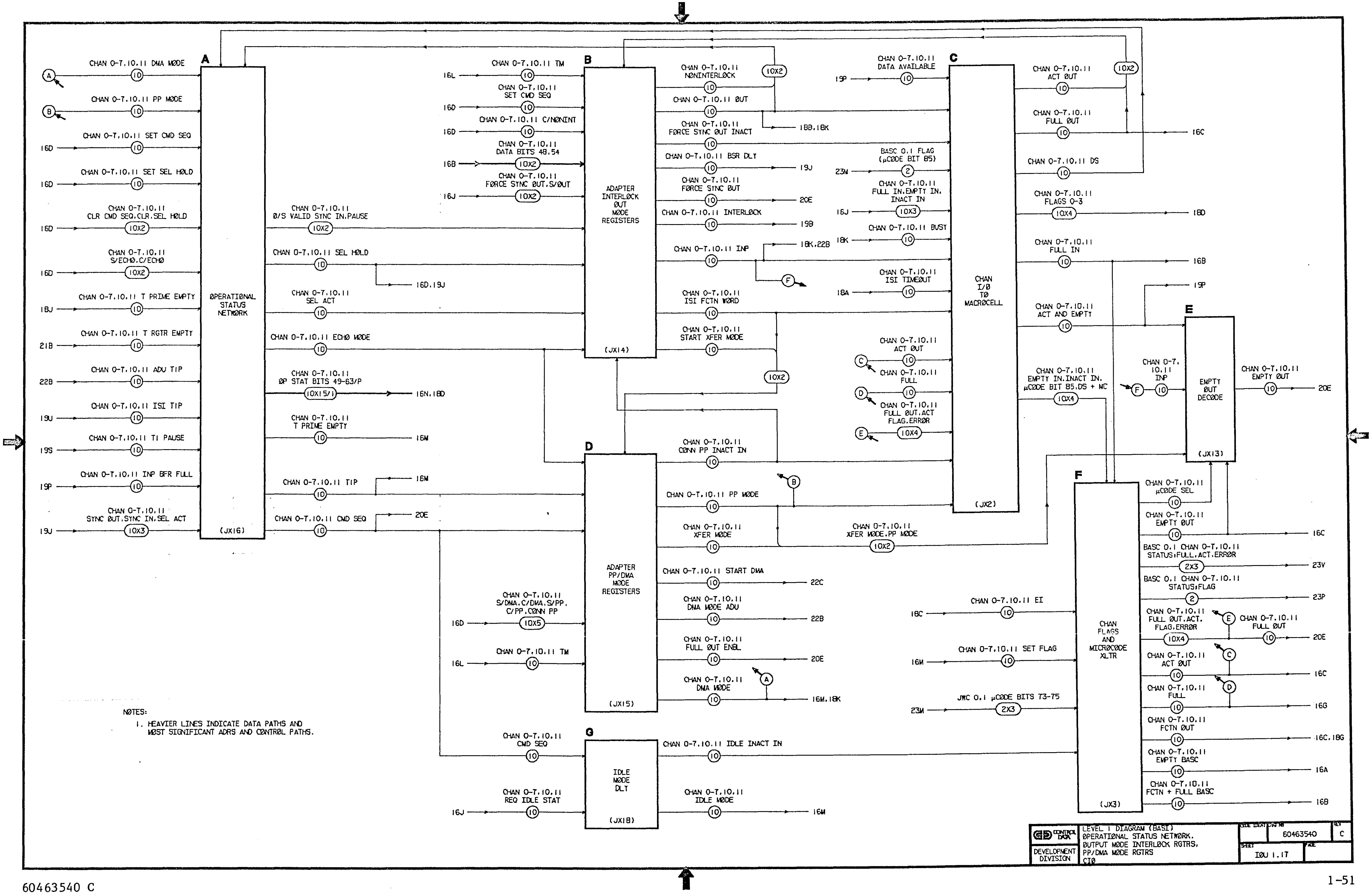
The unit-select and transfer-function words are transferred in interlock mode. The transfer-function word specifies the output mode for the data portion of the transfer.

After the transfer-function word has been sent, the Force Sync Out signal from the Adapter Interlock Output Mode Registers is activated to have the selected ISI unit input the first word if the direction of the transfer is to the adapter.

CHANNEL FLAGS AND MICROCODE TRANSLATOR

This circuit translates Microcode Bits 73 through 75 from a PP and outputs the channel flag for PP sampling. Microcode Bits 73 through 75 indicate when a PP is reading data from or writing data to the Channel Data Register (1.16). These bits also indicate whether the data written to the register is a function code that is to be decoded by the Function Decode PROMs (1.16).

The channel flag is used in various PP intructions to indicate the occurrence of a certain condition. A PP selects the condition to be monitored via the Flag Mask Network (1.16).



NØTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA	LEVEL I DIAGRAM (BASI) ØPERATIØNAL STATUS NETWØRK. ØUTPUT MØDE INTERLØCK RGTRS, PP/DMA MØDE RGTRS CIØ	DWG NO 60463540	REV C
DEVELOPMENT DIVISION		SHEET IØU 1.17	PAGE

This is the third in the series of diagrams 1.16 through 1.22 that show portions of an ISI channel adapter. This diagram shows more JX board circuits.

T PRIME REGISTER AND ASSOCIATED CIRCUITS

The T Prime Register temporarily holds the initial real-memory address and byte count for a DMA transfer before they are transferred to the T Register (1.21). This temporary storage allows DMA requests to be stacked and maintains a smooth data flow when scattered pages of CM are being accessed.

A PP loads the T Prime Register using function code $x6x1_{16}$. This load requires the input of three PP words (48 bits).

CM FUNCTION CODE AND CM RESPONSE CODE TRANSLATOR

The CM Function Code circuit generates the function code sent to CM via the CMI during DMA transfers. The CM Response Code Translator checks the returned CM response for errors.

ERROR STATUS NETWORK

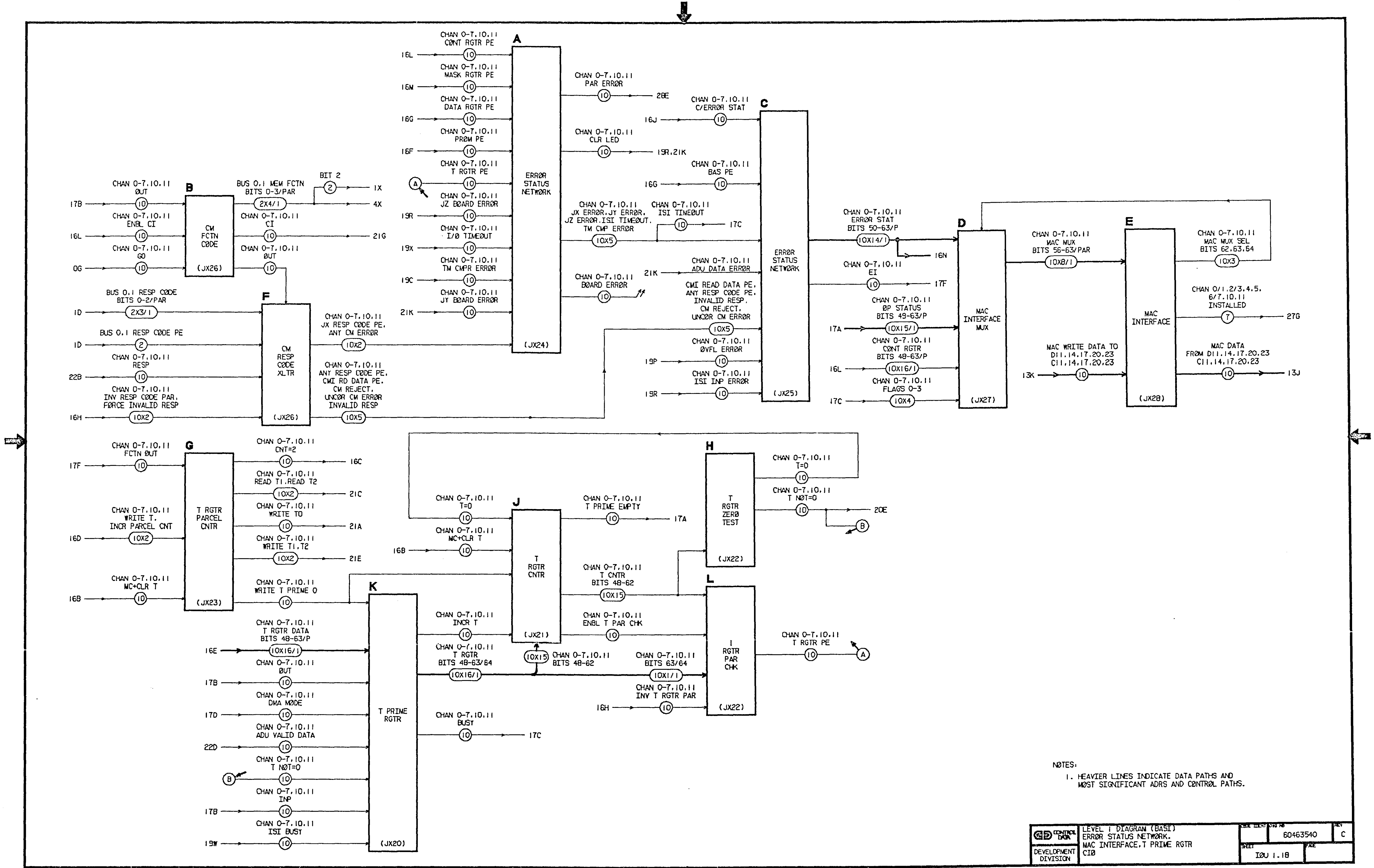
This network contains the Error Status Register that a PP reads via function code $x3x0_{16}$. A PP uses the error status to determine the validity of a transfer and whether a transfer should be redone. The PPs are responsible for logging uncorrected errors.

The error status indicates whether an overrun, timeout, test-mode compare error, parity error, or CM error occurred. A CM error is a CM reject or an invalid CM response during a DMA or an uncorrected CM error. A timeout error is a case where the adapter has sent a Sync Out to an external unit and not received a Sync In response within 1 second. An overflow error is when the adapter receives a Sync In after its Data Input Buffer (1.19) has become full. A test-mode compare error is when PP or DMA output data does not match the data generated by the Operand Generator (1.19) in test mode.

The Error Status Register automatically clears after being read.

MAC INTERFACE AND MUX

These circuits provide the IOU MAC (1.13) with access to the Error Status Register, Control Registers (1.16), and Operational Status Register (1.17) plus access to the channel flags (1.17). This access may be used during a short deadstart. A short deadstart terminates any data transfer being performed by the adapter but does not master clear its status or control registers. This allows the MAC unit to read the registers prior to a dump and restore them to the same state after a dump.


A
ERROR STATUS NETWORK
(JX24)
16L CHAN 0-7,10,11 CONT RGTR PE 10
16M CHAN 0-7,10,11 MASK RGTR PE 10
16G CHAN 0-7,10,11 DATA RGTR PE 10
16F CHAN 0-7,10,11 PROM PE 10
A CHAN 0-7,10,11 T RGTR PE 10
19R CHAN 0-7,10,11 JZ BOARD ERROR 10
19X CHAN 0-7,10,11 I/O TIMEOUT 10
19C CHAN 0-7,10,11 TM CMPR ERROR 10
21K CHAN 0-7,10,11 JY BOARD ERROR 10
CHAN 0-7,10,11 PAR ERROR 10 20E
CHAN 0-7,10,11 CLR LED 10 19R,21K
CHAN 0-7,10,11 JX ERROR,JY ERROR, JZ ERROR,ISI TIMEOUT, TM CMP ERROR 10X5
CHAN 0-7,10,11 ISI TIMEOUT 10 17C
CHAN 0-7,10,11 BOARD ERROR 10
B
CM FCTN CODE
(JX26)
17B CHAN 0-7,10,11 OUT 10
16L CHAN 0-7,10,11 ENBL CI 10
0G CHAN 0-7,10,11 GO 10
BUS 0,1 MEM FCTN BITS 0-3/PAR 2X4/1
BIT 2 2 1X
4X
CHAN 0-7,10,11 CI 10 21G
CHAN 0-7,10,11 OUT 10
F
CM RESP CODE XLTR
(JX26)
1D BUS 0,1 RESP CODE BITS 0-2/PAR 2X3/1
1D BUS 0,1 RESP CODE PE 2
22B CHAN 0-7,10,11 RESP 10
16H CHAN 0-7,10,11 INV RESP CODE PAR, FORCE INVALID RESP 10X2
CHAN 0-7,10,11 JX RESP CODE PE, ANY CM ERROR 10X2
CHAN 0-7,10,11 ANY RESP CODE PE, CMI RD DATA PE, CM REJECT, UNCOR CM ERROR INVALID RESP 10X5
C
ERROR STATUS NETWORK
(JX25)
16J CHAN 0-7,10,11 C/ERROR STAT 10
16G CHAN 0-7,10,11 BAS PE 10
21K CHAN 0-7,10,11 ADU DATA ERROR
CMI READ DATA PE, ANY RESP CODE PE, INVALID RESP, CM REJECT, UNCOR CM ERROR 10X5
19P CHAN 0-7,10,11 OVFL ERROR 10
19R CHAN 0-7,10,11 ISI INP ERROR 10
CHAN 0-7,10,11 ERROR STAT BITS 50-63/P 10X14/1 16N
CHAN 0-7,10,11 EI 10 17F
D
MAC INTERFACE MUX
(JX27)
17A CHAN 0-7,10,11 OP STATUS BITS 49-63/P 10X15/1
16L CHAN 0-7,10,11 CONT RGTR BITS 48-63/P 10X16/1
17C CHAN 0-7,10,11 FLAGS 0-3 10X4
CHAN 0-7,10,11 MAC MUX BITS 56-63/PAR 10X8/1
E
MAC INTERFACE
(JX28)
CHAN 0-7,10,11 MAC MUX SEL BITS 62,63,64 10X3
CHAN 0/1,2/3,4,5, 6/7,10,11 INSTALLED 7 27G
13K MAC WRITE DATA TO D11,14,17,20,23 C11,14,17,20,23 10
MAC DATA FROM D11,14,17,20,23 C11,14,17,20,23 10 13J
G
T RGTR PARCEL CNTR
(JX23)
17F CHAN 0-7,10,11 FCTN OUT 10
16D CHAN 0-7,10,11 WRITE T, INCR PARCEL CNT 10X2
16B CHAN 0-7,10,11 MC+CLR T 10
CHAN 0-7,10,11 CNT=2 10 16C
CHAN 0-7,10,11 READ T1,READ T2 10X2 21C
CHAN 0-7,10,11 WRITE T0 10 21A
CHAN 0-7,10,11 WRITE T1,T2 10X2 21E
CHAN 0-7,10,11 WRITE T PRIME 0 10
K
T PRIME RGTR
(JX20)
16E CHAN 0-7,10,11 T RGTR DATA BITS 48-63/P 10X16/1
17B CHAN 0-7,10,11 OUT 10
17D CHAN 0-7,10,11 DMA MODE 10
22D CHAN 0-7,10,11 ADU VALID DATA 10
B CHAN 0-7,10,11 T NOT=0 10
17B CHAN 0-7,10,11 INP 10
19W CHAN 0-7,10,11 ISI BUSY 10
CHAN 0-7,10,11 INCR T 10
CHAN 0-7,10,11 T RGTR BITS 48-63/64 10X16/1
CHAN 0-7,10,11 BUSY 10 17C
J
T RGTR CNTR
(JX21)
CHAN 0-7,10,11 T=0 10
16B CHAN 0-7,10,11 MC+CLR T 10
CHAN 0-7,10,11 T PRIME EMPTY 10 17A
CHAN 0-7,10,11 T CNTR BITS 48-62 10X15
CHAN 0-7,10,11 ENBL T PAR CHK 10
10X15 CHAN 0-7,10,11 BITS 48-62
CHAN 0-7,10,11 BITS 63/64 10X1/1
16H CHAN 0-7,10,11 INV T RGTR PAR 10
H
T RGTR ZERO TEST
(JX22)
CHAN 0-7,10,11 T=0 10
CHAN 0-7,10,11 T NOT=0 10 20E
B
L
T RGTR PAR CHK
(JX22)
CHAN 0-7,10,11 T RGTR PE 10 A

NOTES:
1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL I DIAGRAM (BASI) ERROR STATUS NETWORK. MAC INTERFACE,T PRIME RGTR CI0	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION		SHEET I0U 1.18	PAGE	

EXTERNAL INTERFACE (CIO) (IOU 1.19)

This is the fourth in the series of diagrams 1.16 through 1.22 that show portions of an ISI channel adapter. This diagram shows ISI interface (JZ) board circuits that interact with the external ISI peripheral devices.

PORT A/B DATA INPUT

Data input from port A or B goes from the Ports A and B Receivers through the Port Fan In Input Mux and to either the Input Data Mux (1.16) or the Data Input Buffer. The path to the Data Input Buffer applies when the selected port is in transaction mode. In transaction mode, the Command Sequence signal of the ports is set and data transfers occur bidirectionally between the selected unit and the adapter. During these transfers, the data lines of the external ISI bus connected to the port may carry function words, status information, or data as directed by a PP. All incoming information from the selected unit goes to the Data Input Buffer while in this mode.

When a port is not in transaction mode, it is in idle mode (Command Sequence signal clear). In idle mode, all slave units on the ISI bus of the port continuously transmit the state of their Attention and Busy signals on assigned bus data lines. The data line assignments for this are based on the bus unit addresses of the units (figure 1-3).

When in idle mode, the Attention and Busy status information from the ISI bus of the selected port goes directly to the Input Data Mux. From there the information goes into the Channel Data Register (1.16) when a function code $x5x0_{16}$ is received (request of ISI idle status). This allows a PP to read the information.

	BUSY BITS								ATTENTION BITS							
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	BUS UNIT ADDRESS								BUS UNIT ADDRESS							

Figure 1-3. Idle Mode Bus Busy/Attention Bit Format

DATA INPUT BUFFER

The Data Input Buffer provides storage for up to 16 words from the selected unit during either PP- or DMA-mode transfers. The input buffer also aligns the received words with the internal 50-nanosecond clock of the adapter. The Input Buffer Word Counter monitors the buffer for full or empty conditions. Due to the operation of the Outstanding Request Counter, an input buffer condition can only apply during diagnostic testing.

Words from the input buffer are checked for parity and routed through the Input Data Fan In circuits. If a DMA-mode input is in progress, the words then go to the DMA Input Data Buffer before going to the JY board circuits (1.22) for assembly. If a PP-mode input is in progress, the words go instead to the PP Input Data Mux and then to the Input Data Mux (1.16).

VALID SYNC IN CIRCUITS

These circuits include the Sync In One-Shot, Sync In Resync, and Valid Sync In Formation. These circuits ensure the validity of a Sync In signal from the selected unit and form the signal into a pulse that is aligned with the adapter's internal 50-nanosecond clock.

OUTSTANDING REQUEST COUNTER

This counter ensures that the Data Input Buffer does not overflow during adapter input and no more than 16 words are sent to the selected unit without a Sync In reply during adapter output. This latter condition applies to DMA-mode transfer sent in noninterlock mode.

ISI ONE-SECOND TIMEOUT CIRCUIT

This circuit sets a timeout error status bit (1.18) when the adapter has sent a Sync Out to the selected unit and did not receive a Sync In reply within 1 second. However, this timeout is disabled by a bit in the Control Registers (1.16) in instances where no Sync In reply is expected.

ISI BUSY CIRCUIT

This circuit monitors for ISI busy conditions, which are a full Data Output Buffer (1.20) or a maximum count in the Outstanding Request Counter. When either of these conditions occur, the ISI Busy circuit disables the transfer in progress until no ISI busy condition exists.

JZ BOARD ERROR CIRCUIT

This circuit sets a JZ Board Error bit in the Error Status Register (1.18) when one of the following conditions occur.

- An input buffer parity error.
- An ISI input data parity error.
- Input buffer overflow.
- An output buffer parity error.

TEST FEATURES

The major test features of the adapter are the Operand Generator and the Compare Network. Other test features appearing on diagram 1.19 are the Transmitter/Receiver Echo and the Inhibit Outstanding Request Counter bit.

OPERAND GENERATOR AND COMPARE NETWORK

These circuits go into operation when the adapter is in that test mode [Enable Test Mode bit set in Control Registers (1.16)]. In test mode, the receivers and transmitters on the selected port are disabled and the Operand Generator simulates external unit I/O.

The Operand Generator is an 8-bit counter that may be preloaded by a PP via function code $x7x1_{16}$ or read via function code $x7x0_{16}$. The Operand Generator increments by 1 for each I/O transfer during test mode, and the output of the generator is duplicated to form a 16-bit word. However, an Inhibit Test Mode Increment bit may be set in the Control Registers to inhibit this incrementing to allow the constant use of a preloaded bit pattern.

During test mode, the Operand Generator provides the:

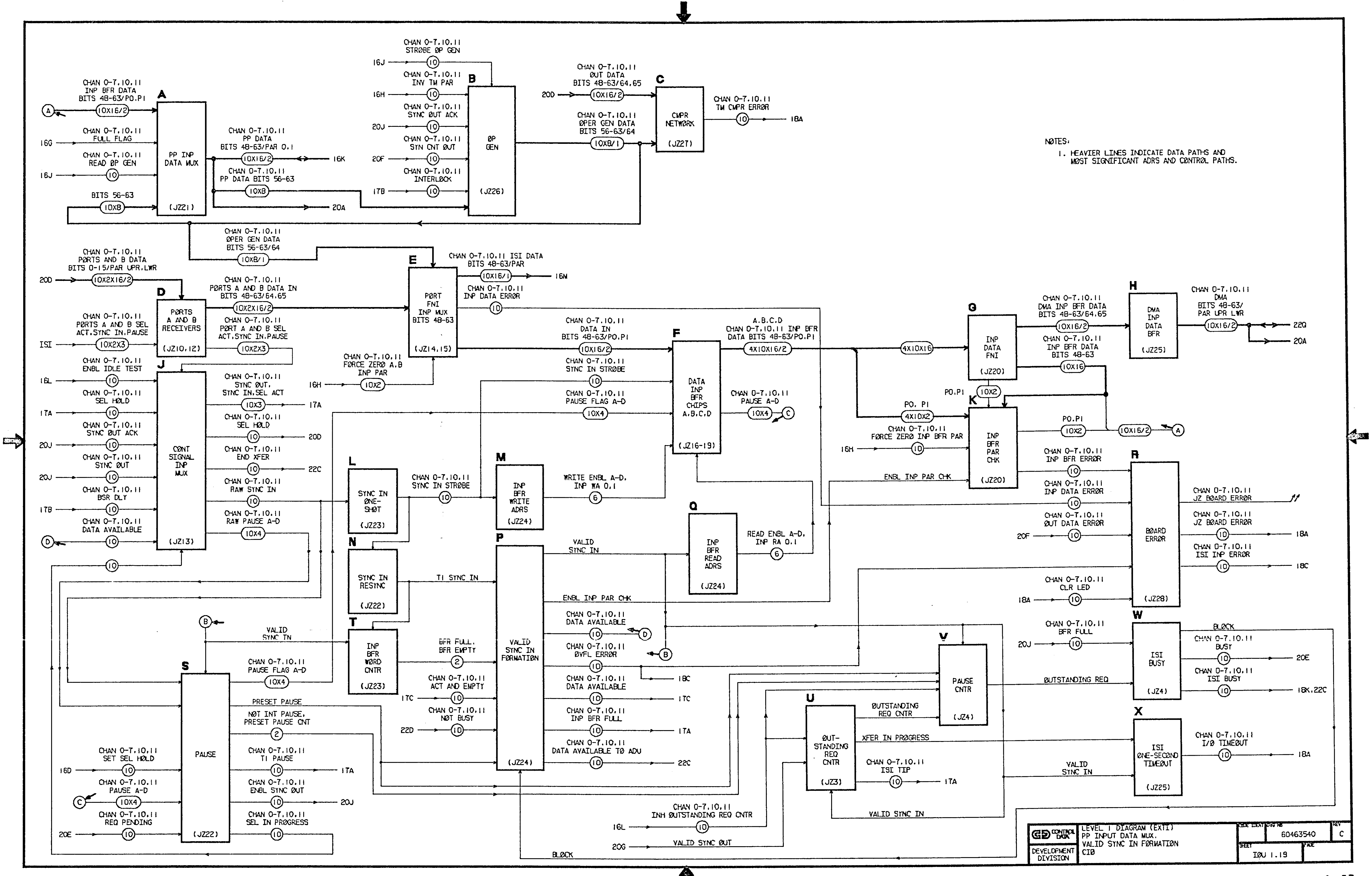
- Data for PP or DMA input until the DMA transfer completes or PP terminates the input.
- Data that the Compare Network compares against the PP or DMA output data. If the data does not compare, the Compare Network sets a Test Mode Compare Error bit in the Error Status Register (1.18).

TRANSMITTER/RECEIVER ECHO

The echo mode of the adapter complements test mode, because it can be used by diagnostic tests to check the receivers and transmitters of the selected port. Echo mode is set through function code $xDx1_{16}$. Echo mode enables data to flow from the Data Output Buffer through the transmitters (1.20) to the receivers (Ports A/B Data Bits 0 through 15 and parity) and into the Data Input Buffer.

INHIBIT OUTSTANDING REQUEST COUNTER BIT

This feature is used in conjunction with echo mode. When this bit is set in the Control Registers, the Outstanding Request Counter is inhibited from counting if the adapter is in echo mode. This inhibiting of counting allows diagnostic tests to purposely overflow the Data Input Buffer to ensure that an Input Buffer Overflow bit sets in the Error Status Register.


A
PP INP DATA MUX (JZ21)
CHAN 0-7,10,11 INP BFR DATA BITS 48-63/P0,P1
10X16/2
16G
CHAN 0-7,10,11 FULL FLAG
16J
CHAN 0-7,10,11 READ ØP GEN
10
BITS 56-63
10X8
CHAN 0-7,10,11 PP DATA BITS 48-63/PAR 0,1
10X16/2
16K
CHAN 0-7,10,11 PP DATA BITS 56-63
10X8
20A
B
ØP GEN (JZ26)
CHAN 0-7,10,11 STRØBE ØP GEN
16J
CHAN 0-7,10,11 INV TM PAR
16H
CHAN 0-7,10,11 SYNC ØUT ACK
20J
CHAN 0-7,10,11 STN CNT ØUT
20F
CHAN 0-7,10,11 INTERLØCK
17B
C
CMPR NETWØRK (JZ27)
20D
CHAN 0-7,10,11 ØUT DATA BITS 48-63/64,65
10X16/2
CHAN 0-7,10,11 ØPER GEN DATA BITS 56-63/64
10X8/1
CHAN 0-7,10,11 TM CMPR ERRØR
18A
CHAN 0-7,10,11 ØPER GEN DATA BITS 56-63/64
10X8/1
E
PØRT FNI INP MUX BITS 48-63 (JZ14,15)
CHAN 0-7,10,11 ISI DATA BITS 48-63/PAR
10X16/1
16N
CHAN 0-7,10,11 INP DATA ERRØR
CHAN 0-7,10,11 PØRTS AND B DATA BITS 0-15/PAR UPR,LWR
20D
10X2X16/2
D
PØRTS A AND B RECEIVERS (JZ10,12)
CHAN 0-7,10,11 PØRTS A AND B DATA IN BITS 48-63/64,65
10X2X16/2
CHAN 0-7,10,11 PØRTS A AND B SEL ACT,SYNC IN,PAUSE
ISI
10X2X3
CHAN 0-7,10,11 PØRT A AND B SEL ACT,SYNC IN,PAUSE
10X2X3
CHAN 0-7,10,11 FØRCE ZERØ A,B INP PAR
16H
10X2
J
CØNT SIGNAL INP MUX (JZ13)
CHAN 0-7,10,11 ENBL IDLE TEST
16L
CHAN 0-7,10,11 SEL HØLD
17A
CHAN 0-7,10,11 SYNC ØUT ACK
20J
CHAN 0-7,10,11 SYNC ØUT
20J
CHAN 0-7,10,11 BSR DLY
17B
CHAN 0-7,10,11 DATA AVAILABLE
D
CHAN 0-7,10,11 SYNC ØUT, SYNC IN,SEL ACT
10X3
17A
CHAN 0-7,10,11 SEL HØLD
20D
CHAN 0-7,10,11 END XFER
22C
CHAN 0-7,10,11 RAW SYNC IN
CHAN 0-7,10,11 RAW PAUSE A-D
10X4
F
DATA INP BFR CHIPS A,B,C,D (JZ16-19)
CHAN 0-7,10,11 DATA IN BITS 48-63/P0,P1
10X16/2
CHAN 0-7,10,11 SYNC IN STRØBE
CHAN 0-7,10,11 PAUSE FLAG A-D
10X4
A,B,C,D CHAN 0-7,10,11 INP BFR DATA BITS 48-63/P0,P1
4X10X16/2
CHAN 0-7,10,11 PAUSE A-D
10X4
C
G
INP DATA FNI (JZ20)
4X10X16
H
DMA INP DATA BFR (JZ25)
CHAN 0-7,10,11 DMA INP BFR DATA BITS 48-63/64,65
10X16/2
CHAN 0-7,10,11 INP BFR DATA BITS 48-63
10X16
CHAN 0-7,10,11 DMA BITS 48-63/PAR UPR LWR
10X16/2
22Q
20A
P0,P1
10X2
K
INP BFR PAR CHK (JZ20)
P0, P1
4X10X2
CHAN 0-7,10,11 FØRCE ZERØ INP BFR PAR
16H
ENBL INP PAR CHK
P0,P1
10X2
10X16/2
A
L
SYNC IN ØNE-SHØT (JZ23)
CHAN 0-7,10,11 SYNC IN STRØBE
M
INP BFR WRITE ADRS (JZ24)
WRITE ENBL A-D, INP WA 0,1
6
Q
INP BFR READ ADRS (JZ24)
READ ENBL A-D, INP RA 0,1
VALID SYNC IN
N
SYNC IN RESYNC (JZ22)
T1 SYNC IN
P
VALID SYNC IN FØRMATIØN (JZ24)
ENBL INP PAR CHK
CHAN 0-7,10,11 DATA AVAILABLE
D
CHAN 0-7,10,11 ØVFL ERRØR
B
18C
CHAN 0-7,10,11 DATA AVAILABLE
17C
CHAN 0-7,10,11 INP BFR FULL
17A
CHAN 0-7,10,11 DATA AVAILABLE TØ ADU
22C
T
INP BFR WØRD CNTR (JZ23)
BFR FULL, BFR EMPTY
2
CHAN 0-7,10,11 ACT AND EMPTY
17C
CHAN 0-7,10,11 NØT BUSY
22D
S
PAUSE (JZ22)
B
VALID SYNC IN
CHAN 0-7,10,11 PAUSE FLAG A-D
10X4
PRESET PAUSE
NØT INT PAUSE, PRESET PAUSE CNT
CHAN 0-7,10,11 SET SEL HØLD
16D
CHAN 0-7,10,11 PAUSE A-D
C
10X4
CHAN 0-7,10,11 REQ PENDING
20E
CHAN 0-7,10,11 T1 PAUSE
17A
CHAN 0-7,10,11 ENBL SYNC ØUT
20J
CHAN 0-7,10,11 SEL IN PRØGRESS
R
BØARD ERRØR (JZ28)
CHAN 0-7,10,11 INP BFR ERRØR
CHAN 0-7,10,11 INP DATA ERRØR
CHAN 0-7,10,11 ØUT DATA ERRØR
20F
CHAN 0-7,10,11 CLR LED
18A
CHAN 0-7,10,11 JZ BØARD ERRØR
CHAN 0-7,10,11 JZ BØARD ERRØR
18A
CHAN 0-7,10,11 ISI INP ERRØR
18C
W
ISI BUSY (JZ4)
CHAN 0-7,10,11 BFR FULL
20J
BLØCK
CHAN 0-7,10,11 BUSY
20E
CHAN 0-7,10,11 ISI BUSY
18K,22C
V
PAUSE CNTR (JZ4)
ØUTSTANDING REQ
U
ØUT-STANDING REQ CNTR (JZ3)
ØUTSTANDING REQ CNTR
XFER IN PRØGRESS
CHAN 0-7,10,11 ISI TIP
17A
VALID SYNC IN
X
ISI ØNE-SECØND TIMEØUT (JZ25)
VALID SYNC IN
CHAN 0-7,10,11 I/Ø TIMEØUT
18A
CHAN 0-7,10,11 INH ØUTSTANDING REQ CNTR
16L
VALID SYNC ØUT
20G
BLØCK

NØTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MØST SIGNIFICANT ADRS AND CØNTRØL PATHS.

CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (EXT1)
PP INPUT DATA MUX.
VALID SYNC IN FØRMATIØN
CIØ

CODE IDENT	DWG NO	REV
	60463540	C

SHEET	PAGE
IØU 1.19	

This is the fifth in the series of diagrams 1.16 through 1.22 that show portions of an ISI channel adapter. This diagram shows more JZ board circuits.

PORT A/B DATA OUTPUT

The PP or DMA data to be transmitted from port A or B is gated through the Output Buffer Data Mux and into the Data Output Buffer. From there, the data goes into the Transmit Register before it is sent from the selected port by the Port A/B Transmitters. The words sent out may either be data or function words from the PP. Which type being sent is indicated by the Command Sequence signal.

The Data Output Buffer can store up to four words. The output buffer also aligns the words with the external 166-nanosecond clock. Words entering the buffer are in line with the internal 50-nanosecond clock.

PORT A/B CONTROL SIGNAL OUTPUT

The control signals transmitted from port A and B are the:

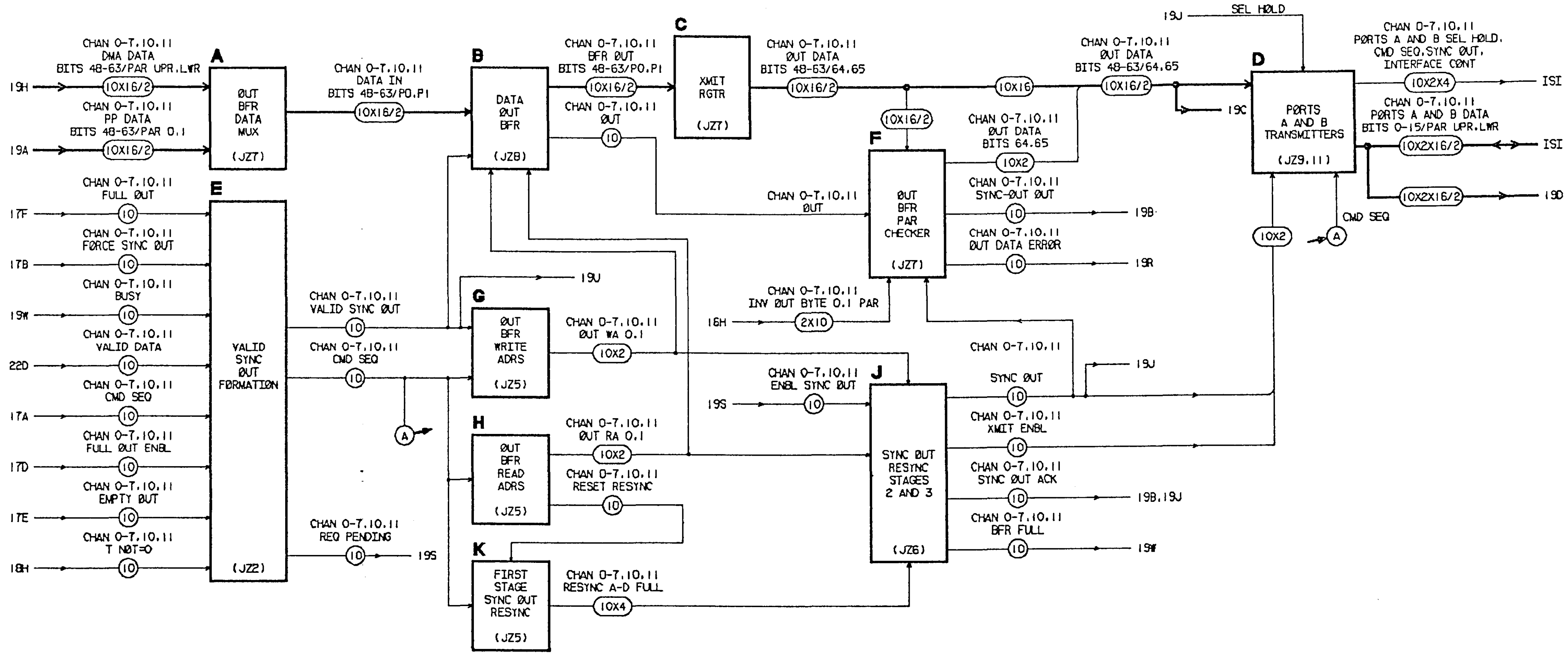
- Command Sequence signal - Goes active at the beginning of each transfer to switch the external bus of the selected port from idle mode to transaction mode and remains active during the unit selection sequence. The Command Sequence signal is also sent to a selected unit when the adapter is transferring a function word.

- Select Hold signal - Is active throughout each transfer on the selected port. The Select Hold signal going active informs the external units on the port bus that either a broadcast master reset or unit selection sequence is to occur next over the data lines. The Select Hold signal going inactive deselects the previously selected unit and places the port bus in idle mode.

- Sync Out signal - Accompanies each word sent from the selected port by the adapter or, if the flow is the opposite direction, signals that the adapter is ready to receive a word.

SYNC OUT RESYNC CIRCUITS

The three stages of the Sync Out Resync circuits generate the Sync Out signal for the selected port. These circuits align the Sync Out signal with the external 166-nanosecond clock.


A
OUT BFR DATA MUX (JZ7)
B
DATA OUT BFR (JZ8)
C
XMIT RGTR (JZ7)
D
PORTS A AND B TRANSMITTERS (JZ9,11)
E
VALID SYNC OUT FORMATION (JZ2)
F
OUT BFR PAR CHECKER (JZ7)
G
OUT BFR WRITE ADRS (JZ5)
H
OUT BFR READ ADRS (JZ5)
J
SYNC OUT RESYNC STAGES 2 AND 3 (JZ6)
K
FIRST STAGE SYNC OUT RESYNC (JZ5)
19H
CHAN 0-7,10,11 DMA DATA BITS 48-63/PAR UPR,LWR
10X16/2
19A
CHAN 0-7,10,11 PP DATA BITS 48-63/PAR 0,1
10X16/2
17F
CHAN 0-7,10,11 FULL OUT
10
17B
CHAN 0-7,10,11 FORCE SYNC OUT
10
19W
CHAN 0-7,10,11 BUSY
10
22D
CHAN 0-7,10,11 VALID DATA
10
17A
CHAN 0-7,10,11 CMD SEQ
10
17D
CHAN 0-7,10,11 FULL OUT ENBL
10
17E
CHAN 0-7,10,11 EMPTY OUT
10
18H
CHAN 0-7,10,11 T NOT=0
10
CHAN 0-7,10,11 DATA IN BITS 48-63/P0,P1
10X16/2
CHAN 0-7,10,11 VALID SYNC OUT
10
CHAN 0-7,10,11 CMD SEQ
10
A
CHAN 0-7,10,11 REQ PENDING
10
19S
19U
CHAN 0-7,10,11 BFR OUT BITS 48-63/P0,P1
10X16/2
CHAN 0-7,10,11 OUT
10
CHAN 0-7,10,11 OUT WA 0,1
10X2
CHAN 0-7,10,11 OUT RA 0,1
10X2
CHAN 0-7,10,11 RESET RESYNC
10
CHAN 0-7,10,11 RESYNC A-D FULL
10X4
CHAN 0-7,10,11 OUT DATA BITS 48-63/64,65
10X16/2
10X16/2
10X16
CHAN 0-7,10,11 OUT
CHAN 0-7,10,11 OUT DATA BITS 64,65
10X2
CHAN 0-7,10,11 SYNC-OUT OUT
10
19B
CHAN 0-7,10,11 OUT DATA ERROR
10
19R
16H
CHAN 0-7,10,11 INV OUT BYTE 0,1 PAR
2X10
19S
CHAN 0-7,10,11 ENBL SYNC OUT
10
CHAN 0-7,10,11
SYNC OUT
10
19U
CHAN 0-7,10,11 XMIT ENBL
10
CHAN 0-7,10,11 SYNC OUT ACK
10
19B,19U
CHAN 0-7,10,11 BFR FULL
10
19W
19J
SEL HOLD
CHAN 0-7,10,11 OUT DATA BITS 48-63/64,65
10X16/2
19C
10X2
A
CMD SEQ
CHAN 0-7,10,11 PORTS A AND B SEL HOLD, CMD SEQ,SYNC OUT, INTERFACE CONT
10X2X4
ISI
CHAN 0-7,10,11 PORTS A AND B DATA BITS 0-15/PAR UPR,LWR
10X2X16/2
ISI
10X2X16/2
19D

NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM (EXT1) PORTS A AND B TRANSMITTERS. VALID SYNC OUT FORMATION CIO	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION		SHEET IOU 1.20	PAGE	

This is the sixth in the series of diagrams 1.16 through 1.22 that show portions of an ISI channel adapter. This diagram shows CIO channel (JY) board circuits that keep track of the CM address and byte count during a DMA transfer.

I REGISTER AND ASSOCIATED CIRCUITS

The T Register provides the real-memory address and byte count for DMA transfers. The initial values for this come from a PP and are loaded into the T Prime Register (1.18). From there, the values are transferred to the T Register if it is empty. This transfer must occur for the associated DMA operation to be performed.

The real-memory address and byte count values transferred into the T Register are the starting address and page length for the pending DMA transfer. Once the transfer begins, the real-memory address in the T Register is incremented by eight after each CM reference.

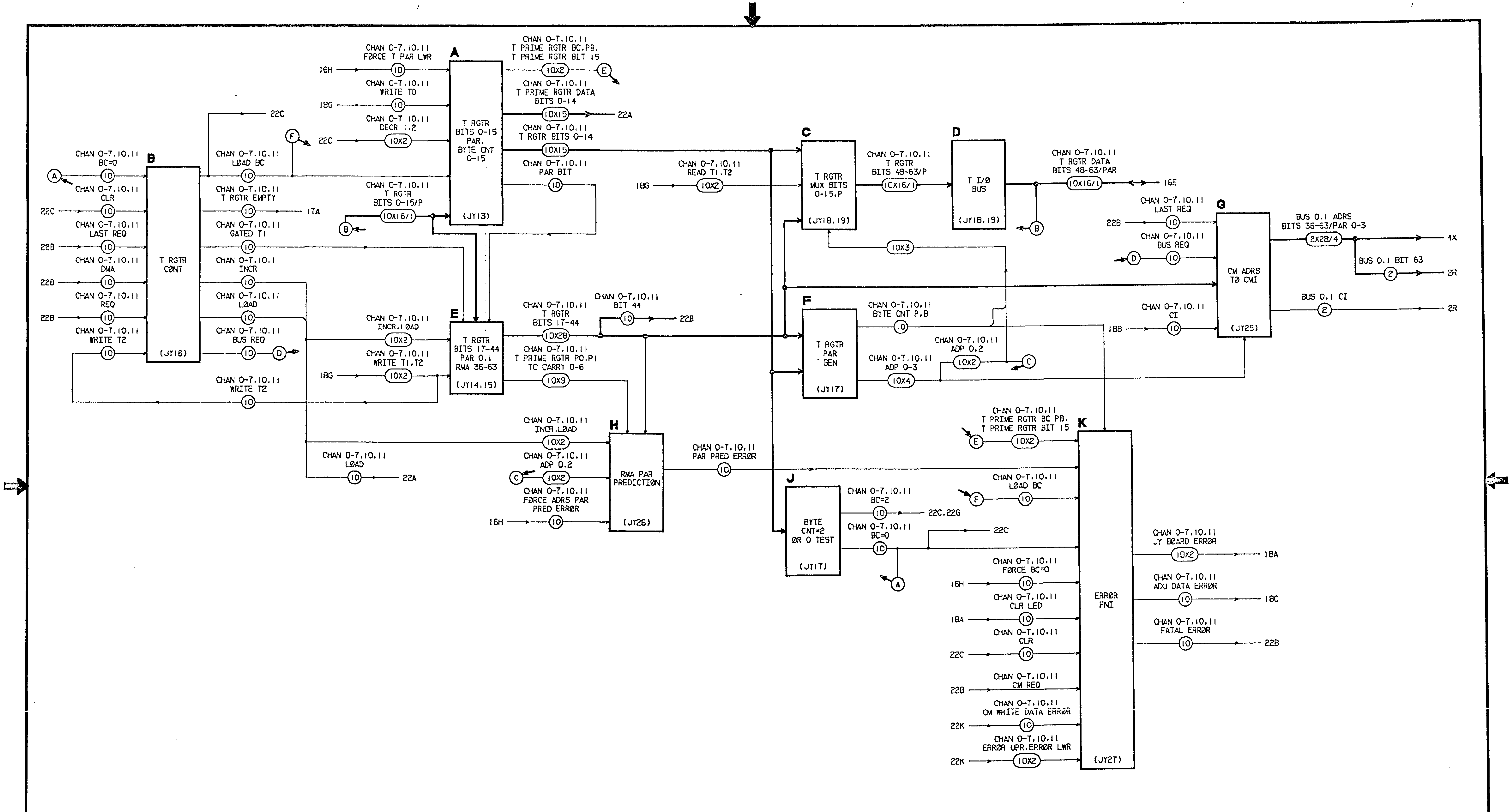
In addition, the byte count is decremented by 2 for each 16-bit word written into the Assembly Buffer (1.22) or read from the Disassembly Buffer (1.22). When the byte count reaches zero, the T Register is ready for new values from the T Prime Register.

The contents of the T Register may be read by a PP sending function code $x6x0_{16}$. The read requires three words (48 bits). The gating of the three words is handled by the T Register Mux.

If a DMA transfer halts because of an error, a PP can clear both the T and T Prime Registers by sending function code $xEx0_{16}$. The two registers may then be restored, and a retry performed without affecting the state of other circuits.

CM-ADDRESS-TO-CMI CIRCUIT

This circuit sends the real-memory address from the T Register to the CMI during a DMA transfer. The circuit also sends Cache Invalidate on every fourth and last CM write of a transfer if the Cache Invalidate bit is set in the Control Registers (1.16).


A
T RGTR BITS 0-15 PAR, BYTE CNT 0-15 (JY13)
16H CHAN 0-7,10,11 FORCE T PAR LWR 10
18G CHAN 0-7,10,11 WRITE TO 10
22C CHAN 0-7,10,11 DECR 1,2 10X2
CHAN 0-7,10,11 T RGTR BITS 0-15/P 10X16/1
CHAN 0-7,10,11 T PRIME RGTR BC,PB, T PRIME RGTR BIT 15 10X2 E
CHAN 0-7,10,11 T PRIME RGTR DATA BITS 0-14 10X15 22A
CHAN 0-7,10,11 T RGTR BITS 0-14 10X15
CHAN 0-7,10,11 PAR BIT 10
22C
F
B
T RGTR CONT (JY16)
A CHAN 0-7,10,11 BC=0 10
22C CHAN 0-7,10,11 CLR 10
22B CHAN 0-7,10,11 LAST REQ 10
22B CHAN 0-7,10,11 DMA 10
22B CHAN 0-7,10,11 REQ 10
CHAN 0-7,10,11 WRITE T2 10
CHAN 0-7,10,11 LOAD BC 10
CHAN 0-7,10,11 T RGTR EMPTY 10 1TA
CHAN 0-7,10,11 GATED T1 10
CHAN 0-7,10,11 INCR 10
CHAN 0-7,10,11 LOAD 10
CHAN 0-7,10,11 BUS REQ 10 D
CHAN 0-7,10,11 WRITE T2 10
C
T RGTR MUX BITS 0-15,P (JY18,19)
18G CHAN 0-7,10,11 READ T1,T2 10X2
CHAN 0-7,10,11 T RGTR BITS 48-63/P 10X16/1
10X3
D
T I/O BUS (JY18,19)
CHAN 0-7,10,11 T RGTR DATA BITS 48-63/PAR 10X16/1 16E
B
G
CM ADRS TO CMI (JY25)
22B CHAN 0-7,10,11 LAST REQ 10
D CHAN 0-7,10,11 BUS REQ 10
18B CHAN 0-7,10,11 CI 10
BUS 0,1 ADRS BITS 36-63/PAR 0-3 2X28/4 4X
BUS 0,1 BIT 63 2 2R
BUS 0,1 CI 2 2R
E
T RGTR BITS 17-44 PAR 0,1 RMA 36-63 (JY14,15)
CHAN 0-7,10,11 INCR,LOAD 10X2
18G CHAN 0-7,10,11 WRITE T1,T2 10X2
CHAN 0-7,10,11 T RGTR BITS 17-44 10X28
CHAN 0-7,10,11 BIT 44 10 22B
CHAN 0-7,10,11 T PRIME RGTR P0,P1 TC CARRY 0-6 10X9
F
T RGTR PAR GEN (JY17)
CHAN 0-7,10,11 BYTE CNT P,B 10
CHAN 0-7,10,11 ADP 0-3 10X4
CHAN 0-7,10,11 ADP 0,2 10X2 C
CHAN 0-7,10,11 LOAD 10 22A
H
RMA PAR PREDICTION (JY26)
CHAN 0-7,10,11 INCR,LOAD 10X2
C CHAN 0-7,10,11 ADP 0,2 10X2
16H CHAN 0-7,10,11 FORCE ADRS PAR PRED ERROR 10
CHAN 0-7,10,11 PAR PRED ERROR 10
J
BYTE CNT=2 OR 0 TEST (JY17)
CHAN 0-7,10,11 BC=2 10 22C,22G
CHAN 0-7,10,11 BC=0 10 22C
A
K
ERROR FNI (JY27)
E CHAN 0-7,10,11 T PRIME RGTR BC PB, T PRIME RGTR BIT 15 10X2
F CHAN 0-7,10,11 LOAD BC 10
16H CHAN 0-7,10,11 FORCE BC=0 10
18A CHAN 0-7,10,11 CLR LED 10
22C CHAN 0-7,10,11 CLR 10
22B CHAN 0-7,10,11 CM REQ
22K CHAN 0-7,10,11 CM WRITE DATA ERROR 10
22K CHAN 0-7,10,11 ERROR UPR,ERROR LWR 10X2
CHAN 0-7,10,11 JY BOARD ERROR 10X2 18A
CHAN 0-7,10,11 ADU DATA ERROR 10 18C
CHAN 0-7,10,11 FATAL ERROR 10 22B

NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CD CONTROL DATA DEVELOPMENT DIVISION	LEVEL I DIAGRAM (A/D) T RGTR CONT. ERROR FAN-IN. CM ADRS TO CMI CIO	60463540 SHEET IOU 1.21	REV C

This is the last in the series of diagrams starting at 1.16 that show portions of an ISI channel adapter. This diagram shows more JY board circuits. The circuits on this diagram assembles/disassembles CM words during a DMA transfer.

ASSEMBLY/DISASSEMBLY CIRCUITS

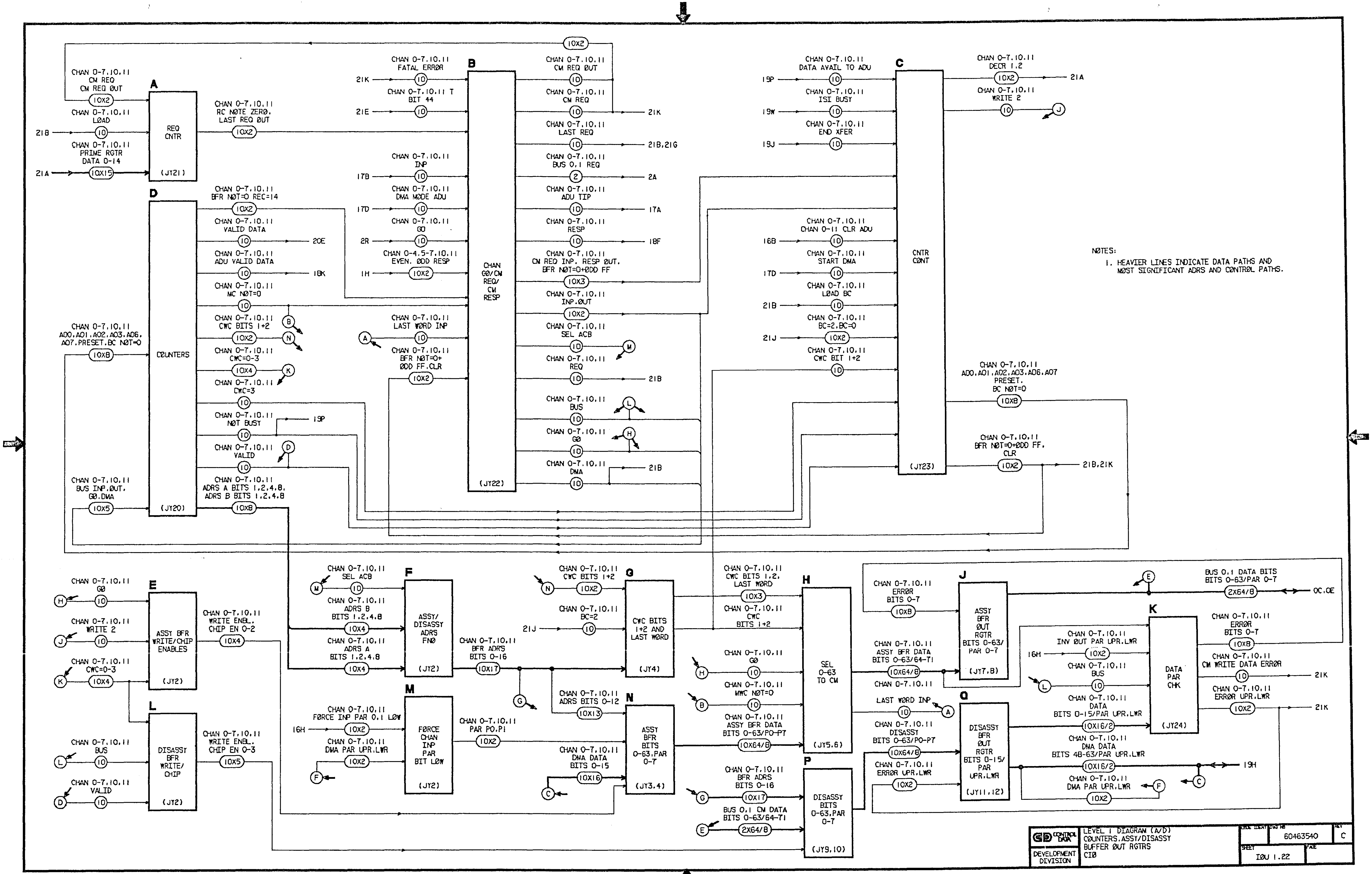
During DMA transfers, the assembly circuits assemble the 16-bit words used on the channel into the 64-bit words used in CM and the disassembly circuits do vice versa. The direction of the data flow in a DMA transfer is specified in the transfer function word. The adapter receives this word from a PP and transfers it to the selected external unit before the DMA transfer takes place.

COUNTERS

The Counters keep track of the number of 16-bit words that are being processed by the assembly/disassembly circuits.

CHANNEL GO/CM REQUEST/CM RESPONSE CIRCUITS

These circuits coordinate the DMA assembly/disassembly operations with the CM requests and responses.


A
REQ CNTR
(JY21)
CHAN 0-7,10,11 CM REQ CM REQ OUT
10X2
CHAN 0-7,10,11 LOAD
21B
CHAN 0-7,10,11 PRIME RGTR DATA 0-14
21A
10X15
CHAN 0-7,10,11 RC NOTE ZERO, LAST REQ OUT
D
COUNTERS
(JY20)
CHAN 0-7,10,11 BFR NOT=0 REC=14
CHAN 0-7,10,11 VALID DATA
20E
CHAN 0-7,10,11 ADU VALID DATA
18K
CHAN 0-7,10,11 MC NOT=0
CHAN 0-7,10,11 CWC BITS 1+2
CHAN 0-7,10,11 CWC=0-3
10X4
CHAN 0-7,10,11 CWC=3
CHAN 0-7,10,11 NOT BUSY
19P
CHAN 0-7,10,11 VALID
CHAN 0-7,10,11 ADRS A BITS 1,2,4,8, ADRS B BITS 1,2,4,8
10X8
CHAN 0-7,10,11 A00,A01,A02,A03,A06, A07,PRESET,BC NOT=0
CHAN 0-7,10,11 BUS INP,OUT, GO,DMA
10X5
B
CHAN GO/CM REQ/ CM RESP
(JY22)
CHAN 0-7,10,11 FATAL ERROR
21K
CHAN 0-7,10,11 T BIT 44
21E
CHAN 0-7,10,11 INP
17B
CHAN 0-7,10,11 DMA MODE ADU
17D
CHAN 0-7,10,11 GO
2R
CHAN 0-4,5-7,10,11 EVEN, ODD RESP
1H
CHAN 0-7,10,11 LAST WORD INP
CHAN 0-7,10,11 BFR NOT=0+ ODD FF,CLR
CHAN 0-7,10,11 CM REQ OUT
CHAN 0-7,10,11 CM REQ
21K
CHAN 0-7,10,11 LAST REQ
21B,21G
CHAN 0-7,10,11 BUS 0,1 REQ
2
2A
CHAN 0-7,10,11 ADU TIP
17A
CHAN 0-7,10,11 RESP
18F
CHAN 0-7,10,11 CM REQ INP, RESP OUT, BFR NOT=0+ODD FF
10X3
CHAN 0-7,10,11 INP,OUT
CHAN 0-7,10,11 SEL ACB
CHAN 0-7,10,11 REQ
21B
CHAN 0-7,10,11 BUS
CHAN 0-7,10,11 GO
CHAN 0-7,10,11 DMA
21B
C
CNTR CONT
(JY23)
CHAN 0-7,10,11 DATA AVAIL TO ADU
19P
CHAN 0-7,10,11 ISI BUSY
19W
CHAN 0-7,10,11 END XFER
19J
CHAN 0-7,10,11 CHAN 0-11 CLR ADU
16B
CHAN 0-7,10,11 START DMA
17D
CHAN 0-7,10,11 LOAD BC
21B
CHAN 0-7,10,11 BC=2,BC=0
21J
CHAN 0-7,10,11 CWC BIT 1+2
CHAN 0-7,10,11 DECR 1,2
21A
CHAN 0-7,10,11 WRITE 2
CHAN 0-7,10,11 A00,A01,A02,A03,A06,A07 PRESET, BC NOT=0
CHAN 0-7,10,11 BFR NOT=0+ODD FF, CLR
21B,21K
E
ASSY BFR WRITE/CHIP ENABLES
(JY2)
CHAN 0-7,10,11 GO
CHAN 0-7,10,11 WRITE 2
CHAN 0-7,10,11 CWC=0-3
CHAN 0-7,10,11 WRITE ENBL, CHIP EN 0-2
L
DISASSY BFR WRITE/ CHIP
(JY2)
CHAN 0-7,10,11 BUS
CHAN 0-7,10,11 VALID
CHAN 0-7,10,11 WRITE ENBL, CHIP EN 0-3
F
ASSY/ DISASSY ADRS FNO
(JY2)
CHAN 0-7,10,11 SEL ACB
CHAN 0-7,10,11 ADRS B BITS 1,2,4,8
CHAN 0-7,10,11 ADRS A BITS 1,2,4,8
CHAN 0-7,10,11 BFR ADRS BITS 0-16
10X17
M
FORCE CHAN INP PAR BIT LOW
(JY2)
CHAN 0-7,10,11 FORCE INP PAR 0,1 LOW
16H
CHAN 0-7,10,11 DMA PAR UPR,LWR
CHAN 0-7,10,11 PAR P0,P1
G
CWC BITS 1+2 AND LAST WORD
(JY4)
CHAN 0-7,10,11 CWC BITS 1+2
CHAN 0-7,10,11 BC=2
21J
N
ASSY BFR BITS 0-63,PAR 0-7
(JY3,4)
CHAN 0-7,10,11 ADRS BITS 0-12
10X13
CHAN 0-7,10,11 DMA DATA BITS 0-15
10X16
H
SEL 0-63 TO CM
(JY5,6)
CHAN 0-7,10,11 CWC BITS 1,2, LAST WORD
CHAN 0-7,10,11 CWC BITS 1+2
CHAN 0-7,10,11 GO
CHAN 0-7,10,11 MWC NOT=0
CHAN 0-7,10,11 ASSY BFR DATA BITS 0-63/P0-P7
10X64/8
P
DISASSY BITS 0-63,PAR 0-7
(JY9,10)
CHAN 0-7,10,11 BFR ADRS BITS 0-16
BUS 0,1 CM DATA BITS 0-63/64-71
2X64/8
J
ASSY BFR OUT RGTR BITS 0-63/ PAR 0-7
(JY7,8)
CHAN 0-7,10,11 ERROR BITS 0-7
CHAN 0-7,10,11 ASSY BFR DATA BITS 0-63/64-71
CHAN 0-7,10,11 LAST WORD INP
CHAN 0-7,10,11 DISASSY BITS 0-63/P0-P7
CHAN 0-7,10,11 ERROR UPR,LWR
BUS 0,1 DATA BITS 0-63/PAR 0-7
0C,0E
K
DATA PAR CHK
(JY24)
CHAN 0-7,10,11 INV OUT PAR UPR,LWR
16H
CHAN 0-7,10,11 BUS
CHAN 0-7,10,11 DATA BITS 0-15/PAR UPR,LWR
10X16/2
CHAN 0-7,10,11 ERROR BITS 0-7
CHAN 0-7,10,11 CM WRITE DATA ERROR
21K
CHAN 0-7,10,11 ERROR UPR,LWR
21K
Q
DISASSY BFR OUT RGTR BITS 0-15/ PAR UPR,LWR
(JY11,12)
CHAN 0-7,10,11 DMA DATA BITS 48-63/PAR UPR,LWR
19H
CHAN 0-7,10,11 DMA PAR UPR,LWR

NOTES:
1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

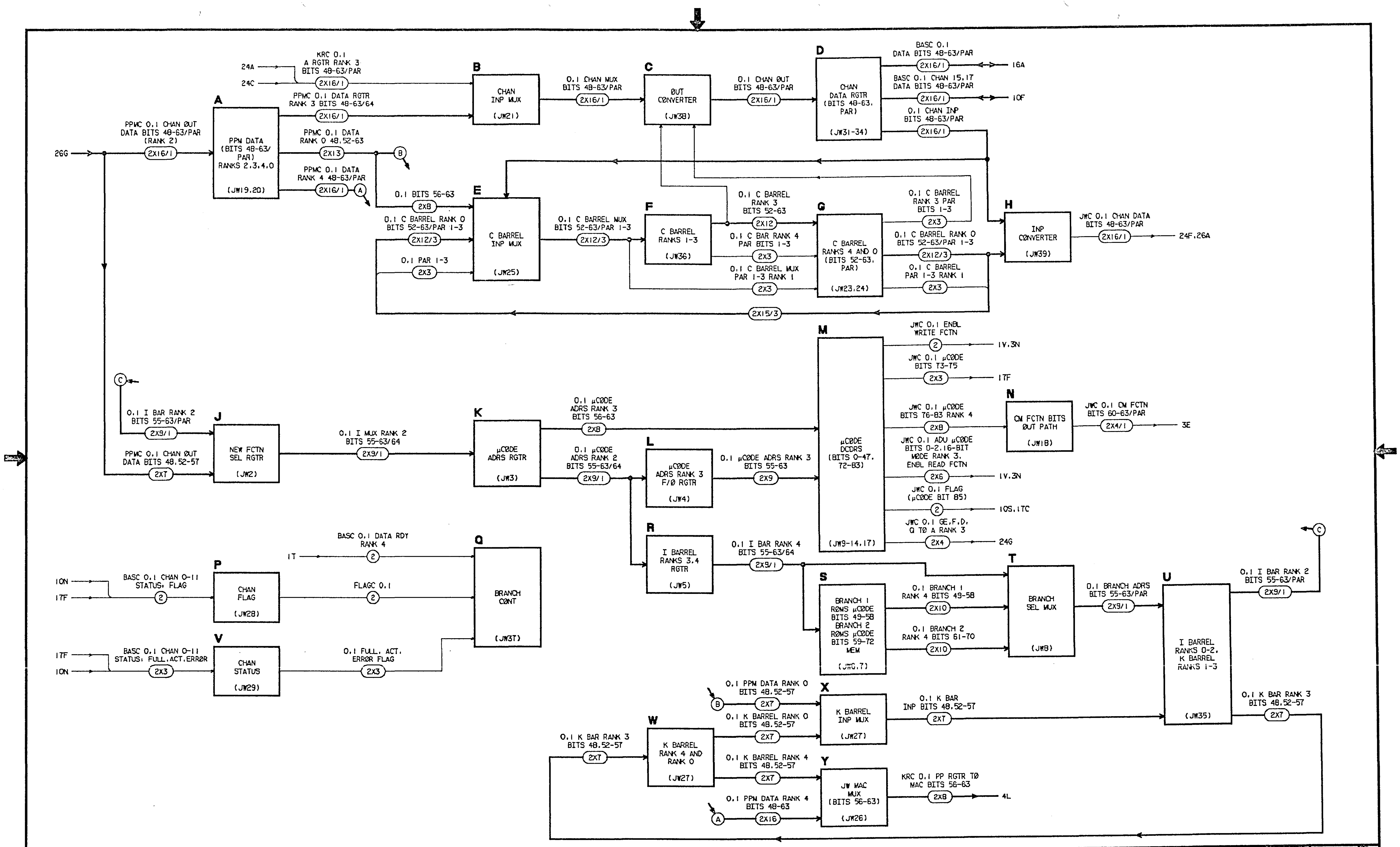
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (A/D)
COUNTERS.ASSY/DISASSY
BUFFER OUT RGTRS
CIO

DWG NO 60463540
REV C
SHEET IOU 1.22

C BARREL, I BARREL, K BARREL (CIO) (IOU 1.23)

The C, I, and K barrels in the CIO are the same as in the NIO. Refer to description for diagram 1.5.


KRC 0.1
A RGTR RANK 3
BITS 48-63/PAR
24A
24C
2X16/1
A
PPM DATA (BITS 48-63/ PAR) RANKS 2,3,4,0 (JW19,20)
PPMC 0.1 CHAN OUT DATA BITS 48-63/PAR (RANK 2)
26G
2X16/1
PPMC 0.1 DATA RGTR RANK 3 BITS 48-63/64
2X16/1
PPMC 0.1 DATA RANK 0 48,52-63
2X13
B
PPMC 0.1 DATA RANK 4 48-63/PAR
2X16/1
A
B
CHAN INP MUX (JW21)
0.1 CHAN MUX BITS 48-63/PAR
2X16/1
C
OUT CONVERTER (JW38)
0.1 CHAN OUT BITS 48-63/PAR
2X16/1
D
CHAN DATA RGTR (BITS 48-63, PAR) (JW31-34)
BASC 0.1 DATA BITS 48-63/PAR
2X16/1
16A
BASC 0.1 CHAN 15,17 DATA BITS 48-63/PAR
2X16/1
10F
0.1 CHAN INP BITS 48-63/PAR
2X16/1
E
0.1 BITS 56-63
2X8
C BARREL INP MUX (JW25)
0.1 C BARREL RANK 0 BITS 52-63/PAR 1-3
2X12/3
0.1 PAR 1-3
2X3
0.1 C BARREL MUX BITS 52-63/PAR 1-3
2X12/3
F
C BARREL RANKS 1-3 (JW36)
0.1 C BARREL RANK 3 BITS 52-63
2X12
0.1 C BAR RANK 4 PAR BITS 1-3
2X3
0.1 C BARREL MUX PAR 1-3 RANK 1
2X3
G
C BARREL RANKS 4 AND 0 (BITS 52-63, PAR) (JW23,24)
0.1 C BARREL RANK 3 PAR BITS 1-3
2X3
0.1 C BARREL RANK 0 BITS 52-63/PAR 1-3
2X12/3
0.1 C BARREL PAR 1-3 RANK 1
2X3
2X15/3
H
INP CONVERTER (JW39)
JWC 0.1 CHAN DATA BITS 48-63/PAR
2X16/1
24F,26A
M
JWC 0.1 ENBL WRITE FCTN
2
1V,3N
JWC 0.1 μCODE BITS T3-T5
2X3
1TF
JWC 0.1 μCODE BITS 76-83 RANK 4
2X8
N
CM FCTN BITS OUT PATH (JW18)
JWC 0.1 CM FCTN BITS 60-63/PAR
2X4/1
3E
JWC 0.1 ADU μCODE BITS 0-2,16-BIT MODE RANK 3, ENBL READ FCTN
2X6
1V,3N
JWC 0.1 FLAG (μCODE BIT 85)
2
10S,1TC
JWC 0.1 GE,F,D, Q TO A RANK 3
2X4
24G
μCODE DCDRS (BITS 0-47, 72-83) (JW9-14,17)
C
0.1 I BAR RANK 2 BITS 55-63/PAR
2X9/1
J
NEW FCTN SEL RGTR (JW2)
PPMC 0.1 CHAN OUT DATA BITS 48,52-57
2X7
0.1 I MUX RANK 2 BITS 55-63/64
2X9/1
K
μCODE ADRS RGTR (JW3)
0.1 μCODE ADRS RANK 3 BITS 56-63
2X8
0.1 μCODE ADRS RANK 2 BITS 55-63/64
2X9/1
L
μCODE ADRS RANK 3 F/O RGTR (JW4)
0.1 μCODE ADRS RANK 3 BITS 55-63
2X9
R
I BARREL RANKS 3,4 RGTR (JW5)
0.1 I BAR RANK 4 BITS 55-63/64
2X9/1
C
P
CHAN FLAG (JW28)
10N
1TF
BASC 0.1 CHAN 0-11 STATUS, FLAG
2
FLAGC 0.1
2
BASC 0.1 DATA RDY RANK 4
1T
2
Q
BRANCH CONT (JW3T)
V
CHAN STATUS (JW29)
1TF
10N
BASC 0.1 CHAN 0-11 STATUS: FULL,ACT,ERROR
2X3
0.1 FULL, ACT, ERROR FLAG
2X3
S
BRANCH 1 ROWS μCODE BITS 49-58 BRANCH 2 ROWS μCODE BITS 59-72 MEM (JWC,7)
0.1 BRANCH 1 RANK 4 BITS 49-58
2X10
0.1 BRANCH 2 RANK 4 BITS 61-70
2X10
T
BRANCH SEL MUX (JW8)
0.1 BRANCH ADRS BITS 55-63/PAR
2X9/1
U
I BARREL RANKS 0-2, K BARREL RANKS 1-3 (JW35)
0.1 I BAR RANK 2 BITS 55-63/PAR
2X9/1
0.1 K BAR RANK 3 BITS 48,52-57
2X7
X
0.1 PPM DATA RANK 0 BITS 48,52-57
B
2X7
K BARREL INP MUX (JW27)
0.1 K BARREL RANK 0 BITS 48,52-57
2X7
0.1 K BAR INP BITS 48,52-57
2X7
W
0.1 K BAR RANK 3 BITS 48,52-57
2X7
K BARREL RANK 4 AND RANK 0 (JW27)
Y
0.1 K BARREL RANK 4 BITS 48,52-57
2X7
0.1 PPM DATA RANK 4 BITS 48-63
A
2X16
JW MAC MUX (BITS 56-63) (JW26)
KRC 0.1 PP RGTR TO MAC BITS 56-63
2X8
4L

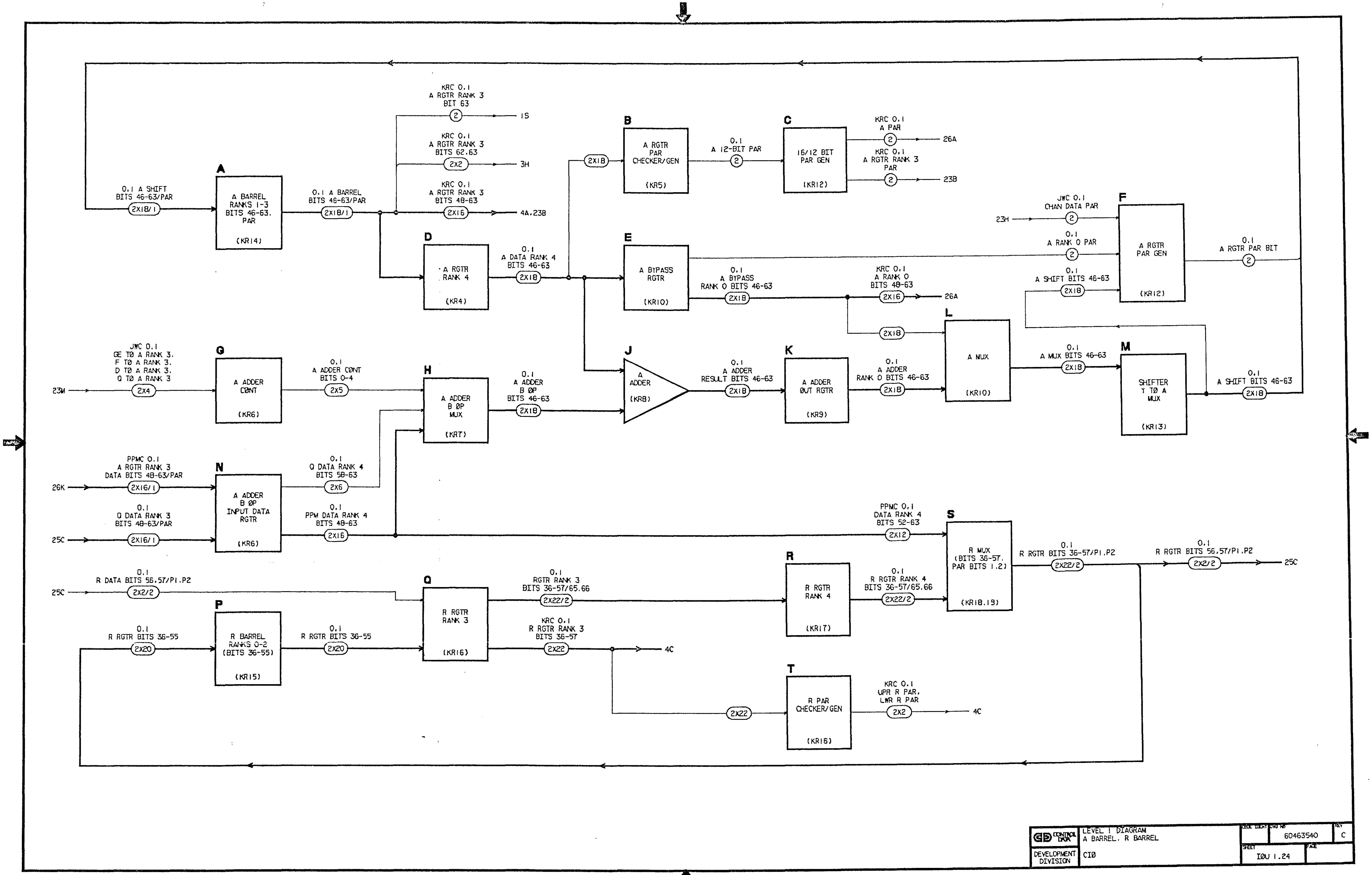
NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM C BARREL, I BARREL, K BARREL	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	CIO	SHEET IOU 1.23	PAGE	

A BARREL, R BARREL (CIO) (IOU 1.24)

The A and R barrels in the CIO are the same as in the NIO. Refer to description for diagram 1.6.

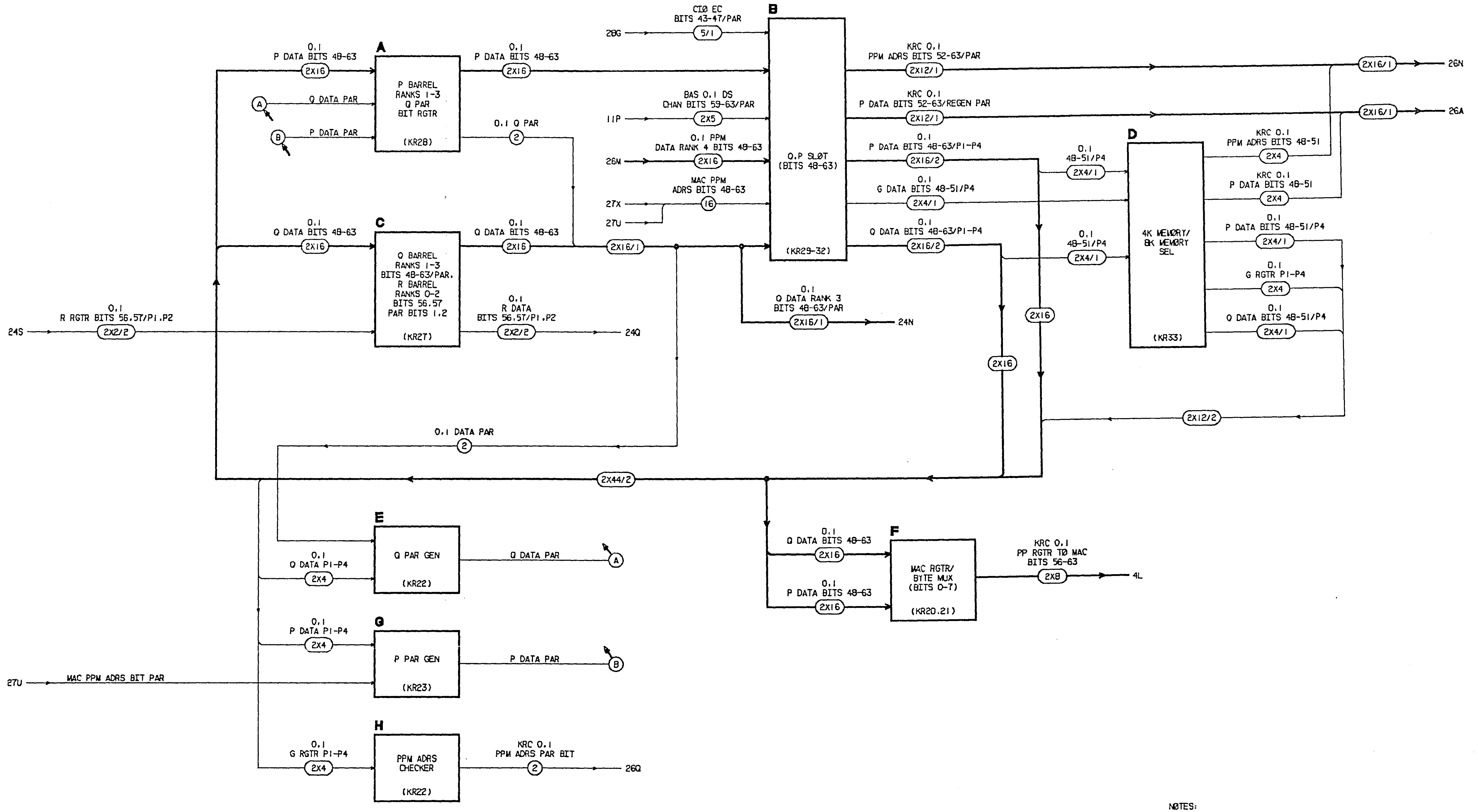


A
A BARREL RANKS 1-3 BITS 46-63, PAR (KR14)
0.1 A SHIFT BITS 46-63/PAR
2X18/1
0.1 A BARREL BITS 46-63/PAR
2X18/1
KRC 0.1 A RGTR RANK 3 BIT 63
2
1S
KRC 0.1 A RGTR RANK 3 BITS 62,63
2X2
3H
KRC 0.1 A RGTR RANK 3 BITS 48-63
2X16
4A,23B
B
A RGTR PAR CHECKER/GEN (KR5)
2X18
0.1 A 12-BIT PAR
2
C
16/12 BIT PAR GEN (KR12)
KRC 0.1 A PAR
2
26A
KRC 0.1 A RGTR RANK 3 PAR
2
23B
D
A RGTR RANK 4 (KR4)
0.1 A DATA RANK 4 BITS 46-63
2X18
E
A BYPASS RGTR (KR10)
0.1 A BYPASS RANK 0 BITS 46-63
2X18
KRC 0.1 A RANK 0 BITS 48-63
2X16
26A
2X18
F
A RGTR PAR GEN (KR12)
23H
JWC 0.1 CHAN DATA PAR
2
0.1 A RANK 0 PAR
2
0.1 A SHIFT BITS 46-63
2X18
0.1 A RGTR PAR BIT
2
G
A ADDER CONT (KR6)
JWC 0.1 GE TO A RANK 3, F TO A RANK 3, D TO A RANK 3, Q TO A RANK 3
23M
2X4
0.1 A ADDER CONT BITS 0-4
2X5
H
A ADDER B OP MUX (KR7)
0.1 A ADDER B OP BITS 46-63
2X18
J
A ADDER (KR8)
0.1 A ADDER RESULT BITS 46-63
2X18
K
A ADDER OUT RGTR (KR9)
0.1 A ADDER RANK 0 BITS 46-63
2X18
L
A MUX (KR10)
0.1 A MUX BITS 46-63
2X18
M
SHIFTER Y TO A MUX (KR13)
0.1 A SHIFT BITS 46-63
2X18
N
A ADDER B OP INPUT DATA RGTR (KR6)
PPMC 0.1 A RGTR RANK 3 DATA BITS 48-63/PAR
26K
2X16/1
0.1 Q DATA RANK 3 BITS 48-63/PAR
25C
2X16/1
0.1 Q DATA RANK 4 BITS 58-63
2X6
0.1 PPM DATA RANK 4 BITS 48-63
2X16
PPMC 0.1 DATA RANK 4 BITS 52-63
2X12
S
R MUX (BITS 36-57, PAR BITS 1,2) (KR18,19)
0.1 R RGTR BITS 36-57/P1,P2
2X22/2
0.1 R RGTR BITS 56,57/P1,P2
2X2/2
25C
0.1 R DATA BITS 56,57/P1,P2
25C
2X2/2
Q
R RGTR RANK 3 (KR16)
0.1 RGTR RANK 3 BITS 36-57/65,66
2X22/2
R
R RGTR RANK 4 (KR17)
0.1 R RGTR RANK 4 BITS 36-57/65,66
2X22/2
P
R BARREL RANKS 0-2 (BITS 36-55) (KR15)
0.1 R RGTR BITS 36-55
2X20
0.1 R RGTR BITS 36-55
2X20
KRC 0.1 R RGTR RANK 3 BITS 36-57
2X22
4C
2X22
T
R PAR CHECKER/GEN (KR16)
KRC 0.1 UPR R PAR, LWR R PAR
2X2
4C

CONTROL DATA
LEVEL 1 DIAGRAM
A BARREL, R BARREL
DEVELOPMENT DIVISION
CIO
60463540
C
IOU 1.24

P BARREL, Q BARREL (CIO) (IOU 1.25)

This diagram shows register (KR) board circuits in a BAS of the CIO. These circuits operate the same as described for diagram 1.7. However, the 4K/8K Memory Select circuits in the CIO are always in 8K mode. This is because Environment Control Register Bit 32 (1.28) is constantly set for 8K.


A
P BARREL RANKS 1-3 Q PAR BIT RGTR (KR28)
B
O.P SLOT (BITS 48-63) (KR29-32)
C
Q BARREL RANKS 1-3 BITS 48-63/PAR. R BARREL RANKS 0-2 BITS 56.57 PAR BITS 1.2 (KR27)
D
4K MEMORY/ 8K MEMORY SEL (KR33)
E
Q PAR GEN (KR22)
F
MAC RGTR/ BYTE MUX (BITS 0-7) (KR20.21)
G
P PAR GEN (KR23)
H
PPM ADRS CHECKER (KR22)
0.1 P DATA BITS 48-63 2X16
0.1 P DATA BITS 48-63 2X16
Q DATA PAR
P DATA PAR
0.1 Q PAR 2
28G CIO EC BITS 43-47/PAR 5/1
11P BAS 0.1 DS CHAN BITS 59-63/PAR 2X5
26M 0.1 PPM DATA RANK 4 BITS 48-63 2X16
27X MAC PPM ADRS BITS 48-63 16
27U
KRC 0.1 PPM ADRS BITS 52-63/PAR 2X12/1
KRC 0.1 P DATA BITS 52-63/REGEN PAR 2X12/1
0.1 P DATA BITS 48-63/P1-P4 2X16/2
0.1 G DATA BITS 48-51/P4 2X4/1
0.1 Q DATA BITS 48-63/P1-P4 2X16/2
2X16/1 26N
2X16/1 26A
0.1 48-51/P4 2X4/1
0.1 48-51/P4 2X4/1
KRC 0.1 PPM ADRS BITS 48-51 2X4
KRC 0.1 P DATA BITS 48-51 2X4
0.1 P DATA BITS 48-51/P4 2X4/1
0.1 G RGTR P1-P4 2X4
0.1 Q DATA BITS 48-51/P4 2X4/1
2X16
2X16
2X12/2
0.1 Q DATA BITS 48-63 2X16
0.1 Q DATA BITS 48-63 2X16
2X16/1
0.1 Q DATA RANK 3 BITS 48-63/PAR 2X16/1 24N
24S 0.1 R RGTR BITS 56.57/P1.P2 2X2/2
0.1 R DATA BITS 56.57/P1.P2 2X2/2 24Q
0.1 DATA PAR 2
2X44/2
0.1 Q DATA P1-P4 2X4
Q DATA PAR A
0.1 P DATA P1-P4 2X4
P DATA PAR B
27U MAC PPM ADRS BIT PAR
0.1 G RGTR P1-P4 2X4
KRC 0.1 PPM ADRS PAR BIT 2 26Q
0.1 Q DATA BITS 48-63 2X16
0.1 P DATA BITS 48-63 2X16
KRC 0.1 PP RGTR TO MAC BITS 56-63 2X8 4L

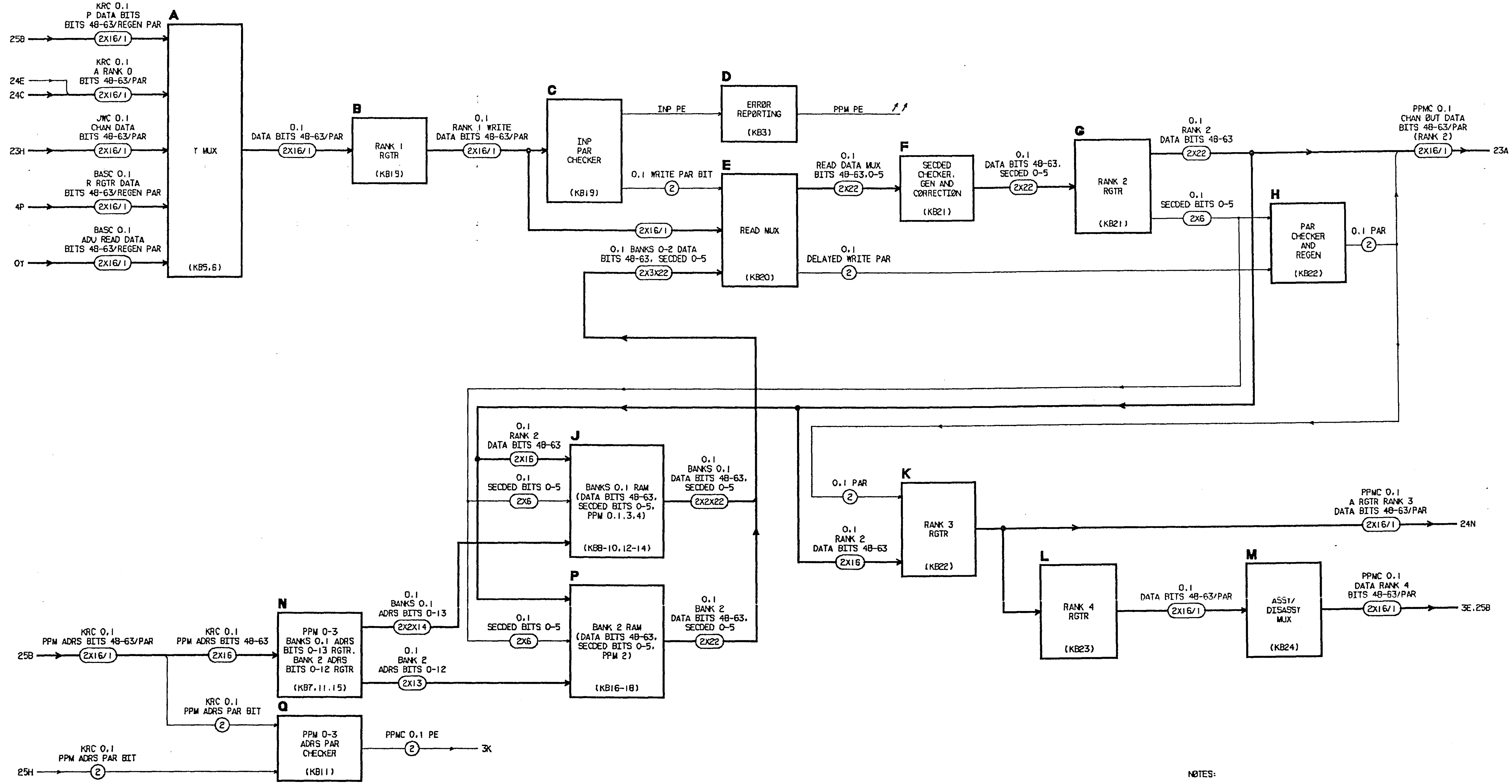
NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM P BARREL. R BARREL. Q BARREL CIO	CODE IDENT / DWG NO 60463540	REV C
DEVELOPMENT DIVISION		SHEET IOU 1.25	PAGE

PP MEMORY (CIO) (IOU 1.26)

This diagram shows PP memory (KB) board circuits in a BAS of the CIO. These circuits operate the same as described for diagram 1.8 except that the PPM in the CIO is always in 8K mode.



NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM PP MEMORY	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	CIO	SHEET IOU 1.26	PAGE	

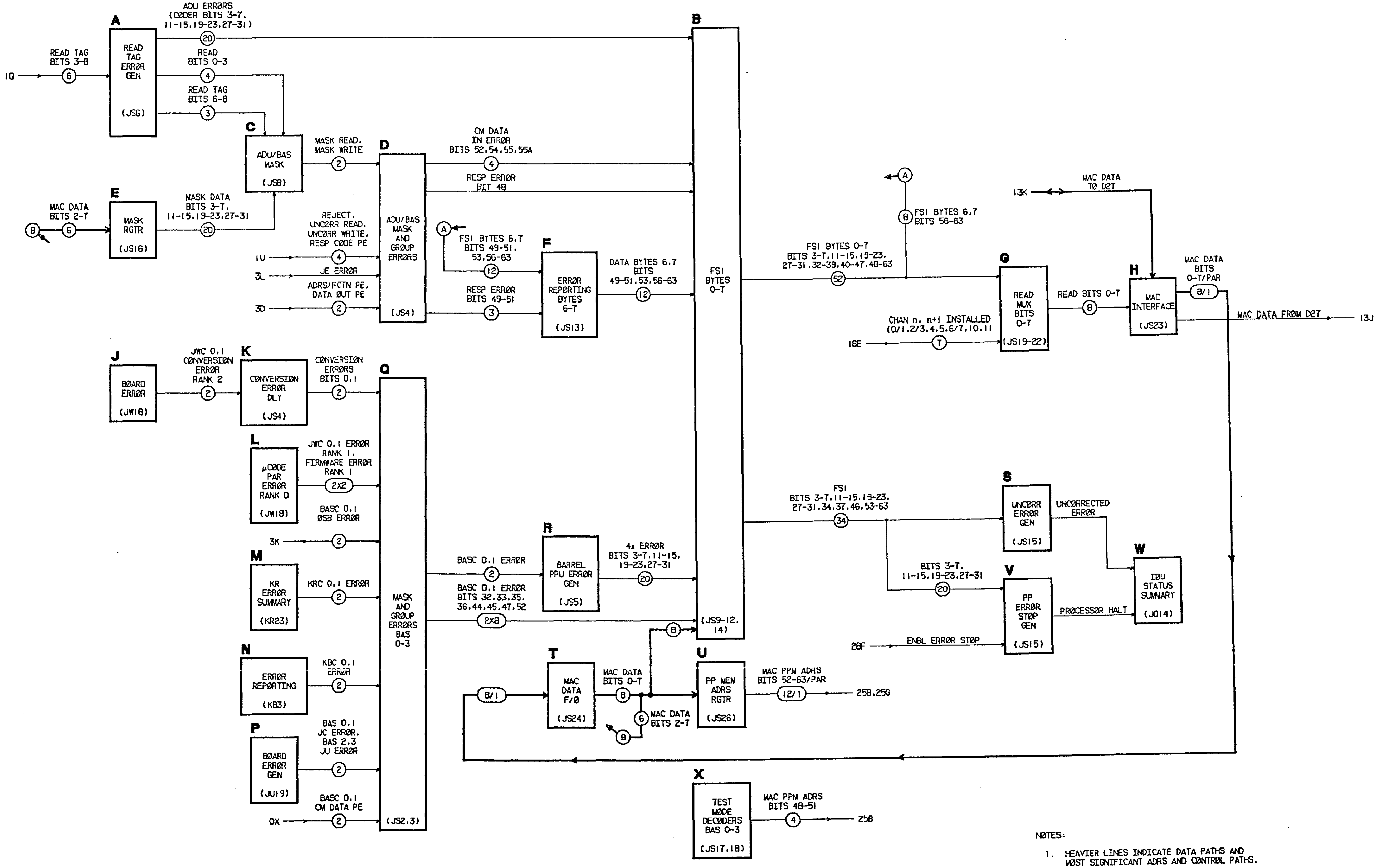
MAINTENANCE REGISTER A (CIO) (IOU 1.27)

The majority of the circuits shown on this diagram are maintenance register A (JS) board circuits. These JS board circuits assemble and mask fault status 1 information for the CIO. This occurs in the same manner described for diagram 1.14.

Table 1-12 lists the fault status 1 information for the CIO.

Table 1-12. CIO Fault Status 1 Information

Byte	Bits	Error Indication When Set
0	0-2	Not used
	3	BAS 0, PP4 error
	4	BAS 0, PP3 error
	5	BAS 0, PP2 error
	6	BAS 0, PP1 error
	7	BAS 0, PP0 error
1	8-10	Not used
	11	BAS 1, PP4 error
	12	BAS 1, PP3 error
	13	BAS 1, PP2 error
	14	BAS 1, PP1 error
	15	BAS 1, PP0 error
2	16-23	Not used
3	24-31	Not used
4	32	Error detected on JW board
	33	Error detected on KR board
	34	Not used
	35	Error detected on KB board
	36	Error detected on JC board
	37	Error detected on JD board
	38	Error detected on JE board
	39	Error detected on JF board
5	40	SECDED error, BAS 0
	41	SECDED error, BAS 1
	42	Not used
	43	Not used
	44	12/16-conversion error
	45	OS bounds violation
	46	OS boundary address parity error
	47	Firmware error
6	48	Response code error
	49	Uncorrected CM read error
	50	Uncorrected CM write error
	51	CM reject
	52	Data-in error - CMI/ADU
	53	Not used
	54	Data-out error - CMI/ADU
	55	Address/function error - CMI/ADU/BAS
7	56-63	Not used


A
READ TAG ERROR GEN (JS6)
READ TAG BITS 3-8
1Q
6
ADU ERRORS (CODER BITS 3-7, 11-15,19-23,27-31)
20
READ BITS 0-3
4
READ TAG BITS 6-8
3
C
ADU/BAS MASK (JS8)
MASK READ, MASK WRITE
2
E
MASK RGTR (JS16)
MAC DATA BITS 2-7
B
6
MASK DATA BITS 3-7, 11-15,19-23,27-31
20
D
ADU/BAS MASK AND GROUP ERRORS (JS4)
REJECT, UNCORR READ, UNCORR WRITE, RESP CODE PE
1U
4
3L
JE ERROR
3D
ADRS/FCTN PE, DATA OUT PE
2
CM DATA IN ERROR BITS 52,54,55,55A
4
RESP ERROR BIT 48
A
FSI BYTES 6,7 BITS 49-51, 53,56-63
12
RESP ERROR BITS 49-51
3
F
ERROR REPORTING BYTES 6-7 (JS13)
DATA BYTES 6,7 BITS 49-51,53,56-63
12
B
FSI BYTES 0-7 (JS9-12, 14)
J
BOARD ERROR (JW18)
JWC 0,1 CONVERSION ERROR RANK 2
2
K
CONVERSION ERROR DLY (JS4)
CONVERSION ERRORS BITS 0,1
2
Q
MASK AND GROUP ERRORS BAS 0-3 (JS2,3)
L
μCODE PAR ERROR RANK 0 (JW18)
JWC 0,1 ERROR RANK 1, FIRMWARE ERROR RANK 1
2X2
BASC 0,1 OSB ERROR
3K
2
M
KR ERROR SUMMARY (KR23)
KRC 0,1 ERROR
2
N
ERROR REPORTING (KB3)
KBC 0,1 ERROR
2
P
BOARD ERROR GEN (JU19)
BAS 0,1 JC ERROR, BAS 2,3 JU ERROR
2
BASC 0,1 CM DATA PE
0X
2
R
BARREL PPU ERROR GEN (JS5)
BASC 0,1 ERROR
2
BASC 0,1 ERROR BITS 32,33,35, 36,44,45,47,52
2X8
4x ERROR BITS 3-7,11-15, 19-23,27-31
20
A
FSI BYTES 6,7 BITS 56-63
8
FSI BYTES 0-7 BITS 3-7,11-15,19-23, 27-31,32-39,40-47,48-63
52
G
READ MUX BITS 0-7 (JS19-22)
CHAN n, n+1 INSTALLED (0/1,2/3,4,5,6/7,10,11)
18E
T
READ BITS 0-7
8
13K
MAC DATA TO D27
H
MAC INTERFACE (JS23)
MAC DATA BITS 0-7/PAR
8/1
MAC DATA FROM D27
13J
S
UNCORR ERROR GEN (JS15)
FSI BITS 3-7,11-15,19-23, 27-31,34,37,46,53-63
34
UNCORRECTED ERROR
BITS 3-7, 11-15,19-23,27-31
20
V
PP ERROR STOP GEN (JS15)
28F
ENBL ERROR STOP
PROCESSOR HALT
W
IOU STATUS SUMMARY (JQ14)
T
MAC DATA F/O (JS24)
8/1
MAC DATA BITS 0-7
8
8
6
MAC DATA BITS 2-7
B
B
U
PP MEM ADRS RGTR (JS26)
MAC PPN ADRS BITS 52-63/PAR
12/1
25B,25G
X
TEST MODE DECODERS BAS 0-3 (JS17,18)
MAC PPN ADRS BITS 48-51
4
25B

NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

CONTROL DATA	LEVEL 1 DIAGRAM MAINTENANCE RGTR A	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	CIO	SHEET IOU 1.27	PAGE	

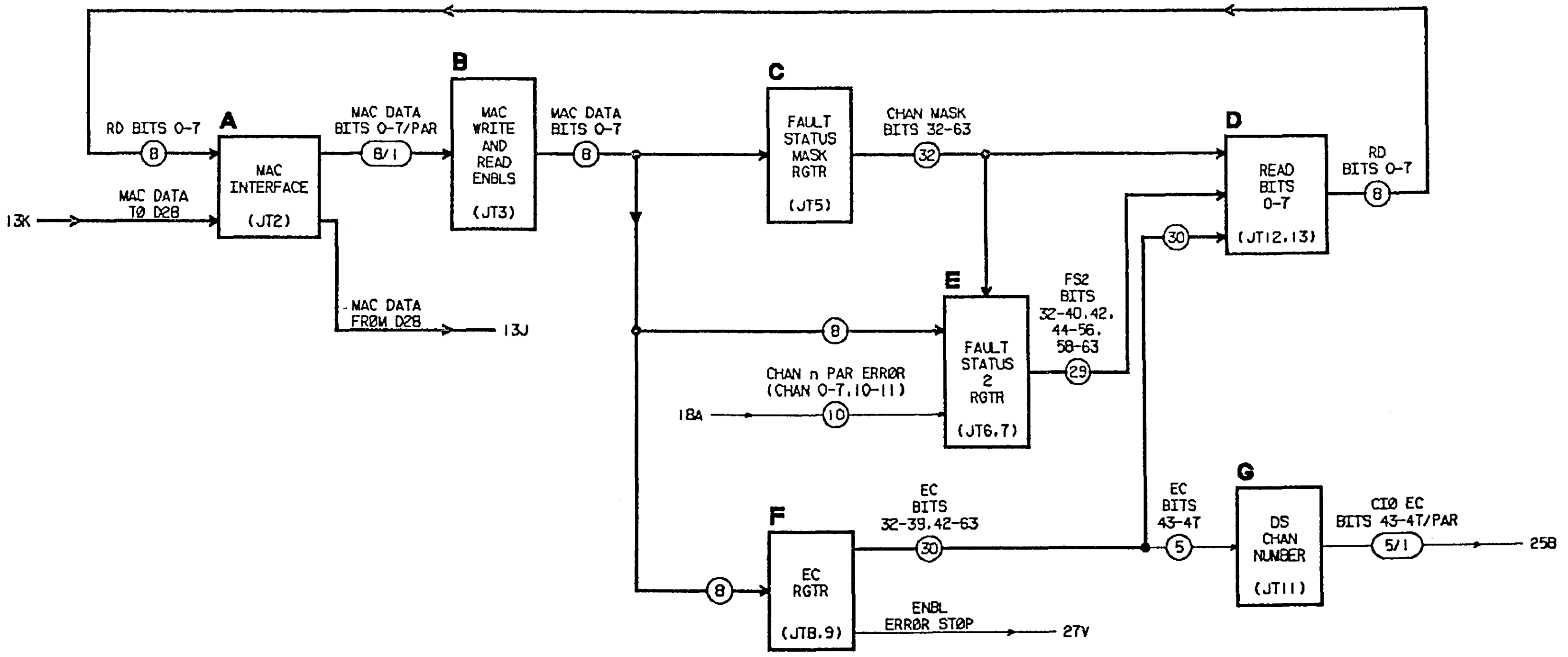
MAINTENANCE REGISTER B (CIO) (IOU 1.28)

The maintenance register B (JT) board circuits shown on this diagram assemble and mask fault status 2 information for the CIO and store its EC bits. This occurs in the same manner described for diagram 1.15. However, EC bit 32 for the CIO is always set to select 8K PPM operation.

The fault status 2 information for the CIO is listed in table 1-13.

Table 1-13. CIO Fault Status 2 Information

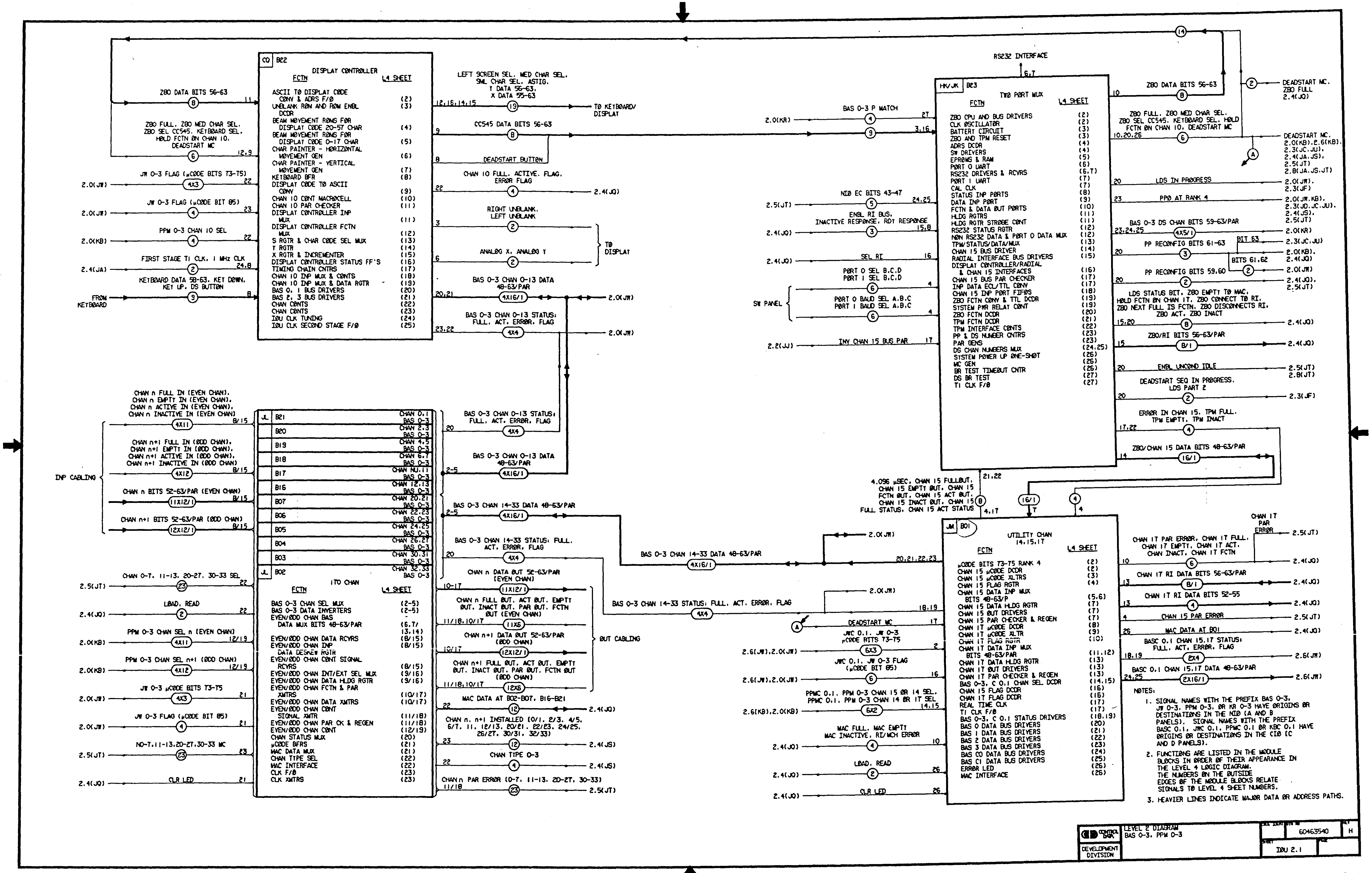
Byte	Bits	Error Indication When Set
0-3	0-31	Not used
4	32	Channel 7 error
	33	Channel 6 error
	34	Channel 5 error
	35	Channel 4 error
	36	Channel 3 error
	37	Channel 2 error
	38	Channel 1 error
	39	Channel 0 error
5	40-45	Not used
	46	Channel 11 error
	47	Channel 10 error
6	48-55	Not used
7	56-63	Not used



NOTES:

1. HEAVIER LINES INDICATE DATA PATHS AND MOST SIGNIFICANT ADRS AND CONTROL PATHS.

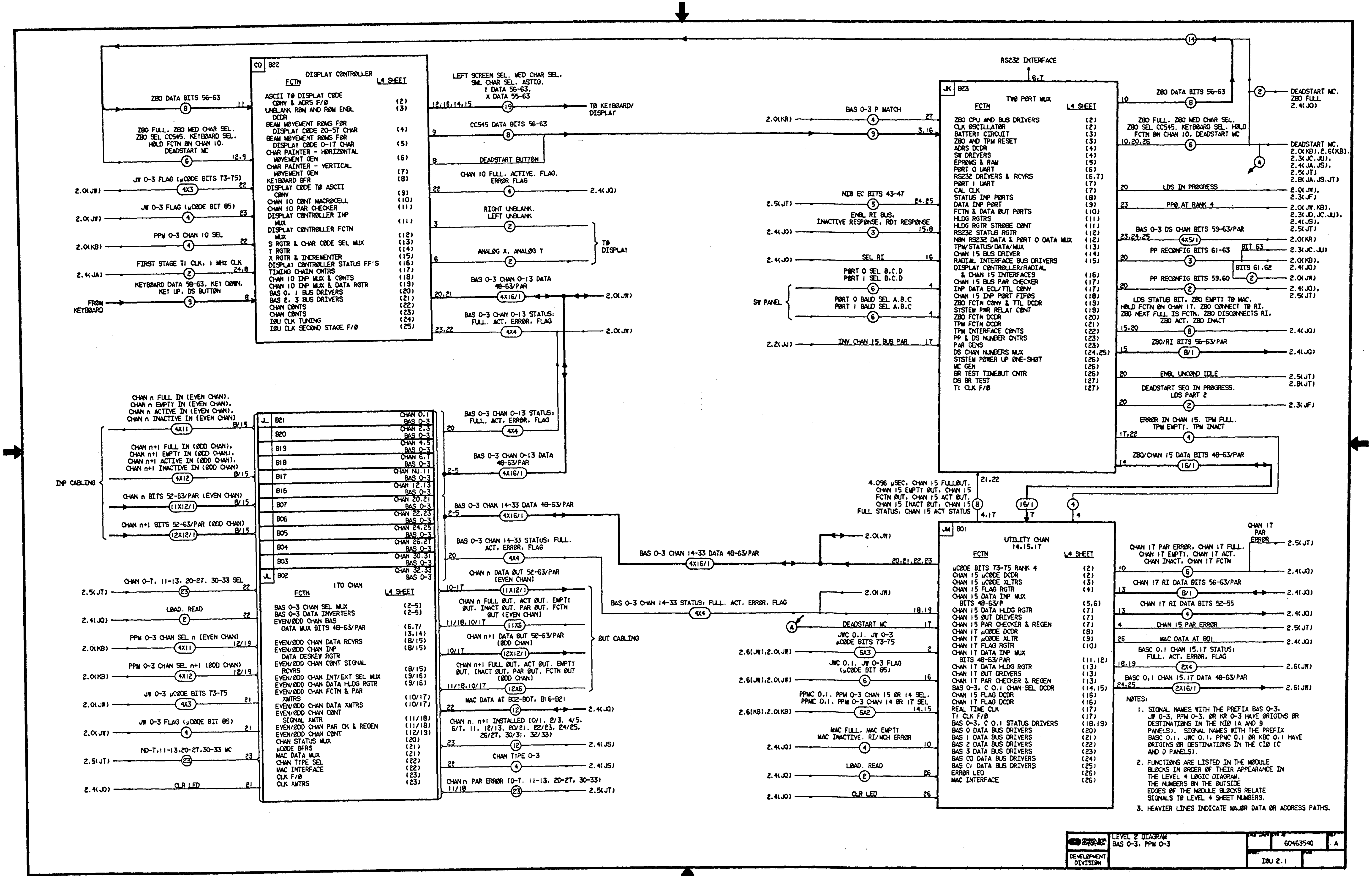
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM
MAINTENANCE RGTR B
CIO
CODE IDENT
DWG NO 60463540
REV C
SHEET IOU 1.28
PAGE


CQ B22
DISPLAY CONTROLLER
FCTN L4 SHEET
ASCII TO DISPLAY CODE CONV & ADRS F/0 (2)
UNBLANK ROW AND ROW ENBL DCDR (3)
BEAM MOVEMENT ROWS FOR DISPLAY CODE 20-57 CHAR (4)
BEAM MOVEMENT ROWS FOR DISPLAY CODE 0-17 CHAR (5)
CHAR PAINTER - HORIZONTAL MOVEMENT GEN (6)
CHAR PAINTER - VERTICAL MOVEMENT GEN (7)
KEYBOARD BFR (8)
DISPLAY CODE TO ASCII CONV (9)
CHAN 10 CONT MACROCELL (10)
CHAN 10 PAR CHECKER (11)
DISPLAY CONTROLLER INP MUX (11)
DISPLAY CONTROLLER FCTN MUX (12)
S RGTR & CHAR CODE SEL MUX (13)
Y RGTR (14)
X RGTR & INCREMENTER (15)
DISPLAY CONTROLLER STATUS FF'S (16)
TIMING CHAIN CNTRS (17)
CHAN 10 INP MUX & CONTS (18)
CHAN 10 INP MUX & DATA RGTR (19)
BAS 0, 1 BUS DRIVERS (20)
BAS 2, 3 BUS DRIVERS (21)
CHAN CONTS (22)
CHAN CONTS (23)
IOU CLK TUNING (24)
IOU CLK SECOND STAGE F/0 (25)
Z80 DATA BITS 56-63
8
11
Z80 FULL, Z80 MED CHAR SEL, Z80 SEL CC545, KEYBOARD SEL, HOLD FCTN ON CHAN 10, DEADSTART MC
6
12,9
JW 0-3 FLAG (µCODE BITS T3-T5)
4X3
22
2.0(JW)
JW 0-3 FLAG (µCODE BIT 05)
4
23
2.0(JW)
PPM 0-3 CHAN 10 SEL
4
22
2.0(KB)
FIRST STAGE TI CLK, 1 MHz CLK
2
24,8
2.4(JA)
KEYBOARD DATA 58-63, KEY DOWN, KEY UP, DS BUTTON
9
8
FROM KEYBOARD
LEFT SCREEN SEL, MED CHAR SEL, SML CHAR SEL, ASTIG, Y DATA 56-63, X DATA 55-63
12,16,14,15
19
TO KEYBOARD/ DISPLAY
CC545 DATA BITS 56-63
9
8
8
DEADSTART BUTTON
CHAN 10 FULL, ACTIVE, FLAG, ERROR FLAG
22
4
2.4(JQ)
RIGHT UNBLANK, LEFT UNBLANK
3
2
ANALOG X, ANALOG Y
6
2
TO DISPLAY
BAS 0-3 CHAN 0-13 DATA 48-63/PAR
20,21
4X16/1
2.0(JW)
BAS 0-3 CHAN 0-13 STATUS: FULL, ACT, ERROR, FLAG
23,22
4X4
2.0(JW)
RS232 INTERFACE
6,7
HV/JK B23
TWO PORT MUX
FCTN L4 SHEET
Z80 CPU AND BUS DRIVERS (2)
CLK OSCILLATOR (2)
BATTERY CIRCUIT (3)
Z80 AND TPM RESET (3)
ADRS DCDR (4)
SW DRIVERS (4)
EPROMS & RAM (5)
PORT 0 UART (6)
RS232 DRIVERS & RCVRS (6,7)
PORT 1 UART (7)
CAL CLK (7)
STATUS INP PORTS (8)
DATA INP PORT (9)
FCTN & DATA OUT PORTS (10)
HLDG RGTRS (11)
HLDG RGTR STROBE CONT (11)
RS232 STATUS RGTR (12)
NON RS232 DATA & PORT 0 DATA MUX (12)
TPM/STATUS/DATA/MUX (13)
CHAN 15 BUS DRIVER (14)
RADIAL INTERFACE BUS DRIVERS (15)
DISPLAY CONTROLLER/RADIAL & CHAN 15 INTERFACES (16)
CHAN 15 BUS PAR CHECKER (17)
INP DATA ECL/TTL CONV (17)
CHAN 15 INP PORT FIFOS (18)
Z80 FCTN CONV & TTL DCDR (19)
SYSTEM PWR RELAY CONT (19)
Z80 FCTN DCDR (20)
TPM FCTN DCDR (21)
TPM INTERFACE CONTS (22)
PP & DS NUMBER CNTRS (23)
PAR GENS (23)
DS CHAN NUMBERS MUX (24,25)
SYSTEM POWER UP ONE-SHOT (26)
MC GEN (26)
BR TEST TIMEOUT CNTR (26)
DS BR TEST (27)
TI CLK F/0 (27)
BAS 0-3 P MATCH
2.0(KR)
4
27
9
3,16
NIO EC BITS 43-47
2.5(JT)
5
24,25
ENBL RI BUS, INACTIVE RESPONSE, RDY RESPONSE
2.4(JQ)
3
15,8
SEL RI
2.4(JQ)
2
16
PORT 0 SEL B,C,D
PORT 1 SEL B,C,D
6
4
SW PANEL
PORT 0 BAUD SEL A,B,C
PORT 1 BAUD SEL A,B,C
6
4
INV CHAN 15 BUS PAR
2.2(JJ)
1
17
14
Z80 DATA BITS 56-63
10
8
2
DEADSTART MC, Z80 FULL
2.4(JQ)
Z80 FULL, Z80 MED CHAR SEL, Z80 SEL CC545, KEYBOARD SEL, HOLD FCTN ON CHAN 10, DEADSTART MC
10,20,26
6
DEADSTART MC, 2.0(KB),2.6(KB), 2.3(JC,JU), 2.4(JA,JS), 2.5(JT), 2.8(JA,JS,JT)
A
20
LDS IN PROGRESS
2.0(JW), 2.3(JF)
23
PPO AT RANK 4
2.0(JW,KB), 2.3(JD,JC,JU), 2.4(JS), 2.5(JT)
BAS 0-3 DS CHAN BITS 59-63/PAR
23,24,25
4X5/1
2.0(KR)
PP RECONFIG BITS 61-63
20
3
BIT 63
2.3(JC,JU)
BITS 61,62
2.0(KB), 2.4(JQ)
PP RECONFIG BITS 59,60
20
2
2.0(JW), 2.4(JQ), 2.5(JT)
LDS STATUS BIT, Z80 EMPTY TO MAC, HOLD FCTN ON CHAN 17, Z80 CONNECT TO RI, Z80 NEXT FULL IS FCTN, Z80 DISCONNECTS RI, Z80 ACT, Z80 INACT
15,20
8
2.4(JQ)
Z80/RI BITS 56-63/PAR
15
8/1
2.4(JQ)
20
ENBL UNCOND IDLE
2.5(JT), 2.8(JT)
DEADSTART SEQ IN PROGRESS, LDS PART 2
20
2
2.3(JF)
ERROR IN CHAN 15, TPM FULL, TPM EMPTY, TPM INACT
17,22
4
Z80/CHAN 15 DATA BITS 48-63/PAR
14
16/1
21,22
4.096 µSEC, CHAN 15 FULLOUT, CHAN 15 EMPTY OUT, CHAN 15 FCTN OUT, CHAN 15 ACT OUT, CHAN 15 INACT OUT, CHAN 15 FULL STATUS, CHAN 15 ACT STATUS
8
4,17
16/1
17
4
4
CHAN n FULL IN (EVEN CHAN), CHAN n EMPTY IN (EVEN CHAN), CHAN n ACTIVE IN (EVEN CHAN), CHAN n INACTIVE IN (EVEN CHAN)
4X11
8/15
CHAN n+1 FULL IN (ODD CHAN), CHAN n+1 EMPTY IN (ODD CHAN), CHAN n+1 ACTIVE IN (ODD CHAN), CHAN n+1 INACTIVE IN (ODD CHAN)
4X12
8/15
INP CABLING
CHAN n BITS 52-63/PAR (EVEN CHAN)
11X12/1
8/15
CHAN n+1 BITS 52-63/PAR (ODD CHAN)
12X12/1
8/15
JL B21 CHAN 0,1 BAS 0-3
B20 CHAN 2,3 BAS 0-3
B19 CHAN 4,5 BAS 0-3
B18 CHAN 6,7 BAS 0-3
B17 CHAN NU,11 BAS 0-3
B16 CHAN 12,13 BAS 0-3
B07 CHAN 20,21 BAS 0-3
B06 CHAN 22,23 BAS 0-3
B05 CHAN 24,25 BAS 0-3
B04 CHAN 26,27 BAS 0-3
B03 CHAN 30,31 BAS 0-3
JL B02 CHAN 32,33 BAS 0-3
ITO CHAN
FCTN L4 SHEET
BAS 0-3 CHAN SEL MUX (2-5)
BAS 0-3 DATA INVERTERS (2-5)
EVEN/ODD CHAN BAS DATA MUX BITS 48-63/PAR (6,7/13,14)
EVEN/ODD CHAN DATA RCVRS (8/15)
EVEN/ODD CHAN INP DATA DESKEW RGTR (8/15)
EVEN/ODD CHAN CONT SIGNAL RCVRS (8/15)
EVEN/ODD CHAN INT/EXT SEL MUX (9/16)
EVEN/ODD CHAN DATA HLDG RGTR (9/16)
EVEN/ODD CHAN FCTN & PAR XMTRS (10/17)
EVEN/ODD CHAN DATA XMTRS (10/17)
EVEN/ODD CHAN CONT SIGNAL XMTR (11/18)
EVEN/ODD CHAN PAR CK & REGEN (11/18)
EVEN/ODD CHAN CONT (12/19)
CHAN STATUS MUX (20)
µCODE BFRS (21)
MAC DATA MUX (22)
CHAN TYPE SEL (22)
MAC INTERFACE (22)
CLK F/0 (23)
CLK XMTRS (23)
BAS 0-3 CHAN 0-13 STATUS: FULL, ACT, ERROR, FLAG
20
4X4
BAS 0-3 CHAN 0-13 DATA 48-63/PAR
2-5
4X16/1
BAS 0-3 CHAN 14-33 DATA 48-63/PAR
2-5
4X16/1
BAS 0-3 CHAN 14-33 STATUS: FULL, ACT, ERROR, FLAG
20
4X4
BAS 0-3 CHAN 14-33 DATA 48-63/PAR
4X16/1
20,21,22,23
2.0(JW)
BAS 0-3 CHAN 14-33 STATUS: FULL, ACT, ERROR, FLAG
4X4
18,19
2.0(JW)
CHAN n DATA OUT 52-63/PAR (EVEN CHAN)
10-17
11X12/1
CHAN n FULL OUT, ACT OUT, EMPTY OUT, INACT OUT, PAR OUT, FCTN OUT (EVEN CHAN)
11/18,10/17
11X6
CHAN n+1 DATA OUT 52-63/PAR (ODD CHAN)
10/17
12X12/1
OUT CABLING
CHAN n+1 FULL OUT, ACT OUT, EMPTY OUT, INACT OUT, PAR OUT, FCTN OUT (ODD CHAN)
11/18,10/17
12X6
MAC DATA AT B02-B07, B16-B21
22
12
2.4(JQ)
CHAN n, n+1 INSTALLED (0/1, 2/3, 4/5, 6/7, 11, 12/13, 20/21, 22/23, 24/25, 26/27, 30/31, 32/33)
23
12
2.4(JS)
CHAN TYPE 0-3
22
4
2.4(JS)
CHAN n PAR ERROR (0-7, 11-13, 20-27, 30-33)
11/18
23
2.5(JT)
CHAN 0-7, 11-13, 20-27, 30-33 SEL
2.5(JT)
23
22
LOAD, READ
2.4(JQ)
2
22
PPM 0-3 CHAN SEL n (EVEN CHAN)
2.0(KB)
4X11
12/19
PPM 0-3 CHAN SEL n+1 (ODD CHAN)
2.0(KB)
4X12
12/19
JW 0-3 µCODE BITS T3-T5
2.0(JW)
4X3
21
JW 0-3 FLAG (µCODE BIT 05)
2.0(JW)
4
21
NO-7,11-13,20-27,30-33 MC
2.5(JT)
23
23
CLR LED
2.4(JQ)
21
JM B01
UTILITY CHAN 14,15,17
FCTN L4 SHEET
µCODE BITS T3-T5 RANK 4 (2)
CHAN 15 µCODE DCDR (2)
CHAN 15 µCODE XLTRS (3)
CHAN 15 FLAG RGTR (4)
CHAN 15 DATA INP MUX BITS 48-63/P (5,6)
CHAN 15 DATA HLDG RGTR (7)
CHAN 15 OUT DRIVERS (7)
CHAN 15 PAR CHECKER & REGEN (7)
CHAN 17 µCODE DCDR (8)
CHAN 17 µCODE XLTR (9)
CHAN 17 FLAG RGTR (10)
CHAN 17 DATA INP MUX BITS 48-63/PAR (11,12)
CHAN 17 DATA HLDG RGTR (13)
CHAN 17 OUT DRIVERS (13)
CHAN 17 PAR CHECKER & REGEN (13)
BAS 0-3, C 0,1 CHAN SEL DCDR (14,15)
CHAN 15 FLAG DCDR (16)
CHAN 17 FLAG DCDR (16)
REAL TIME CLK (17)
TI CLK F/0 (17)
BAS 0-3, C 0,1 STATUS DRIVERS (18,19)
BAS 0 DATA BUS DRIVERS (20)
BAS 1 DATA BUS DRIVERS (21)
BAS 2 DATA BUS DRIVERS (22)
BAS 3 DATA BUS DRIVERS (23)
BAS C0 DATA BUS DRIVERS (24)
BAS C1 DATA BUS DRIVERS (25)
ERROR LED (26)
MAC INTERFACE (26)
A
DEADSTART MC
17
JWC 0,1, JW 0-3 µCODE BITS T3-T5
2.6(JW),2.0(JW)
6X3
2
JWC 0,1, JW 0-3 FLAG (µCODE BIT 05)
2.6(JW),2.0(JW)
6
16
PPMC 0,1, PPM 0-3 CHAN 15 OR 14 SEL, PPMC 0,1, PPM 0-3 CHAN 14 OR 17 SEL
2.6(KB),2.0(KB)
6X2
14,15
MAC FULL, MAC EMPTY, MAC INACTIVE, RI/MCH ERROR
2.4(JQ)
4
10
LOAD, READ
2.4(JQ)
2
26
CLR LED
2.4(JQ)
26
CHAN 17 PAR ERROR
2.5(JT)
CHAN 17 PAR ERROR, CHAN 17 FULL, CHAN 17 EMPTY, CHAN 17 ACT, CHAN INACT, CHAN 17 FCTN
10
6
2.4(JQ)
CHAN 17 RI DATA BITS 56-63/PAR
13
8/1
2.4(JQ)
CHAN 17 RI DATA BITS 52-55
13
4
2.4(JQ)
CHAN 15 PAR ERROR
4
2.5(JT)
MAC DATA AT B01
26
2.4(JQ)
BASC 0,1 CHAN 15,17 STATUS: FULL, ACT, ERROR, FLAG
18,19
2X4
2.6(JW)
BASC 0,1 CHAN 15,17 DATA 48-63/PAR
24,25
2X16/1
2.6(JW)

NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A AND B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0,1, JWC 0,1, PPMC 0,1 OR KBC 0,1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C AND D PANELS).
2. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAM. THE NUMBERS ON THE OUTSIDE EDGES OF THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.
3. HEAVIER LINES INDICATE MAJOR DATA OR ADDRESS PATHS.

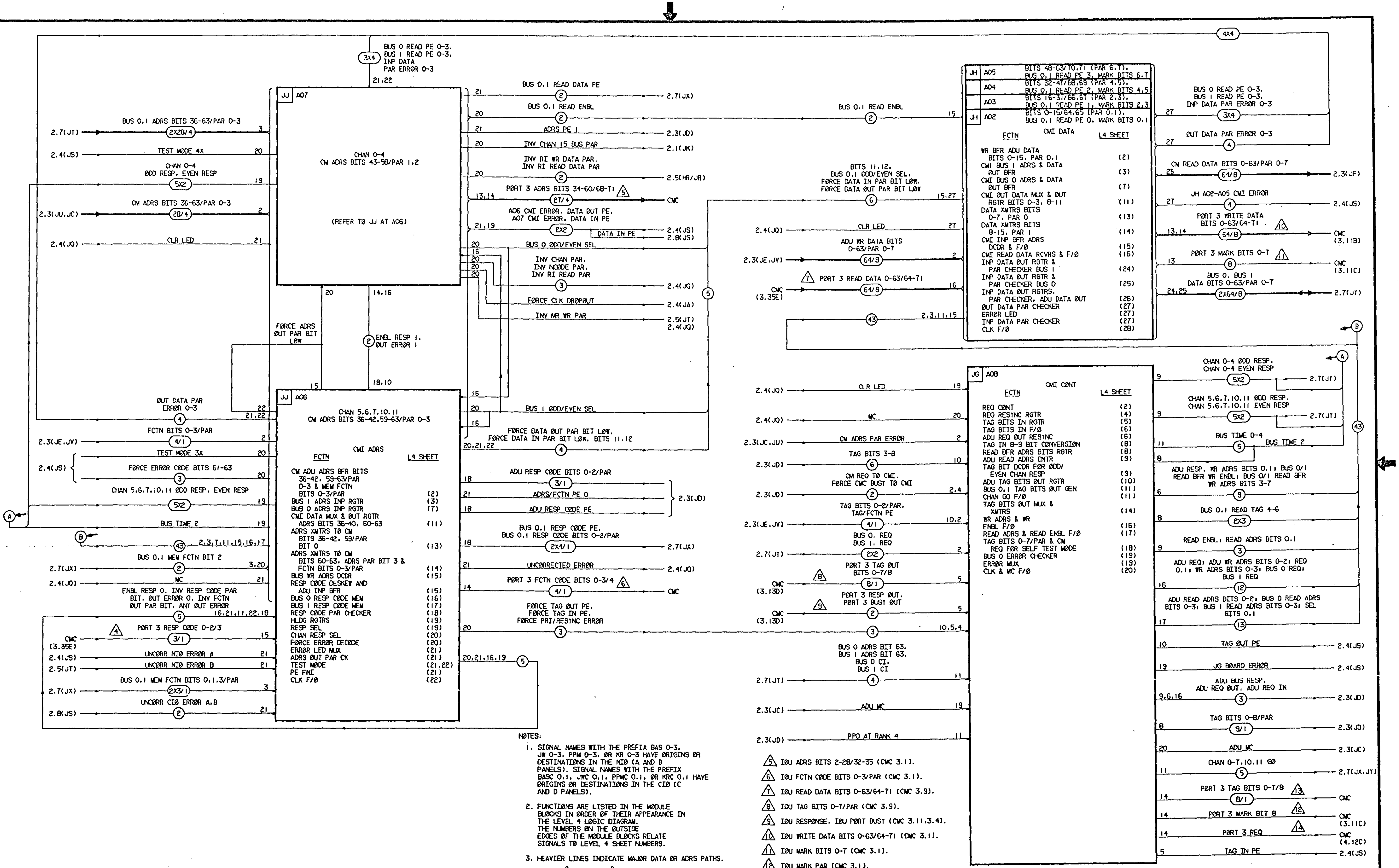
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
BAS 0-3, PPM 0-3
60463540 H
IOU 2.1


CQ B22 DISPLAY CONTROLLER
FCTN L4 SHEET
ASCII TO DISPLAY CODE CONV & ADRS F/0 (2)
UNBLANK ROW AND ROW ENBL DCDR (3)
BEAM MOVEMENT ROWS FOR DISPLAY CODE 20-57 CHAR (4)
BEAM MOVEMENT ROWS FOR DISPLAY CODE 0-17 CHAR (5)
CHAR PAINTER - HORIZONTAL MOVEMENT GEN (6)
CHAR PAINTER - VERTICAL MOVEMENT GEN (7)
KEYBOARD BFR (8)
DISPLAY CODE TO ASCII CONV (9)
CHAN 10 CONT MACROCELL (10)
CHAN 10 PAR CHECKER (11)
DISPLAY CONTROLLER INP MUX (11)
DISPLAY CONTROLLER FCTN MUX (12)
S RGTR & CHAR CODE SEL MUX (13)
Y RGTR (14)
X RGTR & INCREMENTER (15)
DISPLAY CONTROLLER STATUS FF'S (16)
TIMING CHAIN CNTRS (17)
CHAN 10 INP MUX & CONTS (18)
CHAN 10 INP MUX & DATA RGTR (19)
BAS 0, 1 BUS DRIVERS (20)
BAS 2, 3 BUS DRIVERS (21)
CHAN CONTS (22)
CHAN CONTS (23)
IOU CLK TUNING (24)
IOU CLK SECOND STAGE F/0 (25)
Z80 DATA BITS 56-63
Z80 FULL, Z80 MED CHAR SEL, Z80 SEL CC545, KEYBOARD SEL, HOLD FCTN ON CHAN 10, DEADSTART MC
JW 0-3 FLAG (μCODE BITS 73-75)
JW 0-3 FLAG (μCODE BIT 85)
PPM 0-3 CHAN 10 SEL
FIRST STAGE TI CLK, 1 MHz CLK
KEYBOARD DATA 58-63, KEY DOWN, KEY UP, DS BUTTON
FROM KEYBOARD
LEFT SCREEN SEL, MED CHAR SEL, SML CHAR SEL, ASTIG, Y DATA 56-63, X DATA 55-63
TO KEYBOARD/DISPLAY
CC545 DATA BITS 56-63
DEADSTART BUTTON
CHAN 10 FULL, ACTIVE, FLAG, ERROR FLAG
RIGHT UNBLANK, LEFT UNBLANK
ANALOG X, ANALOG Y
TO DISPLAY
BAS 0-3 CHAN 0-13 DATA 48-63/PAR
BAS 0-3 CHAN 0-13 STATUS: FULL, ACT, ERROR, FLAG
JL B21 B20 B19 B18 B17 B16 B07 B06 B05 B04 B03
CHAN 0,1 BAS 0-3; CHAN 2,3 BAS 0-3; CHAN 4,5 BAS 0-3; CHAN 6,7 BAS 0-3; CHAN 10,11 BAS 0-3; CHAN 12,13 BAS 0-3; CHAN 20,21 BAS 0-3; CHAN 22,23 BAS 0-3; CHAN 24,25 BAS 0-3; CHAN 26,27 BAS 0-3; CHAN 30,31 BAS 0-3; CHAN 32,33 BAS 0-3
CHAN n FULL IN (EVEN CHAN), CHAN n EMPTY IN (EVEN CHAN), CHAN n ACTIVE IN (EVEN CHAN), CHAN n INACTIVE IN (EVEN CHAN)
CHAN n+1 FULL IN (ODD CHAN), CHAN n+1 EMPTY IN (ODD CHAN), CHAN n+1 ACTIVE IN (ODD CHAN), CHAN n+1 INACTIVE IN (ODD CHAN)
INP CABLING
CHAN n BITS 52-63/PAR (EVEN CHAN)
CHAN n+1 BITS 52-63/PAR (ODD CHAN)
JL B02 I/O CHAN
FCTN L4 SHEET
BAS 0-3 CHAN SEL MUX (2-5)
BAS 0-3 DATA INVERTERS (2-5)
EVEN/ODD CHAN BAS DATA MUX BITS 48-63/PAR (6,7/13,14)
EVEN/ODD CHAN DATA RCVRS (8/15)
EVEN/ODD CHAN INP DATA DESKEW RGTR (8/15)
EVEN/ODD CHAN CONT SIGNAL RCVRS (8/15)
EVEN/ODD CHAN INT/EXT SEL MUX (9/16)
EVEN/ODD CHAN DATA HLDG RGTR (9/16)
EVEN/ODD CHAN FCTN & PAR XMTRS (10/17)
EVEN/ODD CHAN DATA XMTRS (10/17)
EVEN/ODD CHAN CONT SIGNAL XMTR (11/18)
EVEN/ODD CHAN PAR CK & REGEN (11/18)
EVEN/ODD CHAN CONT (12/19)
CHAN STATUS MUX (20)
μCODE BFRS (21)
MAC DATA MUX (22)
CHAN TYPE SEL (22)
MAC INTERFACE (22)
CLK F/0 (23)
CLK XMTRS (23)
CHAN 0-7, 11-13, 20-27, 30-33 SEL
LOAD, READ
PPM 0-3 CHAN SEL n (EVEN CHAN)
PPM 0-3 CHAN SEL n+1 (ODD CHAN)
JW 0-3 μCODE BITS 73-75
JW 0-3 FLAG (μCODE BIT 85)
NO-7, 11-13, 20-27, 30-33 MC
CLR LED
BAS 0-3 CHAN 14-33 DATA 48-63/PAR
BAS 0-3 CHAN 14-33 STATUS: FULL, ACT, ERROR, FLAG
CHAN n DATA OUT 52-63/PAR (EVEN CHAN)
CHAN n FULL OUT, ACT OUT, EMPTY OUT, INACT OUT, PAR OUT, FCTN OUT (EVEN CHAN)
CHAN n+1 DATA OUT 52-63/PAR (ODD CHAN)
CHAN n+1 FULL OUT, ACT OUT, EMPTY OUT, INACT OUT, PAR OUT, FCTN OUT (ODD CHAN)
OUT CABLING
MAC DATA AT B02-B07, B16-B21
CHAN n, n+1 INSTALLED (0/1, 2/3, 4/5, 6/7, 11, 12/13, 20/21, 22/23, 24/25, 26/27, 30/31, 32/33)
CHAN TYPE 0-3
CHAN n PAR ERROR (0-7, 11-13, 20-27, 30-33)
RS232 INTERFACE
JK B23 TWO PORT MUX
FCTN L4 SHEET
Z80 CPU AND BUS DRIVERS (2)
CLK OSCILLATOR (2)
BATTERY CIRCUIT (3)
Z80 AND TPM RESET (3)
ADRS DCDR (4)
SW DRIVERS (4)
EPROMS & RAM (5)
PORT 0 UART (6)
RS232 DRIVERS & RCVRS (6,7)
PORT 1 UART (7)
CAL CLK (7)
STATUS INP PORTS (8)
DATA INP PORT (9)
FCTN & DATA OUT PORTS (10)
HLDG RGTRS (11)
HLDG RGTR STROBE CONT (11)
RS232 STATUS RGTR (12)
NON RS232 DATA & PORT 0 DATA MUX (12)
TPM STATUS/DATA/MUX (13)
CHAN 15 BUS DRIVER (14)
RADIAL INTERFACE BUS DRIVERS (15)
DISPLAY CONTROLLER/RADIAL & CHAN 15 INTERFACES (16)
CHAN 15 BUS PAR CHECKER (17)
INP DATA ECL/TTL CONV (17)
CHAN 15 INP PORT FIFOS (18)
Z80 FCTN CONV & TTL DCDR (19)
SYSTEM PWR RELAY CONT (19)
Z80 FCTN DCDR (20)
TPM FCTN DCDR (21)
TPM INTERFACE CONTS (22)
PP & DS NUMBER CNTRS (23)
PAR GENS (23)
DS CHAN NUMBERS MUX (24,25)
SYSTEM POWER UP ONE-SHOT (26)
MC GEN (26)
OR TEST TIMEOUT CNTR (26)
DS OR TEST (27)
TI CLK F/0 (27)
BAS 0-3 P MATCH
NIO EC BITS 43-47
ENBL RI BUS, INACTIVE RESPONSE, RDY RESPONSE
SEL RI
PORT 0 SEL B,C,D
PORT 1 SEL B,C,D
PORT 0 BAUD SEL A,B,C
PORT 1 BAUD SEL A,B,C
SW PANEL
INV CHAN 15 BUS PAR
Z80 DATA BITS 56-63
DEADSTART MC, Z80 FULL
Z80 FULL, Z80 MED CHAR SEL, Z80 SEL CC545, KEYBOARD SEL, HOLD FCTN ON CHAN 10, DEADSTART MC
DEADSTART MC
LDS IN PROGRESS
PPO AT RANK 4
BAS 0-3 DS CHAN BITS 59-63/PAR
PP RECONFIG BITS 61-63
BIT 63
BITS 61,62
PP RECONFIG BITS 59,60
LDS STATUS BIT, Z80 EMPTY TO MAC, HOLD FCTN ON CHAN 17, Z80 CONNECT TO RI, Z80 NEXT FULL IS FCTN, Z80 DISCONNECTS RI, Z80 ACT, Z80 INACT
Z80/RI BITS 56-63/PAR
ENBL UNCOND IDLE
DEADSTART SEQ IN PROGRESS, LDS PART 2
ERROR IN CHAN 15, TPM FULL, TPM EMPTY, TPM INACT
Z80/CHAN 15 DATA BITS 48-63/PAR
4.096 μSEC, CHAN 15 FULLOUT, CHAN 15 EMPTY OUT, CHAN 15 FCTN OUT, CHAN 15 ACT OUT, CHAN 15 INACT OUT, CHAN 15 FULL STATUS, CHAN 15 ACT STATUS
JM B01 UTILITY CHAN 14,15,17
FCTN L4 SHEET
μCODE BITS 73-75 RANK 4 (2)
CHAN 15 μCODE DCDR (2)
CHAN 15 μCODE XLTRS (3)
CHAN 15 FLAG RGTR (3)
CHAN 15 DATA INP MUX BITS 48-63/P (4)
CHAN 15 DATA HLDG RGTR (5,6)
CHAN 15 OUT DRIVERS (7)
CHAN 15 PAR CHECKER & REGEN (7)
CHAN 17 μCODE DCDR (7)
CHAN 17 μCODE XLTR (8)
CHAN 17 FLAG RGTR (9)
CHAN 17 DATA INP MUX BITS 48-63/PAR (10)
CHAN 17 DATA HLDG RGTR (11,12)
CHAN 17 OUT DRIVERS (13)
CHAN 17 PAR CHECKER & REGEN (13)
BAS 0-3, C 0,1 CHAN SEL DCDR (13)
CHAN 15 FLAG DCDR (14,15)
CHAN 17 FLAG DCDR (16)
REAL TIME CLK (16)
TI CLK F/0 (17)
BAS 0-3, C 0,1 STATUS DRIVERS (17)
BAS 0 DATA BUS DRIVERS (18,19)
BAS 1 DATA BUS DRIVERS (20)
BAS 2 DATA BUS DRIVERS (21)
BAS 3 DATA BUS DRIVERS (22)
BAS C0 DATA BUS DRIVERS (23)
BAS C1 DATA BUS DRIVERS (24)
ERROR LED (25)
MAC INTERFACE (26)
DEADSTART MC
JWC 0,1, JW 0-3 μCODE BITS 73-75
JWC 0,1, JW 0-3 FLAG (μCODE BIT 85)
PPMC 0,1, PPM 0-3 CHAN 15 OR 14 SEL, PPMC 0,1, PPM 0-3 CHAN 14 OR 17 SEL
MAC FULL, MAC EMPTY, MAC INACTIVE, RI/MCH ERROR
LOAD, READ
CLR LED
CHAN 17 PAR ERROR
CHAN 17 PAR ERROR, CHAN 17 FULL, CHAN 17 EMPTY, CHAN 17 ACT, CHAN INACT, CHAN 17 FCTN
CHAN 17 RI DATA BITS 56-63/PAR
CHAN 17 RI DATA BITS 52-55
CHAN 15 PAR ERROR
MAC DATA AT B01
BASC 0,1 CHAN 15,17 STATUS: FULL, ACT, ERROR, FLAG
BASC 0,1 CHAN 15,17 DATA 48-63/PAR

NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A AND B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0,1, JWC 0,1, PPMC 0,1 OR KBC 0,1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C AND D PANELS).
2. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAM. THE NUMBERS ON THE OUTSIDE EDGES OF THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.
3. HEAVIER LINES INDICATE MAJOR DATA OR ADDRESS PATHS.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	LEVEL 2 DIAGRAM BAS 0-3, PPM 0-3	60463540	A
		IOU 2.1	


BUS 0 READ PE 0-3.
BUS 1 READ PE 0-3.
INP DATA
PAR ERROR 0-3
3X4
21.22
JJ A07
CHAN 0-4
CM ADRS BITS 43-58/PAR 1.2
(REFER TO JJ AT A06)
BUS 0.1 ADRS BITS 36-63/PAR 0-3
2X28/4
2.7(JT)
TEST MODE 4X
2.4(JS)
CHAN 0-4
ODD RESP. EVEN RESP
5X2
CM ADRS BITS 36-63/PAR 0-3
28/4
2.3(JU.JC)
CLR LED
2.4(JQ)
BUS 0.1 READ DATA PE
2.7(JX)
BUS 0.1 READ ENBL
ADRS PE 1
2.3(JD)
INV CHAN 15 BUS PAR
2.1(JK)
INV RI WR DATA PAR.
INV RI READ DATA PAR
2.5(HR/JR)
PORT 3 ADRS BITS 34-60/68-71
27/4
CMC
A06 CMI ERROR. DATA OUT PE.
A07 CMI ERROR. DATA IN PE
2X2
DATA IN PE
2.4(JS)
2.8(JS)
BUS 0 ODD/EVEN SEL
INV CHAN PAR.
INV NCODE PAR.
INV RI READ PAR
2.4(JQ)
FORCE CLK DROPOUT
2.4(JA)
INV WR WR PAR
2.5(JT)
2.4(JQ)
FORCE ADRS
OUT PAR BIT
LOW
ENBL RESP 1.
OUT ERROR 1
18.10
14.16
JJ A06
CHAN 5.6.7.10.11
CM ADRS BITS 36-42.59-63/PAR 0-3
CMI ADRS
FCTN
L4 SHEET
CM ADU ADRS BFR BITS 36-42. 59-63/PAR 0-3 & MEM FCTN BITS 0-3/PAR (2)
BUS 1 ADRS INP RGTR (3)
BUS 0 ADRS INP RGTR (7)
CMI DATA MUX & OUT RGTR ADRS BITS 36-40. 60-63 (11)
ADRS XMTRS TO CM BITS 36-42. 59/PAR BIT 0 (13)
ADRS XMTRS TO CM BITS 60-63. ADRS PAR BIT 3 & FCTN BITS 0-3/PAR (14)
BUS WR ADRS DCDR (15)
RESP CODE DESKEW AND ADU INP BFR (15)
BUS 0 RESP CODE MEM (16)
BUS 1 RESP CODE MEM (17)
RESP CODE PAR CHECKER (18)
HLDG RGTRS (19)
RESP SEL (19)
CHAN RESP SEL (20)
FORCE ERROR DECODE (20)
ERROR LED MUX (21)
ADRS OUT PAR CK (21)
TEST MODE (21.22)
PE FNI (21)
CLK F/0 (22)
OUT DATA PAR ERROR 0-3
FCTN BITS 0-3/PAR
4/1
2.3(JE.JV)
TEST MODE 3X
FORCE ERROR CODE BITS 61-63
2.4(JS)
CHAN 5.6.7.10.11 ODD RESP. EVEN RESP
BUS TIME 2
2.3.7.11.15.16.17
BUS 0.1 MEM FCTN BIT 2
2.7(JX)
MC
ENBL RESP 0. INV RESP CODE PAR BIT. OUT ERROR 0. INV FCTN OUT PAR BIT. ANT OUT ERROR
16.21.11.22.18
PORT 3 RESP CODE 0-2/3
3/1
CMC (3.35E)
UNCORR NIO ERROR A
UNCORR NIO ERROR B
2.5(JT)
BUS 0.1 MEM FCTN BITS 0.1.3/PAR
2X3/1
UNCORR CIO ERROR A.B
2.8(JS)
BUS 1 ODD/EVEN SEL
FORCE DATA OUT PAR BIT LOW.
FORCE DATA IN PAR BIT LOW. BITS 11.12
ADU RESP CODE BITS 0-2/PAR
ADRS/FCTN PE 0
ADU RESP CODE PE
2.3(JD)
BUS 0.1 RESP CODE PE.
BUS 0.1 RESP CODE BITS 0-2/PAR
2X4/1
UNCORRECTED ERROR
PORT 3 FCTN CODE BITS 0-3/4
FORCE TAG OUT PE.
FORCE TAG IN PE.
FORCE PRI/RESINC ERROR
20.21.16.19
BITS 11.12.
BUS 0.1 ODD/EVEN SEL.
FORCE DATA IN PAR BIT LOW.
FORCE DATA OUT PAR BIT LOW
CLR LED
ADU WR DATA BITS 0-63/PAR 0-7
64/8
PORT 3 READ DATA 0-63/64-71
CMC (3.35E)
2.3.11.15
JH A05 BITS 48-63/70.71 (PAR 6.7). BUS 0.1 READ PE 3. MARK BITS 6.7
A04 BITS 32-47/68.69 (PAR 4.5). BUS 0.1 READ PE 2. MARK BITS 4.5
A03 BITS 16-31/66.67 (PAR 2.3). BUS 0.1 READ PE 1. MARK BITS 2.3
JH A02 BITS 0-15/64.65 (PAR 0.1). BUS 0.1 READ PE 0. MARK BITS 0.1
CMI DATA
WR BFR ADU DATA BITS 0-15. PAR 0.1 (2)
CMI BUS 1 ADRS & DATA OUT BFR (3)
CMI BUS 0 ADRS & DATA OUT BFR (7)
CMI OUT DATA MUX & OUT RGTR BITS 0-3. 8-11 (11)
DATA XMTRS BITS 0-7. PAR 0 (13)
DATA XMTRS BITS 8-15. PAR 1 (14)
CMI INP BFR ADRS DCDR & F/0 (15)
CMI READ DATA RCVRS & F/0 (16)
INP DATA OUT RGTR & PAR CHECKER BUS 1 (24)
INP DATA OUT RGTR & PAR CHECKER BUS 0 (25)
INP DATA OUT RGTRS. PAR CHECKER. ADU DATA OUT (26)
OUT DATA PAR CHECKER (27)
ERROR LED (27)
INP DATA PAR CHECKER (27)
CLK F/0 (28)
4X4
BUS 0 READ PE 0-3.
BUS 1 READ PE 0-3.
INP DATA PAR ERROR 0-3
OUT DATA PAR ERROR 0-3
CM READ DATA BITS 0-63/PAR 0-7
2.3(JF)
JH A02-A05 CMI ERROR
PORT 3 WRITE DATA BITS 0-63/64-71
CMC (3.11B)
PORT 3 MARK BITS 0-7
CMC (3.11C)
BUS 0. BUS 1 DATA BITS 0-63/PAR 0-7
2X64/8
JG A08
CMI CONT
REQ CONT (2)
REQ RESYNC RGTR (4)
TAG BITS IN RGTR (5)
TAG BITS IN F/0 (6)
ADU REQ OUT RESYNC (6)
TAG IN 8-9 BIT CONVERSION (8)
READ BFR ADRS BITS RGTR (8)
ADU READ ADRS CNTR (9)
TAG BIT DCDR FOR ODD/EVEN CHAN RESP (9)
ADU TAG BITS OUT RGTR (10)
BUS 0.1 TAG BITS OUT GEN (11)
CHAN GO F/0 (11)
TAG BITS OUT MUX & XMTRS (14)
WR ADRS & WR ENBL F/0 (16)
READ ADRS & READ ENBL F/0 (17)
TAG BITS 0-7/PAR & CM REQ FOR SELF TEST MODE (18)
BUS 0 ERROR CHECKER (19)
ERROR MUX (19)
CLK & MC F/0 (20)
CM ADRS PAR ERROR
TAG BITS 3-8
CM REQ TO CMI.
FORCE CMC BUSY TO CMI
TAG BITS 0-2/PAR.
TAG/FCTN PE
BUS 0. REQ
BUS 1. REQ
PORT 3 TAG OUT BITS 0-7/8
8/1
PORT 3 RESP OUT.
PORT 3 BUSY OUT
CMC (3.13D)
BUS 0 ADRS BIT 63.
BUS 1 ADRS BIT 63.
BUS 0 CI.
BUS 1 CI
ADU MC
PPO AT RANK 4
CHAN 0-4 ODD RESP.
CHAN 0-4 EVEN RESP
CHAN 5.6.7.10.11 ODD RESP.
CHAN 5.6.7.10.11 EVEN RESP
2.7(JT)
BUS TIME 0-4
BUS TIME 2
ADU RESP. WR ADRS BITS 0.1. BUS 0/1 READ BFR WR ENBL. BUS 0/1 READ BFR WR ADRS BITS 3-7
BUS 0.1 READ TAG 4-6
2X3
READ ENBL. READ ADRS BITS 0.1
ADU REQ. ADU WR ADRS BITS 0-2. REQ 0.1. WR ADRS BITS 0-3. BUS 0 REQ. BUS 1 REQ
ADU READ ADRS BITS 0-2. BUS 0 READ ADRS BITS 0-3. BUS 1 READ ADRS BITS 0-3. SEL BITS 0.1
TAG OUT PE
JG BOARD ERROR
ADU BUS RESP.
ADU REQ OUT. ADU REQ IN
TAG BITS 0-8/PAR
9/1
ADU MC
2.3(JC)
CHAN 0-7.10.11 GO
2.7(JX.JT)
PORT 3 TAG BITS 0-7/8
PORT 3 MARK BIT 8
CMC (3.11C)
PORT 3 REQ
CMC (4.12C)
TAG IN PE
2.4(JS)

NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A AND B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0.1, JWC 0.1, PPMC 0.1, OR KRC 0.1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C AND D PANELS).

2. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAM. THE NUMBERS ON THE OUTSIDE EDGES OF THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.

3. HEAVIER LINES INDICATE MAJOR DATA OR ADRS PATHS.

NOTES ⚠4 THROUGH ⚠14 REFER TO MODEL 840-860 SIGNAL NAMES.

⚠4 IOU RESPONSE CODE BITS 0-2/PAR (CMC 3.9).

⚠5 IOU ADRS BITS 2-28/32-35 (CMC 3.1).

⚠6 IOU FCTN CODE BITS 0-3/PAR (CMC 3.1).

⚠7 IOU READ DATA BITS 0-63/64-71 (CMC 3.9).

⚠8 IOU TAG BITS 0-7/PAR (CMC 3.9).

⚠9 IOU RESPONSE, IOU PORT BUSY (CMC 3.11,3.4).

⚠10 IOU WRITE DATA BITS 0-63/64-71 (CMC 3.1).

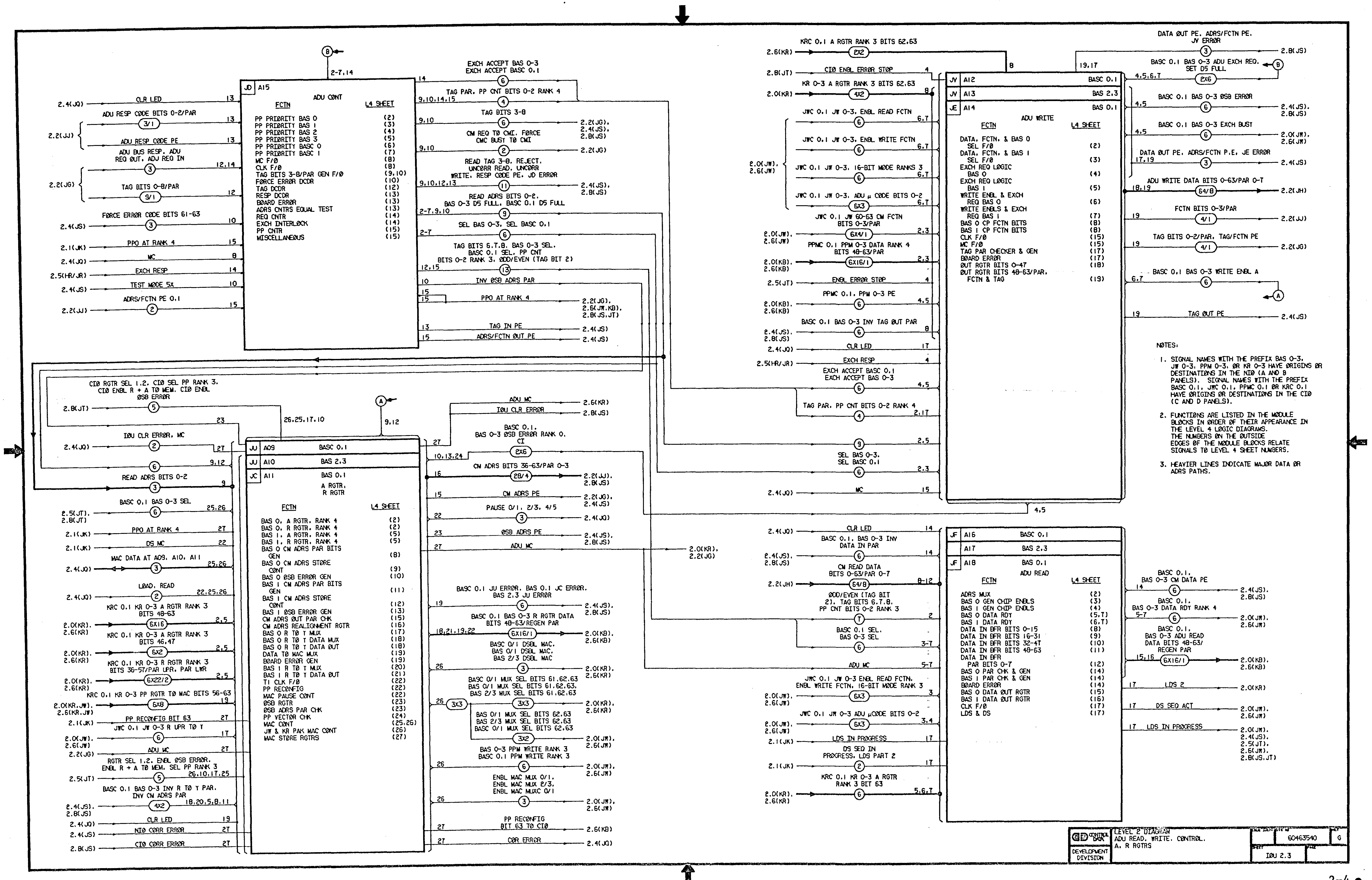
⚠11 IOU MARK BITS 0-7 (CMC 3.1).

⚠12 IOU MARK PAR (CMC 3.1).

⚠13 IOU TAG BITS 0-7/PAR (CMC 3.1).

⚠14 IOU REQ (CMC 3.1).

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
CMI ADRS.
CMI DATA.
CMI CONTROL
60463540 G
IOU 2.2



JD A15
ADU CONT
CLR LED
ADU RESP CODE BITS 0-2/PAR
ADU RESP CODE PE
ADU BUS RESP, ADU REQ OUT, ADU REQ IN
TAG BITS 0-8/PAR
FORCE ERROR CODE BITS 61-63
PPO AT RANK 4
MC
EXCH RESP
TEST MODE 5X
ADRS/FCTN PE 0,1
2.4(JQ)
2.2(JJ)
2.2(JG)
2.4(JS)
2.1(JK)
2.5(HR/JR)
2-7,14
EXCH ACCEPT BAS 0-3
EXCH ACCEPT BASC 0,1
TAG PAR, PP CNT BITS 0-2 RANK 4
TAG BITS 3-8
CM REQ TO CMI, FORCE CMC BUST TO CMI
READ TAG 3-8, REJECT, UNCORR READ, UNCORR WRITE, RESP CODE PE, JD ERROR
READ ADRS BITS 0-2, BAS 0-3 DS FULL, BASC 0,1 DS FULL
SEL BAS 0-3, SEL BASC 0,1
TAG BITS 6,7,8, BAS 0-3 SEL, BASC 0,1 SEL, PP CNT BITS 0-2 RANK 3, ODD/EVEN (TAG BIT 2)
INV OSB ADRS PAR
PPO AT RANK 4
TAG IN PE
ADRS/FCTN OUT PE
2.2(JG), 2.4(JS), 2.8(JS)
2.4(JS), 2.8(JS)
2.2(JG), 2.6(JW,KB), 2.8(JS,JT)
CIO RGTR SEL 1,2, CIO SEL PP RANK 3, CIO ENBL R + A TO MEM, CIO ENBL OSB ERROR
IOU CLR ERROR, MC
READ ADRS BITS 0-2
BASC 0,1 BAS 0-3 SEL
PPO AT RANK 4
DS MC
MAC DATA AT A09, A10, A11
LOAD, READ
KRC 0,1 KR 0-3 A RGTR RANK 3 BITS 48-63
KRC 0,1 KR 0-3 A RGTR RANK 3 BITS 46,47
KRC 0,1 KR 0-3 R RGTR RANK 3 BITS 36-57/PAR UPR, PAR LWR
KRC 0,1 KR 0-3 PP RGTR TO MAC BITS 56-63
PP RECONFIG BIT 63
JWC 0,1 JW 0-3 R UPR TO T
ADU MC
RGTR SEL 1,2, ENBL OSB ERROR, ENBL R + A TO MEM, SEL PP RANK 3
BASC 0,1 BAS 0-3 INV R TO T PAR, INV CM ADRS PAR
CLR LED
NIO CORR ERROR
CIO CORR ERROR
JU A09 BASC 0,1
JU A10 BAS 2,3
JC A11 BAS 0,1
A RGTR, R RGTR
26,25,17,10
9,12
ADU MC
IOU CLR ERROR
BASC 0,1, BAS 0-3 OSB ERROR RANK 0, CI
CM ADRS BITS 36-63/PAR 0-3
CM ADRS PE
PAUSE 0/1, 2/3, 4/5
OSB ADRS PE
ADU MC
BASC 0,1 JU ERROR, BASC 0,1 JC ERROR, BAS 2,3 JU ERROR
BASC 0,1 BAS 0-3 R RGTR DATA BITS 48-63/REGEN PAR
BASC 0/1 DSBL MAC, BAS 0/1 DSBL MAC, BAS 2/3 DSBL MAC
BASC 0/1 MUX SEL BITS 61,62,63, BAS 0/1 MUX SEL BITS 61,62,63, BAS 2/3 MUX SEL BITS 61,62,63
BAS 0/1 MUX SEL BITS 62,63, BAS 2/3 MUX SEL BITS 62,63, BASC 0/1 MUX SEL BITS 62,63
BAS 0-3 PPM WRITE RANK 3, BASC 0,1 PPM WRITE RANK 3
ENBL MAC MUX 0/1, ENBL MAC MUX 2/3, ENBL MAC MUXC 0/1
PP RECONFIG BIT 63 TO CIO
COR ERROR
2.0(KR), 2.2(JG)
2.6(KR)
2.8(JS)
2.0(KR), 2.6(KB)
2.0(KR), 2.6(KR)
2.0(JW), 2.6(JW)
2.6(KB)
2.4(JQ)
KRC 0,1 A RGTR RANK 3 BITS 62,63
CIO ENBL ERROR STOP
KR 0-3 A RGTR RANK 3 BITS 62,63
JWC 0,1 JW 0-3, ENBL READ FCTN
JWC 0,1 JW 0-3, ENBL WRITE FCTN
JWC 0,1 JW 0-3, 16-BIT MODE RANKS 3
JWC 0,1 JW 0-3, ADU μ CODE BITS 0-2
JWC 0,1 JW 60-63 CM FCTN BITS 0-3/PAR
PPMC 0,1 PPM 0-3 DATA RANK 4 BITS 48-63/PAR
ENBL ERROR STOP
PPMC 0,1, PPM 0-3 PE
BASC 0,1 BAS 0-3 INV TAG OUT PAR
CLR LED
EXCH RESP
EXCH ACCEPT BASC 0,1, EXCH ACCEPT BAS 0-3
TAG PAR, PP CNT BITS 0-2 RANK 4
SEL BAS 0-3, SEL BASC 0,1
MC
2.6(KR)
2.8(JT)
2.0(KR)
2.0(JW), 2.6(JW)
2.0(KB), 2.6(KB)
2.5(JT)
2.4(JS), 2.8(JS)
2.5(HR/JR)
JY A12 BASC 0,1
JY A13 BAS 2,3
JE A14 BAS 0,1
ADU WRITE
DATA OUT PE, ADRS/FCTN PE, JY ERROR
BASC 0,1 BAS 0-3 ADU EXCH REQ, SET DS FULL
BASC 0,1 BAS 0-3 OSB ERROR
BASC 0,1 BAS 0-3 EXCH BUST
DATA OUT PE, ADRS/FCTN P.E, JE ERROR
ADU WRITE DATA BITS 0-63/PAR 0-7
FCTN BITS 0-3/PAR
TAG BITS 0-2/PAR, TAG/FCTN PE
BASC 0,1 BAS 0-3 WRITE ENBL A
TAG OUT PE
2.8(JS)
2.4(JS), 2.8(JS)
2.0(JW), 2.6(JW)
2.4(JS)
2.2(JH)
2.2(JJ)
2.2(JG)
CLR LED
BASC 0,1, BAS 0-3 INV DATA IN PAR
CM READ DATA BITS 0-63/PAR 0-7
ODD/EVEN (TAG BIT 2), TAG BITS 6,7,8, PP CNT BITS 0-2 RANK 3
BASC 0,1 SEL, BAS 0-3 SEL
ADU MC
JWC 0,1 JW 0-3 ENBL READ FCTN, ENBL WRITE FCTN, 16-BIT MODE RANK 3
JWC 0,1 JW 0-3 ADU μCODE BITS 0-2
LDS IN PROGRESS
DS SEQ IN PROGRESS, LDS PART 2
KRC 0,1 KR 0-3 A RGTR RANK 3 BIT 63
2.2(JH)
2.1(JK)
JF A16 BASC 0,1
A17 BAS 2,3
JF A18 BAS 0,1
ADU READ
BASC 0,1, BAS 0-3 CM DATA PE
BASC 0,1, BAS 0-3 DATA RDY RANK 4
BASC 0,1, BAS 0-3 ADU READ DATA BITS 48-63/REGEN PAR
LDS 2
DS SEQ ACT
LDS IN PROGRESS
2.0(KB), 2.6(KB)
2.0(KR)
2.0(JW), 2.4(JS), 2.5(JT), 2.6(JW), 2.8(JS,JT)

FCTN	L4 SHEET
PP PRIORITY BAS 0	(2)
PP PRIORITY BAS 1	(3)
PP PRIORITY BAS 2	(4)
PP PRIORITY BAS 3	(5)
PP PRIORITY BASC 0	(6)
PP PRIORITY BASC 1	(7)
MC F/O	(8)
CLK F/O	(8)
TAG BITS 3-8/PAR GEN F/O	(9,10)
FORCE ERROR DCDR	(10)
TAG DCDR	(12)
RESP DCDR	(13)
BOARD ERROR	(13)
ADRS CNTRS EQUAL TEST	(13)
REQ CNTR	(14)
EXCH INTERLOCK	(14)
PP CNTR	(15)
MISCELLANEOUS	(15)

FCTN	L4 SHEET
BAS 0, A RGTR, RANK 4	(2)
BAS 0, R RGTR, RANK 4	(2)
BAS 1, A RGTR, RANK 4	(5)
BAS 1, R RGTR, RANK 4	(5)
BAS 0 CM ADRS PAR BITS GEN	(8)
BAS 0 CM ADRS STORE CONT	(9)
BAS 0 OSB ERROR GEN	(10)
BAS 1 CM ADRS PAR BITS GEN	(11)
BAS 1 CM ADRS STORE CONT	(12)
BAS 1 OSB ERROR GEN	(13)
CM ADRS OUT PAR CHK	(15)
CM ADRS REALIGNMENT RGTR	(16)
BAS 0 R TO T MUX	(17)
BAS 0 R TO T DATA MUX	(18)
BAS 0 R TO T DATA OUT	(18)
DATA TO MAC MUX	(19)
BOARD ERROR GEN	(19)
BAS 1 R TO T MUX	(20)
BAS 1 R TO T DATA OUT	(21)
TI CLK F/O	(22)
PP RECONFIG	(22)
MAC PAUSE CONT	(22)
OSB RGTR	(23)
OSB ADRS PAR CHK	(23)
PP VECTOR CHK	(24)
MAC CONT	(25,26)
JW & KR PAK MAC CONT	(26)
MAC STORE RGTRS	(27)

FCTN	L4 SHEET
DATA, FCTN, & BAS 0 SEL F/O	(2)
DATA, FCTN, & BAS 1 SEL F/O	(3)
EXCH REQ LOGIC BAS 0	(4)
EXCH REQ LOGIC BAS 1	(5)
WRITE ENBL & EXCH REQ BAS 0	(6)
WRITE ENBLS & EXCH REQ BAS 1	(7)
BAS 0 CP FCTN BITS	(8)
BAS 1 CP FCTN BITS	(8)
CLK F/O	(15)
MC F/O	(15)
TAG PAR CHECKER & GEN	(17)
BOARD ERROR	(17)
OUT RGTR BITS 0-47	(18)
OUT RGTR BITS 48-63/PAR, FCTN & TAG	(19)

FCTN	L4 SHEET
ADRS MUX	(2)
BAS 0 GEN CHIP ENBLS	(3)
BAS 1 GEN CHIP ENBLS	(4)
BAS 0 DATA RDY	(5,7)
BAS 1 DATA RDY	(6,7)
DATA IN BFR BITS 0-15	(8)
DATA IN BFR BITS 16-31	(9)
DATA IN BFR BITS 32-47	(10)
DATA IN BFR BITS 48-63	(11)
DATA IN BFR PAR BITS 0-7	(12)
BAS 0 PAR CHK & GEN	(14)
BAS 1 PAR CHK & GEN	(14)
BOARD ERROR	(14)
BAS 0 DATA OUT RGTR	(15)
BAS 1 DATA OUT RGTR	(16)
CLK F/O	(17)
LDS & DS	(17)

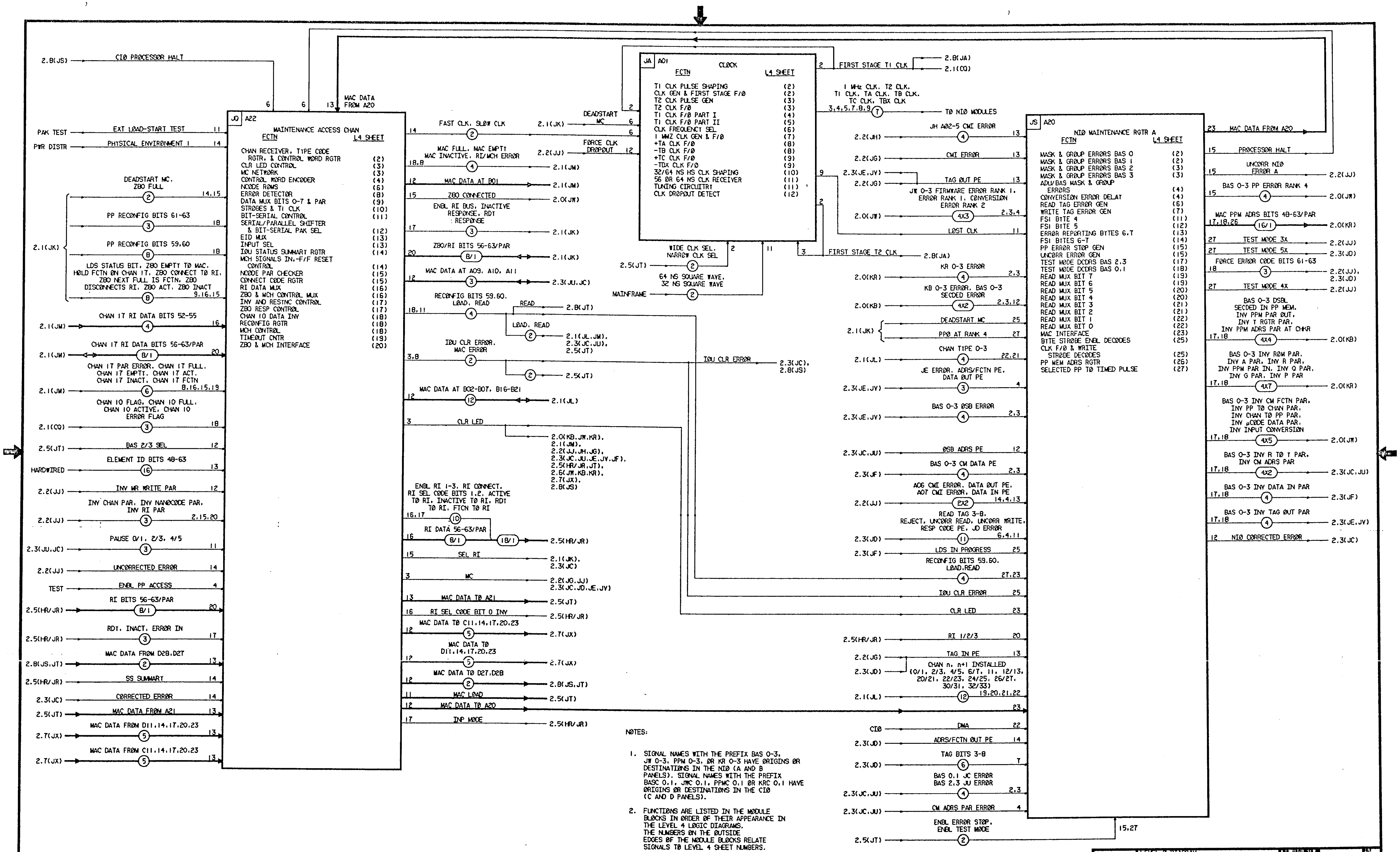
NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A AND B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0,1, JWC 0,1, PPMC 0,1 OR KRC 0,1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C AND D PANELS).

2. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAMS. THE NUMBERS ON THE OUTSIDE EDGES OF THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.

3. HEAVIER LINES INDICATE MAJOR DATA OR ADRS PATHS.

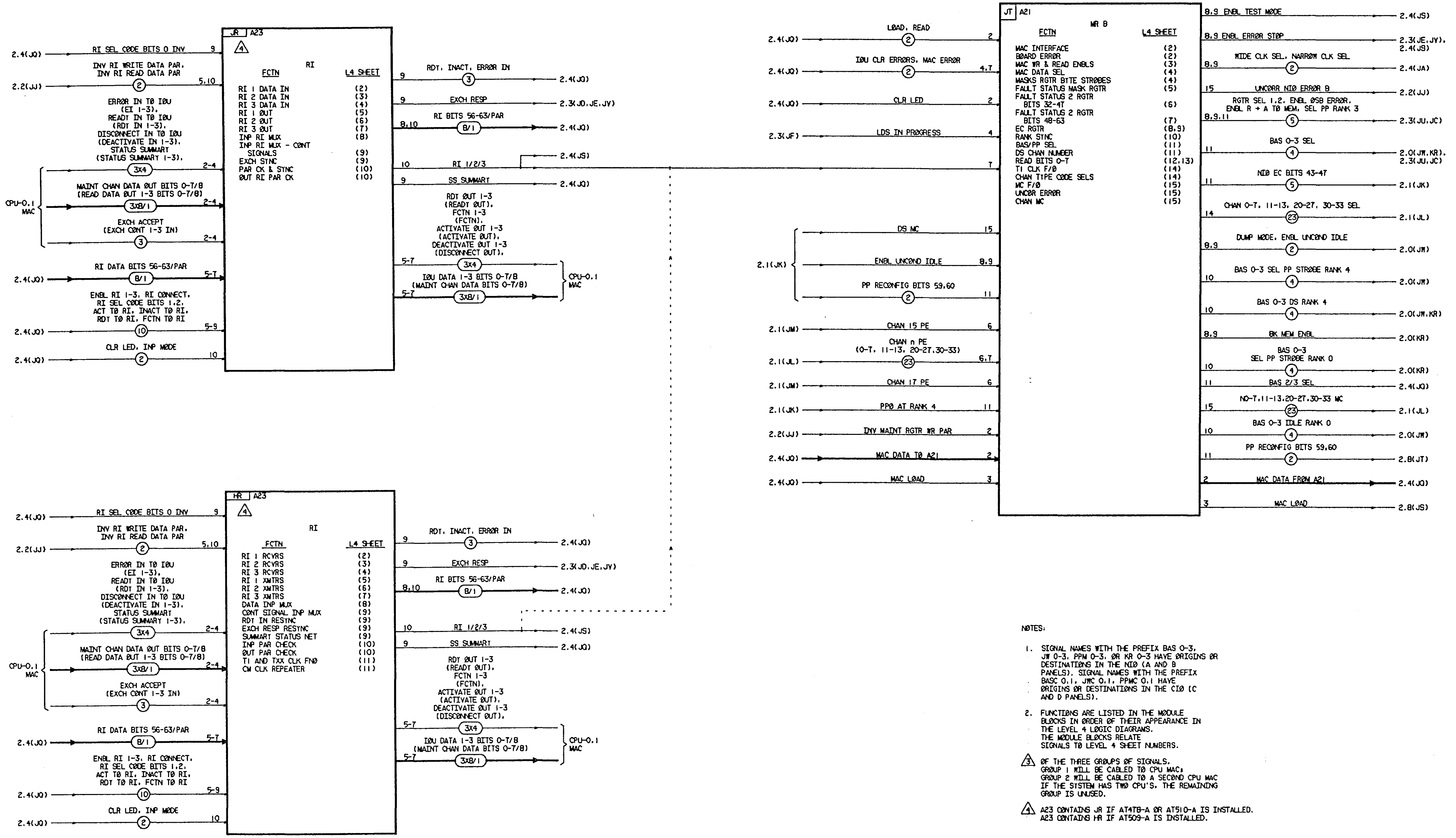
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
ADU READ, WRITE, CONTROL,
A, R RGTRS
60463540 G
IOU 2.3


JQ A22
MAINTENANCE ACCESS CHAN
FCTN
L4 SHEET
CHAN RECEIVER, TYPE CODE RGTR, & CONTROL WORD RGTR (2)
CLR LED CONTROL (3)
MC NETWORK (3)
CONTROL WORD ENCODER (4)
NCODE ROWS (6)
ERROR DETECTOR (8)
DATA MUX BITS 0-7 & PAR (9)
STROBES & TI CLK (10)
BIT-SERIAL CONTROL (11)
SERIAL/PARALLEL SHIFTER & BIT-SERIAL PAK SEL (12)
EID MUX (13)
INPUT SEL (13)
IOU STATUS SUMMARY RGTR (14)
MCH SIGNALS IN,-F/F RESET CONTROL (14)
NCODE PAR CHECKER (15)
CONNECT CODE RGTR (15)
RI DATA MUX (16)
ZBO & MCH CONTROL MUX (16)
INV AND RESTNC CONTROL (17)
ZBO RESP CONTROL (17)
CHAN 10 DATA INV (18)
RECONFIG RGTR (18)
MCH CONTROL (18)
TIMEOUT CNTR (19)
ZBO & MCH INTERFACE (20)
JA A01
CLOCK
FCTN
L4 SHEET
TI CLK PULSE SHAPING (2)
CLK GEN & FIRST STAGE F/0 (2)
T2 CLK PULSE GEN (3)
T2 CLK F/0 (3)
TI CLK F/0 PART I (4)
TI CLK F/0 PART II (5)
CLK FREQUENCY SEL (6)
1 MHZ CLK GEN & F/0 (7)
+TA CLK F/0 (8)
-TB CLK F/0 (8)
+TC CLK F/0 (9)
-TDX CLK F/0 (9)
32/64 NS HS CLK SHAPING (10)
56 OR 64 NS CLK RECEIVER (11)
TUNING CIRCUITRY (11)
CLK DROPOUT DETECT (12)
JS A20
NIO MAINTENANCE RGTR A
FCTN
L4 SHEET
MASK & GROUP ERRORS BAS 0 (2)
MASK & GROUP ERRORS BAS 1 (2)
MASK & GROUP ERRORS BAS 2 (3)
MASK & GROUP ERRORS BAS 3 (3)
ADU/BAS MASK & GROUP ERRORS (4)
CONVERSION ERROR DELAY (4)
READ TAG ERROR GEN (6)
WRITE TAG ERROR GEN (7)
FSI BYTE 4 (11)
FSI BYTE 5 (12)
ERROR REPORTING BYTES 6,7 (13)
FSI BYTES 6-7 (14)
PP ERROR STOP GEN (15)
UNCORR ERROR GEN (15)
TEST MODE DCDRS BAS 2,3 (17)
TEST MODE DCDRS BAS 0,1 (18)
READ MUX BIT 7 (19)
READ MUX BIT 6 (19)
READ MUX BIT 5 (20)
READ MUX BIT 4 (20)
READ MUX BIT 3 (21)
READ MUX BIT 2 (21)
READ MUX BIT 1 (22)
READ MUX BIT 0 (22)
MAC INTERFACE (23)
BITE STROBE ENBL DECODES (25)
CLK F/0 & WRITE STROBE DECODES (25)
PP MEM ADRS RGTR (26)
SELECTED PP TO TIMED PULSE (27)
2.8(JS) CIO PROCESSOR HALT
PAK TEST EXT LOAD-START TEST 11
PWR DISTR PHYSICAL ENVIRONMENT I 14
DEADSTART MC, ZBO FULL 14,15
PP RECONFIG BITS 61-63 18
2.1(JK) PP RECONFIG BITS 59,60 18
LDS STATUS BIT, ZBO EMPTY TO MAC, HOLD FCTN ON CHAN 17, ZBO CONNECT TO RI, ZBO NEXT FULL IS FCTN, ZBO DISCONNECTS RI, ZBO ACT, ZBO INACT 9,16,15
2.1(JM) CHAN 17 RI DATA BITS 52-55 16
2.1(JM) CHAN 17 RI DATA BITS 56-63/PAR 20
2.1(JM) CHAN 17 PAR ERROR, CHAN 17 FULL, CHAN 17 EMPTY, CHAN 17 ACT, CHAN 17 INACT, CHAN 17 FCTN 8,16,15,19
2.1(CQ) CHAN 10 FLAG, CHAN 10 FULL, CHAN 10 ACTIVE, CHAN 10 ERROR FLAG 18
2.5(JT) BAS 2/3 SEL 12
HARDWIRED ELEMENT ID BITS 48-63 13
2.2(JJ) INV WR WRITE PAR 12
2.2(JJ) INV CHAN PAR, INV NANOCODE PAR, INV RI PAR 2,15,20
2.3(JU,JC) PAUSE 0/1, 2/3, 4/5 11
2.2(JJ) UNCORRECTED ERROR 14
TEST ENBL PP ACCESS 4
2.5(HR/JR) RI BITS 56-63/PAR 20
2.5(HR/JR) RDT, INACT, ERROR IN 17
2.8(JS,JT) MAC DATA FROM D28,D27 13
2.5(HR/JR) SS SUMMART 14
2.3(JC) CORRECTED ERROR 14
2.5(JT) MAC DATA FROM A21 13
2.7(JX) MAC DATA FROM D11,14,17,20,23 13
2.7(JX) MAC DATA FROM C11,14,17,20,23 13
MAC DATA FROM A20
FAST CLK, SLOW CLK 2.1(JK)
MAC FULL, MAC EMPTY MAC INACTIVE, RI/MCH ERROR 2.2(JJ) 2.1(JM)
MAC DATA AT B01 2.1(JM)
ZBO CONNECTED 2.0(JW)
ENBL RI BUS, INACTIVE RESPONSE, RDT RESPONSE 2.1(JK)
ZBO/RI BITS 56-63/PAR 2.1(JK)
MAC DATA AT A09, A10, A11 2.3(JU,JC)
RECONFIG BITS 59,60, LOAD, READ
READ 2.8(JT)
LOAD, READ 2.1(JL,JM), 2.3(JC,JU), 2.5(JT)
IOU CLR ERROR, MAC ERROR
IOU CLR ERROR 2.3(JC), 2.8(JS)
2.5(JT)
MAC DATA AT B02-B07, B16-B21 2.1(JL)
CLR LED 2.0(KB,JW,KR), 2.1(JM), 2.2(JJ,JH,JG), 2.3(JC,JU,JE,JY,JF), 2.5(HR/JR,JT), 2.6(JW,KB,KR), 2.7(JX), 2.8(JS)
ENBL RI 1-3, RI CONNECT, RI SEL CODE BITS 1,2, ACTIVE TO RI, INACTIVE TO RI, RDT TO RI, FTCN TO RI
RI DATA 56-63/PAR 2.5(HR/JR)
SEL RI 2.1(JK), 2.3(JC)
MC 2.2(JG,JJ) 2.3(JC,JD,JE,JY)
MAC DATA TO A21 2.5(JT)
RI SEL CODE BIT 0 INV 2.5(HR/JR)
MAC DATA TO C11,14,17,20,23 2.7(JX)
MAC DATA TO D11,14,17,20,23 2.7(JX)
MAC DATA TO D27,D28 2.8(JS,JT)
MAC LOAD 2.5(JT)
MAC DATA TO A20
INP MODE 2.5(HR/JR)
DEADSTART MC
FORCE CLK DROPOUT
2.5(JT) WIDE CLK SEL, NARROW CLK SEL
64 NS SQUARE WAVE, 32 NS SQUARE WAVE
MAINFRAME
FIRST STAGE TI CLK 2.8(JA) 2.1(CQ)
1 MHz CLK, T2 CLK, TI CLK, TA CLK, TB CLK, TC CLK, TBX CLK 3,4,5,7,8,9 TO NIO MODULES
FIRST STAGE T2 CLK 2.8(JA)
2.2(JH) JH A02-5 CWI ERROR 13
2.2(JG) CWI ERROR 13
2.3(JE,JY) 2.2(JG) TAG OUT PE 13
2.0(JW) JW 0-3 FIRMWARE ERROR RANK 1, ERROR RANK 1, CONVERSION ERROR RANK 2 2,3,4
LOST CLK 11
2.0(KR) KR 0-3 ERROR 2,3
2.0(KB) KB 0-3 ERROR, BAS 0-3 SECDED ERROR 2,3,12
2.1(JK) DEADSTART MC 25
PPO AT RANK 4 27
2.1(JL) CHAN TYPE 0-3 22,21
2.3(JE,JY) JE ERROR, ADRS/FCTN PE, DATA OUT PE 4
2.3(JE,JY) BAS 0-3 OSB ERROR 2,3
2.3(JC,JU) OSB ADRS PE 12
2.3(JF) BAS 0-3 CM DATA PE 2,3
2.2(JJ) A06 CWI ERROR, DATA OUT PE, A07 CWI ERROR, DATA IN PE 14,4,13
2.3(JD) READ TAG 3-8, REJECT, UNCORR READ, UNCORR WRITE, RESP CODE PE, JD ERROR 6,4,11
2.3(JF) LDS IN PROGRESS 25
RECONFIG BITS 59,60, LOAD,READ 27,23
IOU CLR ERROR 25
CLR LED 23
2.5(HR/JR) RI 1/2/3 20
2.2(JG) TAG IN PE 13
2.3(JD) 2.1(JL) CHAN n, n+1 INSTALLED (0/1, 2/3, 4/5, 6/7, 11, 12/13, 20/21, 22/23, 24/25, 26/27, 30/31, 32/33) 19,20,21,22
23
CIO DMA 22
2.3(JD) ADRS/FCTN OUT PE 14
2.3(JD) TAG BITS 3-8 7
2.3(JC,JU) BAS 0,1 JC ERROR BAS 2,3 JU ERROR 2,3
2.3(JC,JU) CM ADRS PAR ERROR 4
2.5(JT) ENBL ERROR STOP, ENBL TEST MODE
15,27
MAC DATA FROM A20
PROCESSOR HALT
UNCORR NIO ERROR A 2.2(JJ)
BAS 0-3 PP ERROR RANK 4 2.0(JW)
MAC PPM ADRS BITS 48-63/PAR 17,18,26 2.0(KR)
TEST MODE 3X 2.2(JJ)
TEST MODE 5X 2.3(JD)
FORCE ERROR CODE BITS 61-63 2.2(JJ), 2.3(JD)
TEST MODE 4X 2.2(JJ)
BAS 0-3 DSBL SECDED IN PP MEM, INV PPM PAR OUT, INV T RGTR PAR, INV PPM ADRS PAR AT CHKR 2.0(KB)
BAS 0-3 INV ROM PAR, INV A PAR, INV R PAR, INV PPM PAR IN, INV Q PAR, INV G PAR, INV P PAR 2.0(KR)
BAS 0-3 INV CM FCTN PAR, INV PP TO CHAN PAR, INV CHAN TO PP PAR, INV μCODE DATA PAR, INV INPUT CONVERSION 2.0(JW)
BAS 0-3 INV R TO T PAR, INV CM ADRS PAR 2.3(JC,JU)
BAS 0-3 INV DATA IN PAR 2.3(JF)
BAS 0-3 INV TAG OUT PAR 2.3(JE,JY)
NIO CORRECTED ERROR 2.3(JC)

NOTES:

1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A AND B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0,1, JWC 0,1, PPMC 0,1 OR KRC 0,1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C AND D PANELS).
2. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAMS. THE NUMBERS ON THE OUTSIDE EDGES OF THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.
3. HEAVIER LINES INDICATE MAJOR DATA OR ADDRESS PATHS.

CONTROL DATA DEVELOPMENT DIVISION	LEVEL 2 DIAGRAM MAC, MAINT RGTR A	60463540	G
		SHEET IOU 2.4	


JR A23
4
RI
FCTN
L4 SHEET
RI 1 DATA IN (2)
RI 2 DATA IN (3)
RI 3 DATA IN (4)
RI 1 OUT (5)
RI 2 OUT (6)
RI 3 OUT (7)
INP RI MUX (8)
INP RI MUX - CONT SIGNALS (9)
EXCH SYNC (9)
PAR CK & SYNC (10)
OUT RI PAR CK (10)
2.4(JQ) RI SEL CODE BITS 0 INV 9
2.2(JJ) INV RI WRITE DATA PAR, INV RI READ DATA PAR 2 5,10
ERROR IN TO IOU (EI 1-3), READY IN TO IOU (RDY IN 1-3), DISCONNECT IN TO IOU (DEACTIVATE IN 1-3), STATUS SUMMARY (STATUS SUMMARY 1-3), 3X4 2-4
MAINT CHAN DATA OUT BITS 0-7/8 (READ DATA OUT 1-3 BITS 0-7/8) 3X8/1 2-4
EXCH ACCEPT (EXCH CONT 1-3 IN) 3 2-4
CPU-0,1 MAC
2.4(JQ) RI DATA BITS 56-63/PAR 8/1 5-7
2.4(JQ) ENBL RI 1-3, RI CONNECT, RI SEL CODE BITS 1,2, ACT TO RI, INACT TO RI, RDY TO RI, FCTN TO RI 10 5-9
2.4(JQ) CLR LED, INP MODE 2 10
9 RDY, INACT, ERROR IN 3 2.4(JQ)
9 EXCH RESP 2.3(JD,JE,JY)
8,10 RI BITS 56-63/PAR 8/1 2.4(JQ)
10 RI 1/2/3 2.4(JS)
9 SS SUMMARY 2.4(JQ)
5-7 RDY OUT 1-3 (READY OUT), FCTN 1-3 (FCTN), ACTIVATE OUT 1-3 (ACTIVATE OUT), DEACTIVATE OUT 1-3 (DISCONNECT OUT), 3X4
5-7 IOU DATA 1-3 BITS 0-7/8 (MAINT CHAN DATA BITS 0-7/8) 3X8/1
CPU-0,1 MAC
HR A23
4
RI
FCTN
L4 SHEET
RI 1 RCVRS (2)
RI 2 RCVRS (3)
RI 3 RCVRS (4)
RI 1 XMTRS (5)
RI 2 XMTRS (6)
RI 3 XMTRS (7)
DATA INP MUX (8)
CONT SIGNAL INP MUX (9)
RDY IN RESYNC (9)
EXCH RESP RESYNC (9)
SUMMARY STATUS NET (9)
INP PAR CHECK (10)
OUT PAR CHECK (10)
TI AND TXX CLK FNO (11)
CM CLK REPEATER (11)
2.4(JQ) RI SEL CODE BITS 0 INV 9
2.2(JJ) INV RI WRITE DATA PAR, INV RI READ DATA PAR 2 5,10
ERROR IN TO IOU (EI 1-3), READY IN TO IOU (RDY IN 1-3), DISCONNECT IN TO IOU (DEACTIVATE IN 1-3), STATUS SUMMARY (STATUS SUMMARY 1-3), 3X4 2-4
MAINT CHAN DATA OUT BITS 0-7/8 (READ DATA OUT 1-3 BITS 0-7/8) 3X8/1 2-4
EXCH ACCEPT (EXCH CONT 1-3 IN) 3 2-4
CPU-0,1 MAC
2.4(JQ) RI DATA BITS 56-63/PAR 8/1 5-7
2.4(JQ) ENBL RI 1-3, RI CONNECT, RI SEL CODE BITS 1,2, ACT TO RI, INACT TO RI, RDY TO RI, FCTN TO RI 10 5-9
2.4(JQ) CLR LED, INP MODE 2 10
9 RDY, INACT, ERROR IN 3 2.4(JQ)
9 EXCH RESP 2.3(JD,JE,JY)
8,10 RI BITS 56-63/PAR 8/1 2.4(JQ)
10 RI 1/2/3 2.4(JS)
9 SS SUMMARY 2.4(JQ)
5-7 RDY OUT 1-3 (READY OUT), FCTN 1-3 (FCTN), ACTIVATE OUT 1-3 (ACTIVATE OUT), DEACTIVATE OUT 1-3 (DISCONNECT OUT), 3X4
5-7 IOU DATA 1-3 BITS 0-7/8 (MAINT CHAN DATA BITS 0-7/8) 3X8/1
CPU-0,1 MAC
JT A21
MR B
FCTN
L4 SHEET
MAC INTERFACE (2)
BOARD ERROR (2)
MAC WR & READ ENBLS (3)
MAC DATA SEL (4)
MASKS RGTR BYTE STROBES (4)
FAULT STATUS MASK RGTR (5)
FAULT STATUS 2 RGTR BITS 32-47 (6)
FAULT STATUS 2 RGTR BITS 48-63 (7)
EC RGTR (8,9)
RANK SYNC (10)
BAS/PP SEL (11)
DS CHAN NUMBER (11)
READ BITS 0-7 (12,13)
TI CLK F/0 (14)
CHAN TYPE CODE SELS (14)
MC F/0 (15)
UNCOR ERROR (15)
CHAN MC (15)
2.4(JQ) LOAD, READ 2 2
2.4(JQ) IOU CLR ERRORS, MAC ERROR 2 4,7
2.4(JQ) CLR LED 2
2.3(JF) LDS IN PROGRESS 4
7
2.1(JK) DS MC 15
ENBL UNCOND IDLE 8,9
PP RECONFIG BITS 59,60 2 11
2.1(JM) CHAN 15 PE 6
2.1(JL) CHAN n PE (0-7, 11-13, 20-27,30-33) 23 6,7
2.1(JM) CHAN 17 PE 6
2.1(JK) PP0 AT RANK 4 11
2.2(JJ) INV MAINT RGTR WR PAR 2
2.4(JQ) MAC DATA TO A21 2
2.4(JQ) MAC LOAD 3
8,9 ENBL TEST MODE 2.4(JS)
8,9 ENBL ERROR STOP 2.3(JE,JY), 2.4(J9)
8,9 WIDE CLK SEL, NARROW CLK SEL 2 2.4(JA)
15 UNCORR NIO ERROR B 2.2(JJ)
8,9,11 RGTR SEL 1,2, ENBL OSB ERROR, ENBL R + A TO MEM, SEL PP RANK 3 5 2.3(JU,JC)
11 BAS 0-3 SEL 4 2.0(JW,KR), 2.3(JU,JC)
11 NIO EC BITS 43-47 5 2.1(JK)
14 CHAN 0-7, 11-13, 20-27, 30-33 SEL 23 2.1(JL)
8,9 DUMP MODE, ENBL UNCOND IDLE 2 2.0(JW)
10 BAS 0-3 SEL PP STROBE RANK 4 4 2.0(JW)
10 BAS 0-3 DS RANK 4 4 2.0(JW,KR)
8,9 8K MEM ENBL 2.0(KR)
10 BAS 0-3 SEL PP STROBE RANK 0 4 2.0(KR)
11 BAS 2/3 SEL 2.4(JQ)
15 NO-7,11-13,20-27,30-33 MC 23 2.1(JL)
10 BAS 0-3 IDLE RANK 0 4 2.0(JW)
11 PP RECONFIG BITS 59,60 2 2.8(JT)
2 MAC DATA FROM A21 2.4(JQ)
3 MAC LOAD 2.8(JS)

NOTES:

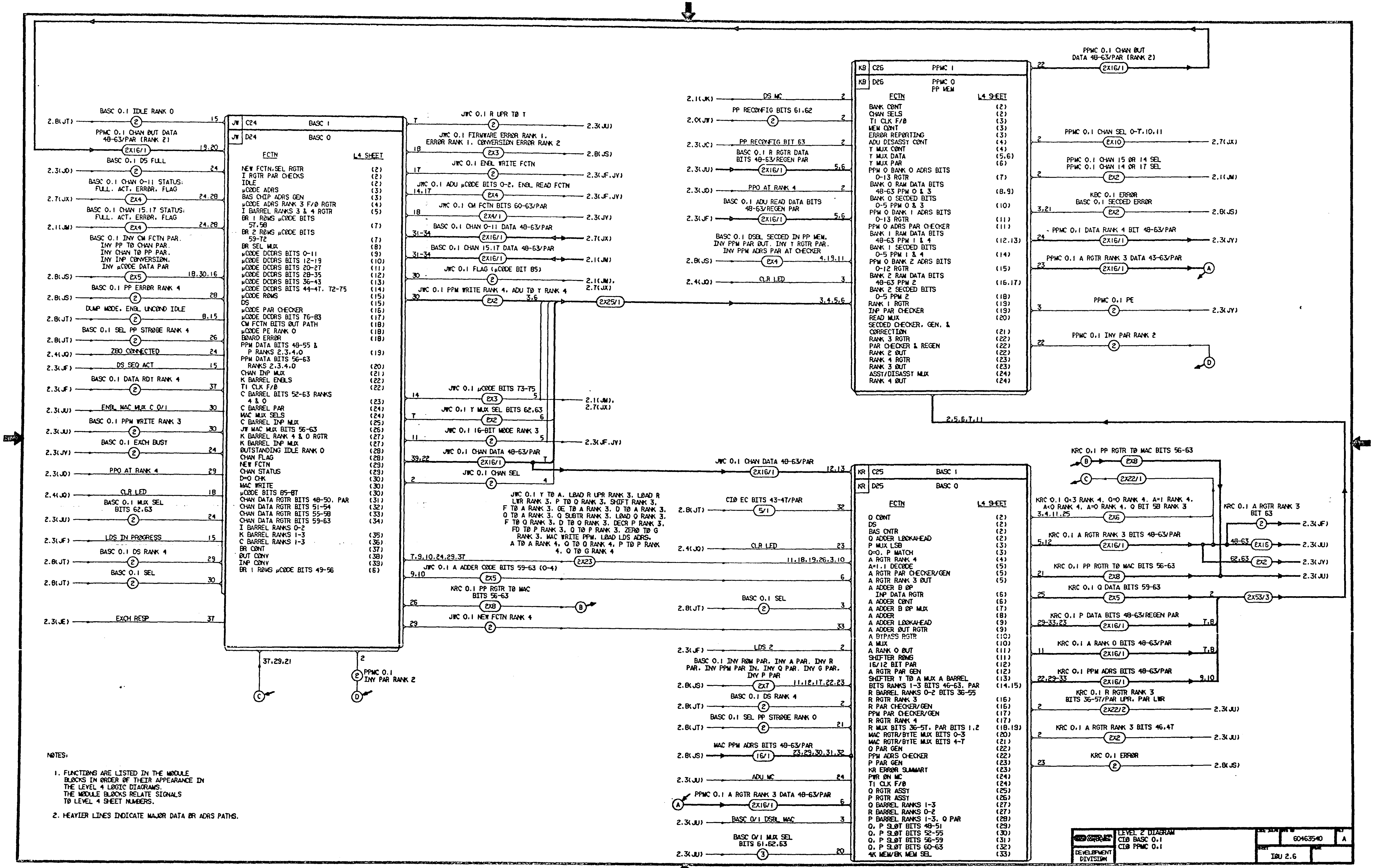
1. SIGNAL NAMES WITH THE PREFIX BAS 0-3, JW 0-3, PPM 0-3, OR KR 0-3 HAVE ORIGINS OR DESTINATIONS IN THE NIO (A AND B PANELS). SIGNAL NAMES WITH THE PREFIX BASC 0,1, JWC 0,1, PPMC 0,1 HAVE ORIGINS OR DESTINATIONS IN THE CIO (C AND D PANELS).

2. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAMS. THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.

3. OF THE THREE GROUPS OF SIGNALS, GROUP 1 WILL BE CABLED TO CPU MAC; GROUP 2 WILL BE CABLED TO A SECOND CPU MAC IF THE SYSTEM HAS TWO CPU'S. THE REMAINING GROUP IS UNUSED.

4. A23 CONTAINS JR IF AT478-A OR AT510-A IS INSTALLED. A23 CONTAINS HR IF AT509-A IS INSTALLED.

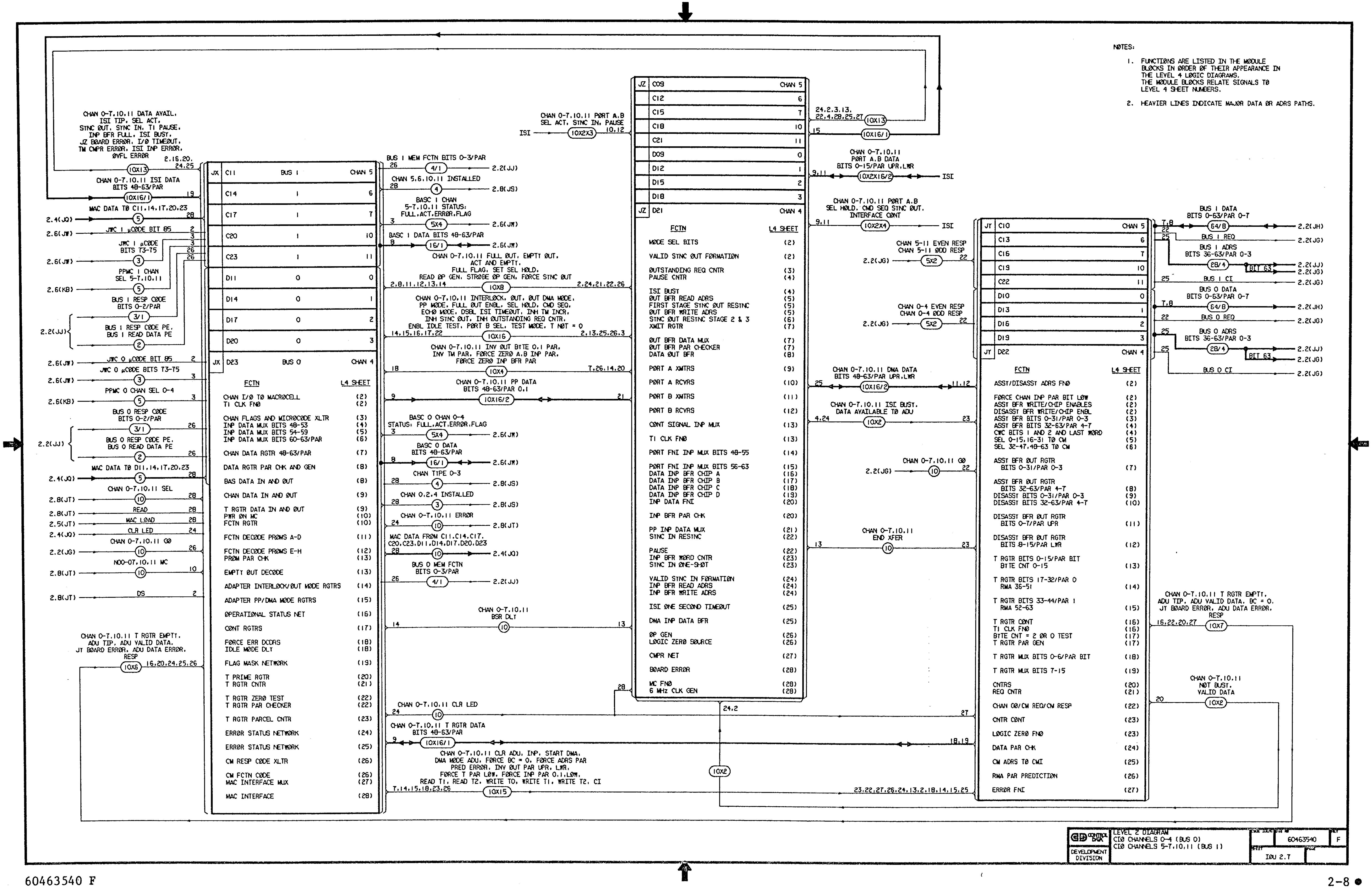
CONTROL DATA DEVELOPMENT DIVISION	LEVEL 2 DIAGRAM MAINTENANCE RGTR B. RADIAL INTERFACE	60463540	G
		IOU 2.5	


BASC 0.1 IDLE RANK 0
PPMC 0.1 CHAN OUT DATA 48-63/PAR (RANK 2)
BASC 0.1 DS FULL
BASC 0.1 CHAN 0-11 STATUS: FULL, ACT, ERROR, FLAG
BASC 0.1 CHAN 15,17 STATUS: FULL, ACT, ERROR, FLAG
BASC 0.1 INV CM FCTN PAR, INV PP TO CHAN PAR, INV CHAN TO PP PAR, INV INP CONVERSION, INV μCODE DATA PAR
BASC 0.1 PP ERROR RANK 4
DUMP MODE, ENBL UNCOND IDLE
BASC 0.1 SEL PP STROBE RANK 4
Z80 CONNECTED
DS SEQ ACT
BASC 0.1 DATA RDY RANK 4
ENBL MAC MUX C 0/1
BASC 0.1 PPM WRITE RANK 3
BASC 0.1 EXCH BUSY
PPO AT RANK 4
CLR LED
BASC 0.1 MUX SEL BITS 62,63
LDS IN PROGRESS
BASC 0.1 DS RANK 4
BASC 0.1 SEL
EXCH RESP
JW C24 BASC 1
JW D24 BASC 0
FCTN
L4 SHEET
NEW FCTN,SEL RGTR (2)
I RGTR PAR CHECKS (2)
IDLE (2)
μCODE ADRS (3)
BAS CHIP ADRS GEN (3)
μCODE ADRS RANK 3 F/O RGTR (4)
I BARREL RANKS 3 & 4 RGTR (5)
BR 1 ROWS μCODE BITS 57,58 (7)
BR 2 ROWS μCODE BITS 59-72 (7)
BR SEL MUX (8)
μCODE DCDRS BITS 0-11 (9)
μCODE DCDRS BITS 12-19 (10)
μCODE DCDRS BITS 20-27 (11)
μCODE DCDRS BITS 28-35 (12)
μCODE DCDRS BITS 36-43 (13)
μCODE DCDRS BITS 44-47, 72-75 (14)
μCODE ROWS (15)
DS (15)
μCODE PAR CHECKER (16)
μCODE DCDRS BITS 76-83 (17)
CM FCTN BITS OUT PATH (18)
μCODE PE RANK 0 (18)
BOARD ERROR (18)
PPM DATA BITS 48-55 & P RANKS 2,3,4,0 (19)
PPM DATA BITS 56-63 RANKS 2,3,4,0 (20)
CHAN INP MUX (21)
K BARREL ENBLS (22)
TI CLK F/0 (22)
C BARREL BITS 52-63 RANKS 4 & 0 (23)
C BARREL PAR (24)
MAC MUX SELS (24)
C BARREL INP MUX (25)
JW MAC MUX BITS 56-63 (26)
K BARREL RANK 4 & 0 RGTR (27)
K BARREL INP MUX (27)
OUTSTANDING IDLE RANK 0 (28)
CHAN FLAG (28)
NEW FCTN (29)
CHAN STATUS (29)
D=0 CHK (30)
MAC WRITE (30)
μCODE BITS 85-87 (30)
CHAN DATA RGTR BITS 48-50, PAR (31)
CHAN DATA RGTR BITS 51-54 (32)
CHAN DATA RGTR BITS 55-58 (33)
CHAN DATA RGTR BITS 59-63 (34)
I BARREL RANKS 0-2
K BARREL RANKS 1-3 (35)
C BARREL RANKS 1-3 (36)
BR CONT (37)
OUT CONV (38)
INP CONV (39)
BR 1 ROWS μCODE BITS 49-56 (6)
JWC 0.1 R UPR TO T
JWC 0.1 FIRMWARE ERROR RANK 1, ERROR RANK 1, CONVERSION ERROR RANK 2
JWC 0.1 ENBL WRITE FCTN
JWC 0.1 ADU μCODE BITS 0-2, ENBL READ FCTN
JWC 0.1 CM FCTN BITS 60-63/PAR
BASC 0.1 CHAN 0-11 DATA 48-63/PAR
BASC 0.1 CHAN 15,17 DATA 48-63/PAR
JWC 0.1 FLAG (μCODE BIT 85)
JWC 0.1 PPM WRITE RANK 4, ADU TO Y RANK 4
JWC 0.1 μCODE BITS 73-75
JWC 0.1 Y MUX SEL BITS 62,63
JWC 0.1 16-BIT MODE RANK 3
JWC 0.1 CHAN DATA 48-63/PAR
JWC 0.1 CHAN SEL
JWC 0.1 Y TO A, LOAD R UPR RANK 3, LOAD R LWR RANK 3, P TO Q RANK 3, SHIFT RANK 3, F TO A RANK 3, GE TO A RANK 3, LOAD R TO A RANK 3, Q TO A RANK 3, Q SUBTR RANK 3, LOAD Q RANK 3, F TO Q RANK 3, D TO Q RANK 3, DECR P RANK 3, FD TO P RANK 3, Q TO P RANK 3, ZERO TO G RANK 3, MAC WRITE PPM, LOAD LDS ADRS, A TO A RANK 4, Q TO P RANK 4, P TO P RANK 4, Q TO G RANK 4
JWC 0.1 A ADDER CODE BITS 59-63 (0-4)
KRC 0.1 PP RGTR TO MAC BITS 56-63
JWC 0.1 NEW FCTN RANK 4
PPMC 0.1 INV PAR RANK 2
DS MC
PP RECONFIG BITS 61,62
PP RECONFIG BIT 63
BASC 0.1 R RGTR DATA BITS 48-63/REGEN PAR
PPO AT RANK 4
BASC 0.1 ADU READ DATA BITS 48-63/REGEN PAR
BASC 0.1 DSBL SECDED IN PP MEM, INV PPM PAR OUT, INV Y RGTR PAR, INV PPM ADRS PAR AT CHECKER
CLR LED
KB C26 PPMC 1
KB D26 PPMC 0 PP MEM
BANK CONT (2)
CHAN SELS (2)
TI CLK F/0 (3)
MEM CONT (3)
ERROR REPORTING (3)
ADU DISASSY CONT (4)
Y MUX CONT (4)
Y MUX DATA (5,6)
Y MUX PAR (6)
PPM 0 BANK 0 ADRS BITS 0-13 RGTR (7)
BANK 0 RAM DATA BITS 48-63 PPM 0 & 3 (8,9)
BANK 0 SECDED BITS 0-5 PPM 0 & 3 (10)
PPM 0 BANK 1 ADRS BITS 0-13 RGTR (11)
PPM 0 ADRS PAR CHECKER (11)
BANK 1 RAM DATA BITS 48-63 PPM 1 & 4 (12,13)
BANK 1 SECDED BITS 0-5 PPM 1 & 4 (14)
PPM 0 BANK 2 ADRS BITS 0-12 RGTR (15)
BANK 2 RAM DATA BITS 48-63 PPM 2 (16,17)
BANK 2 SECDED BITS 0-5 PPM 2 (18)
RANK 1 RGTR (19)
INP PAR CHECKER (19)
READ MUX (20)
SECDED CHECKER, GEN, & CORRECTION (21)
RANK 3 RGTR (22)
PAR CHECKER & REGEN (22)
RANK 2 OUT (22)
RANK 4 RGTR (23)
RANK 3 OUT (23)
ASSY/DISASSY MUX (24)
RANK 4 OUT (24)
PPMC 0.1 CHAN OUT DATA 48-63/PAR (RANK 2)
PPMC 0.1 CHAN SEL 0-7,10,11
PPMC 0.1 CHAN 15 OR 14 SEL
PPMC 0.1 CHAN 14 OR 17 SEL
KBC 0.1 ERROR
BASC 0.1 SECDED ERROR
PPMC 0.1 DATA RANK 4 BIT 48-63/PAR
PPMC 0.1 A RGTR RANK 3 DATA 43-63/PAR
PPMC 0.1 PE
PPMC 0.1 INV PAR RANK 2
JWC 0.1 CHAN DATA 48-63/PAR
CIO EC BITS 43-47/PAR
CLR LED
BASC 0.1 SEL
LDS 2
BASC 0.1 INV ROW PAR, INV A PAR, INV R PAR, INV PPM PAR IN, INV Q PAR, INV G PAR, INV P PAR
BASC 0.1 DS RANK 4
BASC 0.1 SEL PP STROBE RANK 0
MAC PPM ADRS BITS 48-63/PAR
ADU MC
PPMC 0.1 A RGTR RANK 3 DATA 48-63/PAR
BASC 0/1 DSBL MAC
BASC 0/1 MUX SEL BITS 61,62,63
KR C25 BASC 1
KR D25 BASC 0
Q CONT (2)
DS (2)
BAS CNTR (2)
Q ADDER LOOKAHEAD (2)
P MUX LSB (3)
Q=0, P MATCH (3)
A RGTR RANK 4 (4)
A=1,1 DECODE (5)
A RGTR PAR CHECKER/GEN (5)
A RGTR RANK 3 OUT (5)
A ADDER B OP INP DATA RGTR (6)
A ADDER CONT (6)
A ADDER B OP MUX (7)
A ADDER (8)
A ADDER LOOKAHEAD (9)
A ADDER OUT RGTR (9)
A BYPASS RGTR (10)
A MUX (10)
A RANK 0 OUT (11)
SHIFTER ROWS (11)
16/12 BIT PAR (12)
A RGTR PAR GEN (12)
SHIFTER Y TO A MUX A BARREL BITS RANKS 1-3 BITS 46-63, PAR (13) (14,15)
R BARREL RANKS 0-2 BITS 36-55
R RGTR RANK 3 (16)
R PAR CHECKER/GEN (16)
PPM PAR CHECKER/GEN (17)
R RGTR RANK 4 (17)
R MUX BITS 36-57, PAR BITS 1,2 (18,19)
MAC RGTR/BYTE MUX BITS 0-3 (20)
MAC RGTR/BYTE MUX BITS 4-7 (21)
Q PAR GEN (22)
PPM ADRS CHECKER (22)
P PAR GEN (23)
KR ERROR SUMMARY (23)
PWR ON MC (24)
TI CLK F/0 (24)
Q RGTR ASSY (25)
P RGTR ASSY (26)
Q BARREL RANKS 1-3 (27)
R BARREL RANKS 0-2 (27)
P BARREL RANKS 1-3, Q PAR (28)
Q, P SLOT BITS 48-51 (29)
Q, P SLOT BITS 52-55 (30)
Q, P SLOT BITS 56-59 (31)
Q, P SLOT BITS 60-63 (32)
4K MEM/BK MEM SEL (33)
KRC 0.1 PP RGTR TO MAC BITS 56-63
KRC 0.1 Q<3 RANK 4, Q=0 RANK 4, A=1 RANK 4, A<0 RANK 4, A=0 RANK 4, Q BIT 58 RANK 3
KRC 0.1 A RGTR RANK 3 BITS 48-63/PAR
KRC 0.1 PP RGTR TO MAC BITS 56-63
KRC 0.1 Q DATA BITS 59-63
KRC 0.1 P DATA BITS 48-63/REGEN PAR
KRC 0.1 A RANK 0 BITS 48-63/PAR
KRC 0.1 PPM ADRS BITS 48-63/PAR
KRC 0.1 R RGTR RANK 3 BITS 36-57/PAR UPR, PAR LWR
KRC 0.1 A RGTR RANK 3 BITS 46,47
KRC 0.1 ERROR
KRC 0.1 A RGTR RANK 3 BIT 63
2.8(JT)
2.3(JD)
2.7(JX)
2.1(JM)
2.8(JS)
2.4(JQ)
2.3(JF)
2.3(JU)
2.3(JY)
2.4(JQ)
2.3(JE)
2.3(JF,JY)
2.1(JK)
2.0(JM)
2.3(JC)
2.1(JM), 2.7(JX)
2.3(JX)
2.3(JY)
2.2(JU)

NOTES:

1. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAMS. THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.
2. HEAVIER LINES INDICATE MAJOR DATA OR ADRS PATHS.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
CIO BASC 0.1
CIO PPMC 0.1
60463540 A
IOU 2.6



CHAN 0-7,10,11 DATA AVAIL, ISI TIP, SEL ACT, SYNC OUT, SYNC IN, TI PAUSE, INP BFR FULL, ISI BUSY, JZ BOARD ERROR, I/O TIMEOUT, TM CMPR ERROR, ISI INP ERROR, OVFL ERROR
10X13
2.16.20. 24.25
CHAN 0-7,10,11 ISI DATA BITS 48-63/PAR
10X16/1
MAC DATA TO C11,14,17,20,23
2.4(JQ)
2.6(JM)
JMC 1 µCODE BIT 85
JMC 1 µCODE BITS T3-T5
PPMC 1 CHAN SEL 5-7,10,11
2.6(KB)
BUS 1 RESP CODE BITS 0-2/PAR
2.2(JJ)
BUS 1 RESP CODE PE, BUS 1 READ DATA PE
JMC 0 µCODE BIT 85
JMC 0 µCODE BITS T3-T5
PPMC 0 CHAN SEL 0-4
BUS 0 RESP CODE BITS 0-2/PAR
BUS 0 RESP CODE PE, BUS 0 READ DATA PE
MAC DATA TO D11,14,17,20,23
CHAN 0-7,10,11 SEL
2.8(JT)
READ
2.5(JT)
MAC LOAD
CLR LED
CHAN 0-7,10,11 GO
NOO-07,10,11 MC
DS
CHAN 0-7,10,11 T RGTR EMPTY, ADU TIP, ADU VALID DATA, JT BOARD ERROR, ADU DATA ERROR, RESP
10X5
16,20,24,25,26
JX C11 BUS 1 CHAN 5
C14 1 6
C17 1 7
C20 1 10
C23 1 11
D11 0 0
D14 0 1
D17 0 2
D20 0 3
JX D23 BUS 0 CHAN 4
FCTN L4 SHEET
CHAN I/O TO MACROCELL (2)
TI CLK FNO (2)
CHAN FLAGS AND MICROCODE XLTR (3)
INP DATA MUX BITS 48-53 (4)
INP DATA MUX BITS 54-59 (5)
INP DATA MUX BITS 60-63/PAR (6)
CHAN DATA RGTR 48-63/PAR (7)
DATA RGTR PAR CHK AND GEN (8)
BAS DATA IN AND OUT (8)
CHAN DATA IN AND OUT (9)
T RGTR DATA IN AND OUT (9)
PWR ON MC (10)
FCTN RGTR (10)
FCTN DECODE PROMS A-D (11)
FCTN DECODE PROMS E-H (12)
PROM PAR CHK (13)
EMPTY OUT DECODE (13)
ADAPTER INTERLOCK/OUT MODE RGTRS (14)
ADAPTER PP/DMA MODE RGTRS (15)
OPERATIONAL STATUS NET (16)
CONT RGTRS (17)
FORCE ERR DCDRS (18)
IDLE MODE DLY (18)
FLAG MASK NETWORK (19)
T PRIME RGTR (20)
T RGTR CNTR (21)
T RGTR ZERO TEST (22)
T RGTR PAR CHECKER (22)
T RGTR PARCEL CNTR (23)
ERROR STATUS NETWORK (24)
ERROR STATUS NETWORK (25)
CM RESP CODE XLTR (26)
CM FCTN CODE (26)
MAC INTERFACE MUX (27)
MAC INTERFACE (28)
BUS 1 MEM FCTN BITS 0-3/PAR
4/1
2.2(JJ)
CHAN 5,6,10,11 INSTALLED
2.8(JS)
BASC 1 CHAN 5-7,10,11 STATUS: FULL,ACT,ERROR,FLAG
5X4
2.6(JM)
BASC 1 DATA BITS 48-63/PAR
16/1
CHAN 0-7,10,11 FULL OUT, EMPTY OUT, ACT AND EMPTY, FULL FLAG, SET SEL HOLD, READ OP GEN, STROBE OP GEN, FORCE SYNC OUT
2,8,11,12,13,14
10X8
2,24,21,22,26
CHAN 0-7,10,11 INTERLOCK, OUT, OUT DMA MODE, PP MODE, FULL OUT ENBL, SEL HOLD, CMD SEQ, ECHO MODE, DSBL ISI TIMEOUT, INH TM INCR, INH SYNC OUT, INH OUTSTANDING REQ CNTR, ENBL IDLE TEST, PORT B SEL, TEST MODE, T NOT = 0
14,15,16,17,22
10X16
2,13,25,26,3
CHAN 0-7,10,11 INV OUT BYTE 0,1 PAR, INV TM PAR, FORCE ZERO A,B INP PAR, FORCE ZERO INP BFR PAR
10X4
7,26,14,20
CHAN 0-7,10,11 PP DATA BITS 48-63/PAR 0,1
10X16/2
BASC 0 CHAN 0-4 STATUS: FULL,ACT,ERROR,FLAG
BASC 0 DATA BITS 48-63/PAR
CHAN TYPE 0-3
CHAN 0,2,4 INSTALLED
CHAN 0-7,10,11 ERROR
MAC DATA FROM C11,C14,C17,C20,C23,D11,D14,D17,D20,D23
2.4(JQ)
BUS 0 MEM FCTN BITS 0-3/PAR
CHAN 0-7,10,11 BSR DLT
CHAN 0-7,10,11 CLR LED
CHAN 0-7,10,11 T RGTR DATA BITS 48-63/PAR
10X16/1
CHAN 0-7,10,11 CLR ADU, INP, START DMA, DMA MODE ADU, FORCE BC = 0, FORCE ADRS PAR PRED ERROR, INV OUT PAR UPR, LWR, FORCE T PAR LOW, FORCE INP PAR 0,1,LOW, READ T1, READ T2, WRITE T0, WRITE T1, WRITE T2, CI
7,14,15,18,23,26
10X15
23,22,27,26,24,13,2,18,14,15,25
10X2
24,2
CHAN 0-7,10,11 PORT A,B SEL ACT, SYNC IN, PAUSE
ISI
10X2X3
10,12
JZ C09 CHAN 5
C12 6
C15 7
C18 10
C21 11
D09 0
D12 1
D15 2
D18 3
JZ D21 CHAN 4
FCTN L4 SHEET
MODE SEL BITS (2)
VALID SYNC OUT FORMATION (2)
OUTSTANDING REQ CNTR (3)
PAUSE CNTR (4)
ISI BUSY (4)
OUT BFR READ ADRS (5)
FIRST STAGE SYNC OUT RESYNC (5)
OUT BFR WRITE ADRS (5)
SYNC OUT RESYNC STAGE 2 & 3 (6)
XMIT RGTR (7)
OUT BFR DATA MUX (7)
OUT BFR PAR CHECKER (7)
DATA OUT BFR (8)
PORT A XMTRS (9)
PORT A RCVRS (10)
PORT B XMTRS (11)
PORT B RCVRS (12)
CONT SIGNAL INP MUX (13)
TI CLK FNO (13)
PORT FNI INP MUX BITS 48-55 (14)
PORT FNI INP MUX BITS 56-63 (15)
DATA INP BFR CHIP A (16)
DATA INP BFR CHIP B (17)
DATA INP BFR CHIP C (18)
DATA INP BFR CHIP D (19)
INP DATA FNI (20)
INP BFR PAR CHK (20)
PP INP DATA MUX (21)
SYNC IN RESYNC (22)
PAUSE (22)
INP BFR WORD CNTR (23)
SYNC IN ONE-SHOT (23)
VALID SYNC IN FORMATION (24)
INP BFR READ ADRS (24)
INP BFR WRITE ADRS (24)
ISI ONE SECOND TIMEOUT (25)
DMA INP DATA BFR (25)
OP GEN (26)
LOGIC ZERO SOURCE (26)
CMPR NET (27)
BOARD ERROR (28)
MC FNO (28)
6 MHz CLK GEN (28)
24,2,3,13, 22,4,28,25,27
10X13
10X16/1
CHAN 0-7,10,11 PORT A,B DATA BITS 0-15/PAR UPR,LWR
10X2X16/2
CHAN 0-7,10,11 PORT A,B SEL HOLD, CMD SEQ SYNC OUT, INTERFACE CONT
10X2X4
CHAN 5-11 EVEN RESP CHAN 5-11 ODD RESP
2.2(JG)
5X2
CHAN 0-4 EVEN RESP CHAN 0-4 ODD RESP
CHAN 0-7,10,11 DMA DATA BITS 48-63/PAR UPR,LWR
10X16/2
CHAN 0-7,10,11 ISI BUSY, DATA AVAILABLE TO ADU
CHAN 0-7,10,11 GO
CHAN 0-7,10,11 END XFER
JT C10 CHAN 5
C13 6
C16 7
C19 10
C22 11
D10 0
D13 1
D16 2
D19 3
JT D22 CHAN 4
FCTN L4 SHEET
ASST/DISASST ADRS FNO (2)
FORCE CHAN INP PAR BIT LOW (2)
ASST BFR WRITE/CHIP ENABLES (2)
DISASST BFR WRITE/CHIP ENBL (2)
ASST BFR BITS 0-31/PAR 0-3 (3)
ASST BFR BITS 32-63/PAR 4-7 (4)
CWC BITS 1 AND 2 AND LAST WORD (4)
SEL 0-15,16-31 TO CM (5)
SEL 32-47,48-63 TO CM (6)
ASST BFR OUT RGTR BITS 0-31/PAR 0-3 (7)
ASST BFR OUT RGTR BITS 32-63/PAR 4-7 (8)
DISASST BITS 0-31/PAR 0-3 (9)
DISASST BITS 32-63/PAR 4-7 (10)
DISASST BFR OUT RGTR BITS 0-7/PAR UPR (11)
DISASST BFR OUT RGTR BITS 8-15/PAR LWR (12)
T RGTR BITS 0-15/PAR BIT BYTE CNT 0-15 (13)
T RGTR BITS 17-32/PAR 0 RMA 36-51 (14)
T RGTR BITS 33-44/PAR 1 RMA 52-63 (15)
T RGTR CONT (16)
TI CLK FNO (16)
BYTE CNT = 2 OR 0 TEST (17)
T RGTR PAR GEN (17)
T RGTR MUX BITS 0-6/PAR BIT (18)
T RGTR MUX BITS 7-15 (19)
CNTRS (20)
REQ CNTR (21)
CHAN GO/CM REQ/CM RESP (22)
CNTR CONT (23)
LOGIC ZERO FNO (23)
DATA PAR CHK (24)
CM ADRS TO CMI (25)
RMA PAR PREDICTION (26)
ERROR FNI (27)
BUS 1 DATA BITS 0-63/PAR 0-7
64/8
2.2(JH)
BUS 1 REQ
2.2(JG)
BUS 1 ADRS BITS 36-63/PAR 0-3
28/4
BIT 63
2.2(JJ)
BUS 1 CI
BUS 0 DATA BITS 0-63/PAR 0-7
BUS 0 REQ
BUS 0 ADRS BITS 36-63/PAR 0-3
BUS 0 CI
CHAN 0-7,10,11 T RGTR EMPTY, ADU TIP, ADU VALID DATA, BC = 0, JT BOARD ERROR, ADU DATA ERROR, RESP
16,22,20,27
10X7
CHAN 0-7,10,11 NOT BUSY, VALID DATA
10X2

NOTES:

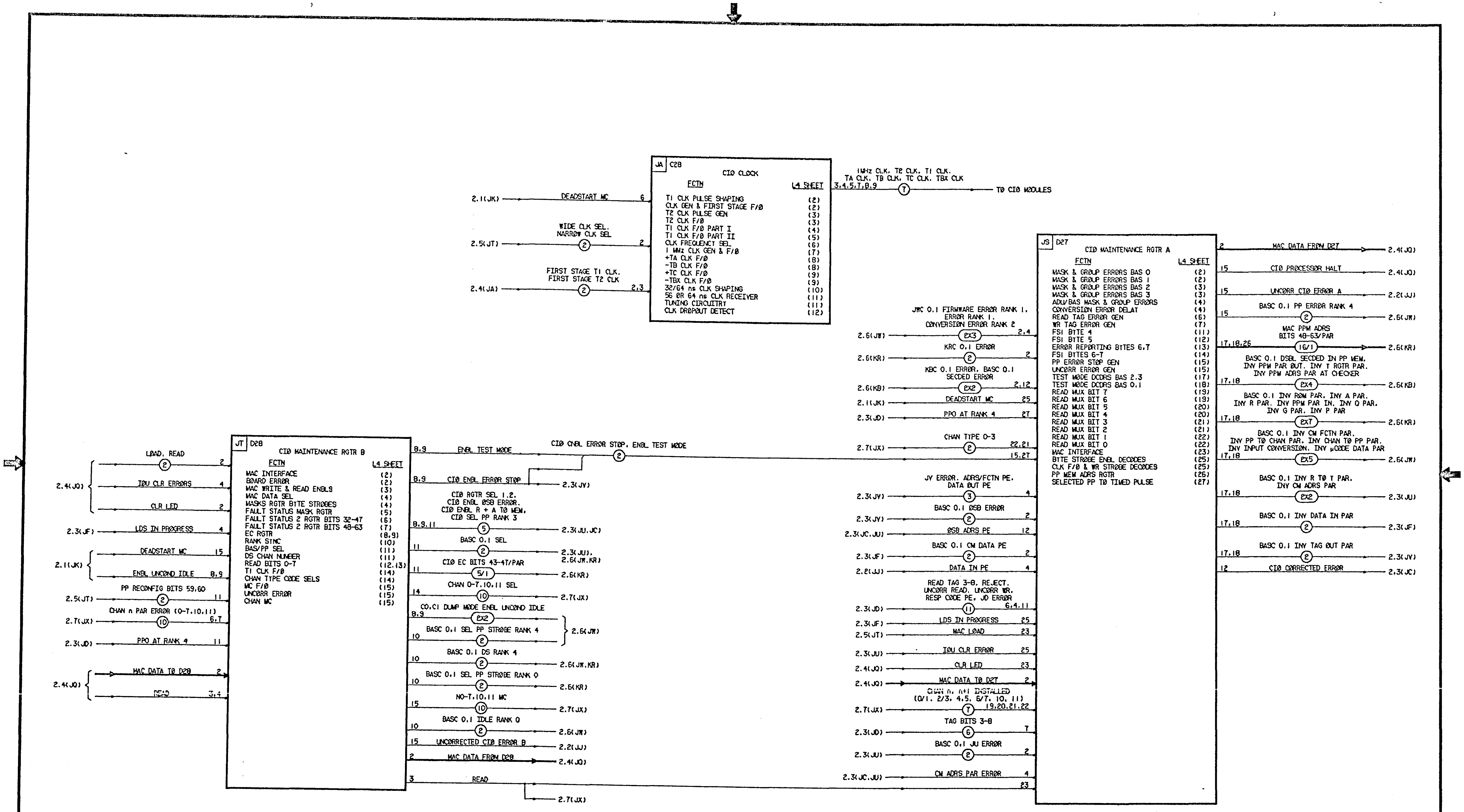
1. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAMS. THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.
2. HEAVIER LINES INDICATE MAJOR DATA OR ADRS PATHS.

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 2 DIAGRAM
CIO CHANNELS 0-4 (BUS 0)
CIO CHANNELS 5-7,10,11 (BUS 1)

60463540 F

IOU 2.7


JA C28
CIO CLOCK
FCTN
L4 SHEET
T1 CLK PULSE SHAPING (2)
CLK GEN & FIRST STAGE F/O (2)
T2 CLK PULSE GEN (3)
T2 CLK F/O (3)
T1 CLK F/O PART I (4)
T1 CLK F/O PART II (5)
CLK FREQUENCY SEL (6)
1 MHz CLK GEN & F/O (7)
+TA CLK F/O (8)
-TB CLK F/O (8)
+TC CLK F/O (9)
-TBX CLK F/O (9)
32/64 ns CLK SHAPING (10)
56 OR 64 ns CLK RECEIVER (11)
TUNING CIRCUITRY (11)
CLK DROPOUT DETECT (12)
2.1(JK) DEADSTART MC 6
2.5(JT) WIDE CLK SEL. NARROW CLK SEL 2 2
2.4(JA) FIRST STAGE T1 CLK. FIRST STAGE T2 CLK 2 2,3
1MHz CLK. T2 CLK. T1 CLK. TA CLK. TB CLK. TC CLK. TBX CLK
3,4,5,7,8,9 7 TO CIO MODULES
JT D28
CIO MAINTENANCE RGTR B
FCTN
L4 SHEET
MAC INTERFACE (2)
BOARD ERROR (2)
MAC WRITE & READ ENBLS (3)
MAC DATA SEL (4)
MASKS RGTR BYTE STROBES (4)
FAULT STATUS MASK RGTR (5)
FAULT STATUS 2 RGTR BITS 32-47 (6)
FAULT STATUS 2 RGTR BITS 48-63 (7)
EC RGTR (8,9)
RANK SYNC (10)
BAS/PP SEL (11)
DS CHAN NUMBER (11)
READ BITS 0-7 (12,13)
T1 CLK F/O (14)
CHAN TYPE CODE SELS (14)
MC F/O (15)
UNCORR ERROR (15)
CHAN MC (15)
2.4(JQ) LOAD, READ 2 2
IOU CLR ERRORS 4
CLR LED 2
2.3(JF) LDS IN PROGRESS 4
2.1(JK) DEADSTART MC 15
ENBL UNCOND IDLE 8,9
2.5(JT) PP RECONFIG BITS 59,60 2 11
2.7(JX) CHAN n PAR ERROR (0-7,10,11) 10 6,7
2.3(JD) PPO AT RANK 4 11
2.4(JQ) MAC DATA TO D28 2
READ 3,4
8,9 ENBL TEST MODE
CIO CNBL ERROR STOP, ENBL TEST MODE 2
8,9 CIO ENBL ERROR STOP 2.3(JV)
CIO RGTR SEL 1,2. CIO ENBL OSB ERROR. CIO ENBL R + A TO MEM. CIO SEL PP RANK 3
8,9,11 5 2.3(JU,JC)
BASC 0.1 SEL 11 2 2.3(JU). 2.6(JW,KR)
CIO EC BITS 43-47/PAR 11 5/1 2.6(KR)
CHAN 0-7,10,11 SEL 14 10 2.7(JX)
CO,CI DUMP MODE ENBL UNCOND IDLE 8,9 2X2
BASC 0.1 SEL PP STROBE RANK 4 10 2 2.6(JW)
BASC 0.1 DS RANK 4 10 2 2.6(JW,KR)
BASC 0.1 SEL PP STROBE RANK 0 10 2 2.6(KR)
NO-7,10,11 MC 15 10 2.7(JX)
BASC 0.1 IDLE RANK 0 10 2 2.6(JW)
15 UNCORRECTED CIO ERROR B 2.2(JJ)
2 MAC DATA FROM D28 2.4(JQ)
3 READ 2.7(JX)
JS D27
CIO MAINTENANCE RGTR A
FCTN
L4 SHEET
MASK & GROUP ERRORS BAS 0 (2)
MASK & GROUP ERRORS BAS 1 (2)
MASK & GROUP ERRORS BAS 2 (3)
MASK & GROUP ERRORS BAS 3 (3)
ADU/BAS MASK & GROUP ERRORS (4)
CONVERSION ERROR DELAY (4)
READ TAG ERROR GEN (6)
WR TAG ERROR GEN (7)
FSI BYTE 4 (11)
FSI BYTE 5 (12)
ERROR REPORTING BYTES 6,7 (13)
FSI BYTES 6-7 (14)
PP ERROR STOP GEN (15)
UNCORR ERROR GEN (15)
TEST MODE DCDRS BAS 2,3 (17)
TEST MODE DCDRS BAS 0,1 (18)
READ MUX BIT 7 (19)
READ MUX BIT 6 (19)
READ MUX BIT 5 (20)
READ MUX BIT 4 (20)
READ MUX BIT 3 (21)
READ MUX BIT 2 (21)
READ MUX BIT 1 (22)
READ MUX BIT 0 (22)
MAC INTERFACE (23)
BYTE STROBE ENBL DECODES (25)
CLK F/O & WR STROBE DECODES (25)
PP MEM ADRS RGTR (26)
SELECTED PP TO TIMED PULSE (27)
JWC 0.1 FIRMWARE ERROR RANK 1. ERROR RANK 1. CONVERSION ERROR RANK 2
2.6(JW) 2X3 2,4
KRC 0.1 ERROR 2.6(KR) 2 2
KBC 0.1 ERROR. BASC 0.1 SECDED ERROR 2.6(KB) 2X2 2,12
2.1(JK) DEADSTART MC 25
2.3(JD) PPO AT RANK 4 27
CHAN TYPE 0-3 2.7(JX) 2 22,21
15,27
JY ERROR. ADRS/FCTN PE. DATA OUT PE 2.3(JY) 3 4
BASC 0.1 OSB ERROR 2.3(JY) 2 2
2.3(JC,JU) OSB ADRS PE 12
BASC 0.1 CM DATA PE 2.3(JF) 2 2
2.2(JJ) DATA IN PE 4
READ TAG 3-8. REJECT. UNCORR READ. UNCORR WR. RESP CODE PE. JD ERROR 2.3(JD) 11 6,4,11
2.3(JF) LDS IN PROGRESS 25
2.5(JT) MAC LOAD 23
2.3(JU) IOU CLR ERROR 25
2.4(JQ) CLR LED 23
2.4(JQ) MAC DATA TO D27 2
CHAN n, n+1 INSTALLED (0/1, 2/3, 4,5, 6/7, 10, 11) 2.7(JX) 7 19,20,21,22
TAG BITS 3-8 2.3(JD) 6 7
BASC 0.1 JU ERROR 2.3(JU) 2 2
2.3(JC,JU) CM ADRS PAR ERROR 4
23
2 MAC DATA FROM D27 2.4(JQ)
15 CIO PROCESSOR HALT 2.4(JQ)
15 UNCORR CIO ERROR A 2.2(JJ)
BASC 0.1 PP ERROR RANK 4 15 2 2.6(JW)
MAC PPM ADRS BITS 48-63/PAR 17,18,26 16/1 2.6(KR)
BASC 0.1 DSBL SECDED IN PP MEM. INV PPM PAR OUT. INV Y RGTR PAR. INV PPM ADRS PAR AT CHECKER 17,18 2X4 2.6(KB)
BASC 0.1 INV ROM PAR. INV A PAR. INV R PAR. INV PPM PAR IN. INV Q PAR. INV G PAR. INV P PAR 17,18 2X7 2.6(KR)
BASC 0.1 INV CM FCTN PAR. INV PP TO CHAN PAR. INV CHAN TO PP PAR. INV INPUT CONVERSION. INV µCODE DATA PAR 17,18 2X5 2.6(JW)
BASC 0.1 INV R TO Y PAR. INV CM ADRS PAR 17,18 2X2 2.3(JU)
BASC 0.1 INV DATA IN PAR 17,18 2 2.3(JF)
BASC 0.1 INV TAG OUT PAR 17,18 2 2.3(JV)
12 CIO CORRECTED ERROR 2.3(JC)

NOTES:

1. FUNCTIONS ARE LISTED IN THE MODULE BLOCKS IN ORDER OF THEIR APPEARANCE IN THE LEVEL 4 LOGIC DIAGRAMS. THE MODULE BLOCKS RELATE SIGNALS TO LEVEL 4 SHEET NUMBERS.
2. HEAVIER LINES INDICATE MAJOR DATA OR ADRS PATHS.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 2 DIAGRAM
CIO MAINTENANCE RGTRS
CIO CLOCK

60463540 A
IOU 2.8

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Z80 CPU AND BUS DRIVERS

The Z80 CPU controls all the data flow from a CC634 Display Terminal or CC598 System Console to channel 15, and from the MAC to channel 10, to a CC634 terminal, or to a CC598 console. The Z80 also controls the PP reconfiguration bits (TPM 3.5B), which gate the proper outputs of the PP and Deadstart Number Counters (TPM 3.7A) to the Q Register of the PPs. The Z80 is controlled by microcode that is stored in the EPROMs.

The Diagnostic Interrupt going to the Z80 is a troubleshooting input signal that tests the data paths between the Z80 and the CC634 terminals, CC598 consoles, or display controller. When the Enable Diagnostic switch is set to enable the Diagnostic Interrupt, an interrupt occurs every 4096 microseconds that causes the Z80 to start executing diagnostic code at a particular EPROM address. This code causes characters received from the display controller, one of the terminals, or one of the consoles, to be echoed back. This allows a check that all data bits are being gated through properly. If the port option switches are set so neither port 0 nor port 1 is selected, the echoed data goes to the display controller.

The Interrupt input signal interrupts the Z80 for port 0 or port 1 communications. Conditions that cause this interrupt are: Data ready in the UART, a ring from a modem, or a change in the carrier (either a drop or rise). A data-ready condition in deadstart mode causes the Z80 to read the byte stored in the UART and assemble it into a character string. A data-ready condition in TPM mode causes the Z80 to read the byte and place it in the soft FIFO buffer in RAM for subsequent transfer to channel 15.

RESET CONTROL

The Deadstart switch on the display controller or a power-up starts the Z80 executing from address 0. This initializes the TPM.

POWER STATUS SIGNALS

There are two power status signals. One is the +5 Volt Power Good signal and the other is the System Power Good signal (TPM 3.1D). In order for the Z80 to process data transfers, both of these signals have to be present.

The +5 Volt Power Good signal guards against a case where erroneous data may be transferred because of unstable +5-volt power. If the +5-volt power starts to vary, the +5 Volt Power Good signal drops, causing Bus Request to go to the Z80. With Bus Request present, the Z80 outputs Bus Acknowledge after it finishes executing the current instruction. This resets a flip-flop that provides the Address Decoder with the RAM/Calendar Clock Enable. Without this enable, the Calendar Clock and RAM go into standby mode (Calendar Clock keeps incrementing as long as battery power is present) and the Switch Drivers are disabled.

If +5-volt power becomes stable again, the +5 Volt Power Good signal causes operations to return to normal.

MEMORY REQUEST AND I/O REQUEST SIGNALS

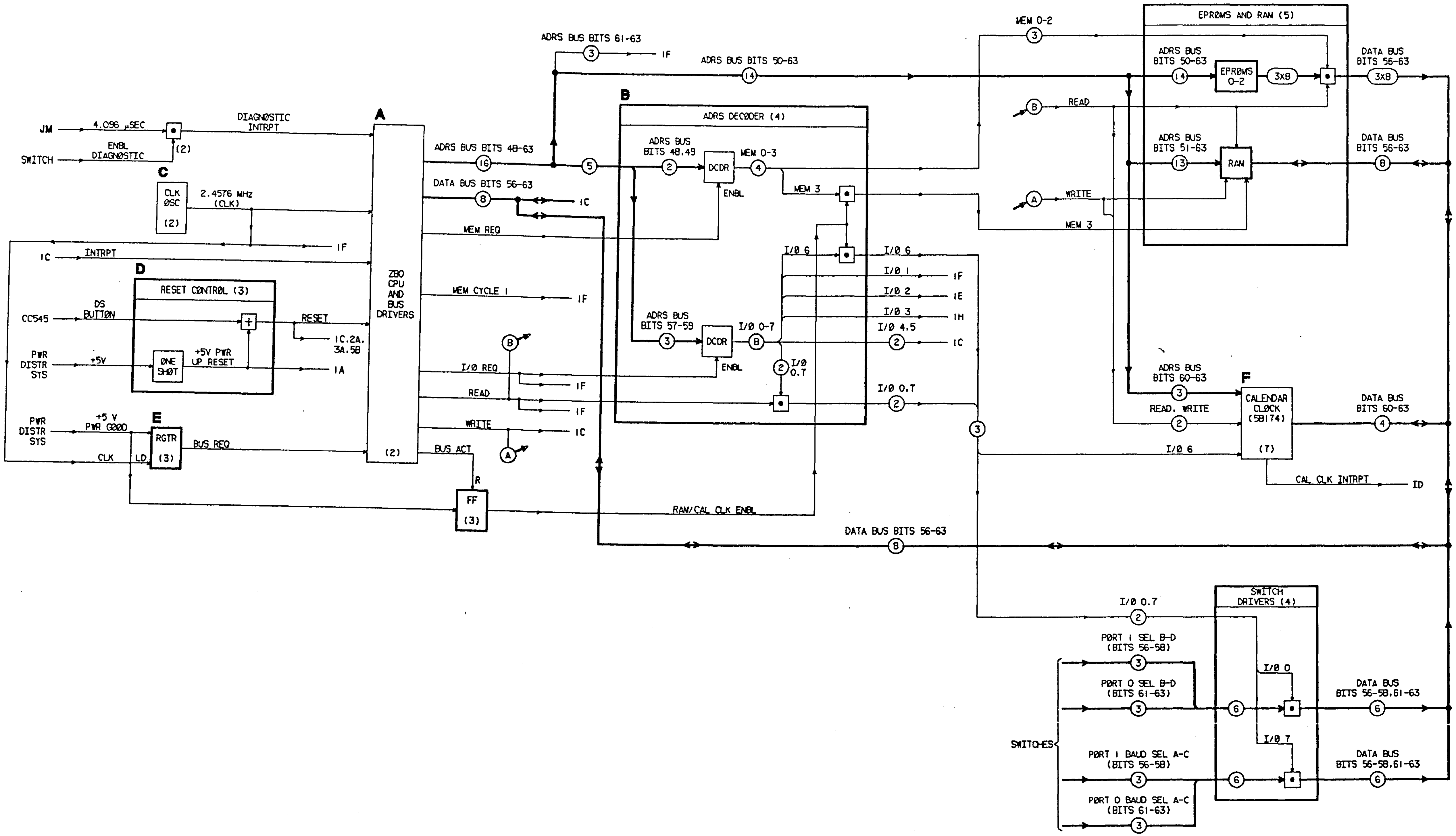
The Memory Request output signal from the Z80 is always present when the Z80 is accessing EPROMs or RAM. I/O Request is always present when the Z80 is accessing one of the ports, one of the UARTs, the Switch Drivers, or the Calendar Clock.

ADDRESS DECODER

The Address Decoder generates the chip selects for the EPROMs, RAM, Calendar Clock, Switch Drivers, and UARTs.

EPROMS AND RAM

The EPROMs contain the display driver code and deadstart programs. The RAM contains the soft FIFO buffers. The RAM also contains various flags that carry information such as which terminals are active, whether a password is required, and which display happens to be on the system console at that particular time. The RAM also contains deadstart user programs 0 through 3 and the screen deadstart program.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JK)
Z80 CPU. ADRS DECODER.
EPROMS. RAM. CALENDAR CLOCK

CODE IDENT	DWG NO	REV
	60463540	H

SHEET	PAGE
TPM 3.0	

BATTERY CIRCUIT

The Battery Circuit monitors the voltage level of the lithium battery that is mounted on the Z80 card. If the battery voltage drops below +2.5 volts, the Battery Failed Flip-Flop sets. The Z80 (TPM 3.0A) then outputs a message to the display controller, CC634 terminal, or CC598 console indicating that the battery has started to fail. At this point, no damage has occurred to data in the Calendar Clock or RAM (TPM 3.0) because +2.2 volts will suffice. However, once the battery begins failing, it fails very rapidly.

DATA INPUT PORT

All incoming data to the Z80 comes through the Data Input Port. The Port 0 and Port 1 FIFO data inputs are from the least significant half of channel 15 via the Channel 15 Input Port FIFO Buffers (TPM 3.2C). Muxed Data Bits 56 through 63 contain display controller data, MAC data, or channel 15 function codes.

The Input Port Empty signal from the Data Input Port is always active except after the Z80 has read a byte. Immediately after Z80 reads a byte, Input Port Empty goes inactive for a pulse and then goes active again.

STATUS INPUT PORT

The Z80 reads this port to obtain status information during data transfers with channel 15, during deadstarts, and during slow functions (channel 15 functions translated by the Z80 microcode). The major inputs to this port are described in the following paragraphs.

The Ports 0 and 1 FIFO Data Ready signals indicate whether a data byte from channel 15 has advanced to the top of the Channel 15 Input Port FIFO Buffers (TPM 3.2C). If so, the Z80 reads the data byte and sends it out the selected port.

Ports 0 and 1 Holding Register Full signals indicate whether channel 15 has taken the previous byte that the Z80 stored in the Holding Register (TPM 3.3C). If not, the Z80 leaves this byte in the Holding Register and starts storing subsequent bytes from the connected terminal into the RAM soft buffer FIFO (TPM 3.0). Five bytes may come in, one in the Holding Register and four in the soft FIFO buffer before the bytes start to be overwritten and an overrun status bit is set.

Select Port 1 informs the Z80 whether the 7000_8 or 7001_8 function was issued from channel 15. The Z80 uses this to determine which port is affected by subsequent functions, such as setting two-port mux mode or clearing output and input buffers.

The Long Deadstart Branch Test Failed bit indicates whether the first part of the long deadstart code (test of the 300 instruction) has executed properly. In the case of a long deadstart branch test failure, the Z80 outputs a message for the screen and does not execute a short deadstart.

Long Deadstart End informs the Z80 that the branch test part of the long deadstart code is complete and other conditions can be checked to determine if the Z80 should start executing a short deadstart.

Ready Response and Inactive Response are not currently used.

Function Code Bits 56 through 58 and 63 are channel 15 control signals that are used when the Z80 is processing a slow function or sending or receiving words from channel 15. Function Code Bit 56 (Mux Condition Busy) sets whenever the Z80 is processing a slow function. It remains set during the data transfer. If a data transfer is not involved, Mux Condition Busy remains set while the slow function is being decoded and executed by the Z80.

PORTS 0,1 UARTS

The functions of the UARTs are to assemble the serial asynchronous bit stream into a parallel data byte that can be gated onto the data bus and read by the Z80, and to disassemble the data byte from the data bus into serial asynchronous bits and send them to a CC634 terminal or CC598 console.

The UARTs use standard RS-232-C control signals. The Data Terminal Ready, Request To Send, Carrier On†, and Clear To Send signals are always on when a terminal or console is directly connected to a port; the Ring Indicator signal is not on. However, if port communications for a CC634 terminal are through a modem, the RS232 signals are only on when applicable. In this case, when a port is called, the Z80 detects a ring via the Ring Indicator signal. If a PP does not answer by setting the Data Terminal Ready signal, the Z80 sets the Data Terminal Ready and Request To Send signals.

After the call has been answered, the modem sets Clear To Send, Carrier On, and Data Set Ready. Carrier On indicates that the modem on the other end is connected and transmitting a carrier frequency, thus establishing a good connection. The Z80 waits up to 21 seconds for all three of these signals to be present. If all are not present, the Z80 clears Data Terminal Ready and Request To Send.

FUNCTION AND DATA OUTPUT PORTS

The Function Port gates the function codes that control the TPM and allows the Z80 to send inactive responses (empties and fulls) to channel 15 on slow functions and data transfers. The Data Output Port sends data to the display controller, the MAC, or to channel 15 through one of the Holding Registers (TPM 3.3C).

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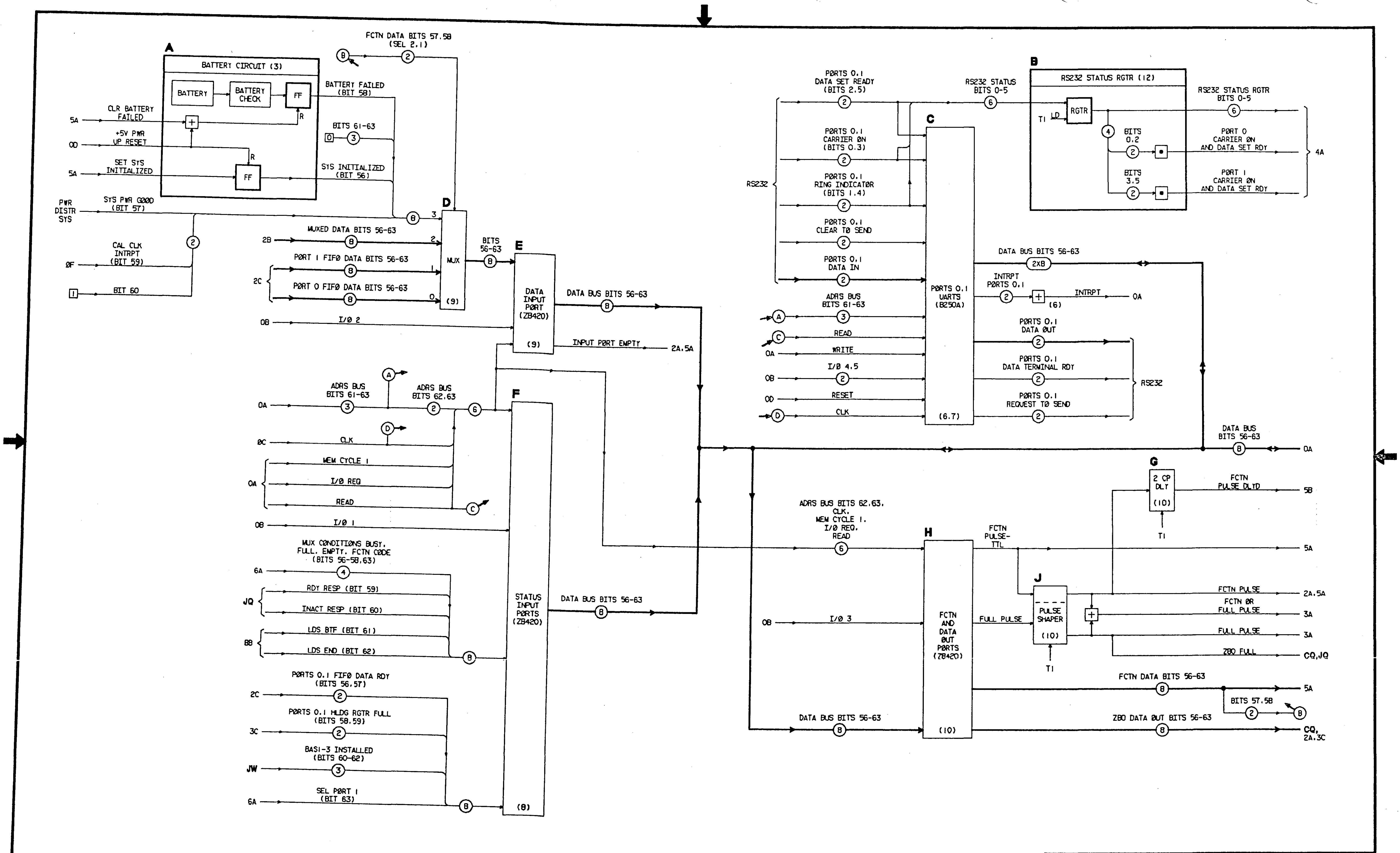
† The Carrier On signal does drop momentarily when the RESET switch is pressed.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JK)
INPUT/OUTPUT PORTS

60463540

REV H

SHEET TPM 3.1

RI BUS DRIVER

All data going from the Z80 to the MAC passes through the RI (Radial Interface) Bus Driver. The Z80 executes reads and writes to the MAC according to the following sequence.

NOTE

> The Hold Function On Channel 17 signal (TPM 3.5B) must be set before the following sequence can occur. When the TPM is in deadstart mode, this signal is held set.

1. The Z80 issues the deselect CC545 data path function to enable connection to the MAC data path.
2. The Z80 Function Decoder sends the Z80 Connect signal to the MAC. This selects the MAC data path; the MAC returns the signal Select RI to Z80 (TPM 3.2B).
3. The Z80 (TPM 3.0A) sends connect code 0 on the data bus to the MAC through the Data Output Port (TPM 3.1H) and RI Bus Driver. This connects the MAC.
4. The Z80 Function Decoder sends the Z80 Inactive signal to the MAC.
5. The Z80 Function Decoder sends the Z80 Next Full Is A Function signal to the MAC.
6. The Z80 sends the read or write function code on the data bus to the MAC through the Data Output Port and RI Bus Driver.
7. The Z80 Function Decoder sends the Z80 Active signal to the MAC to activate the data path.
8. The Z80 sends the first control word on the data bus to the MAC through the Data Output Port and RI Bus Driver. The first control word is ignored.
9. The Z80 sends the second control word through the same path. The second control word identifies which data source the MAC is to access. For example, this may be the register number of a maintenance register, channel status, or a PPM.
10. The Z80 Function Decoder sends Z80 Inactive to the MAC.
11. The Z80 Function Decoder sends Z80 Active to the MAC. This informs the MAC that the Z80 is now waiting for the MAC to perform either a read or write - whichever function the Z80 issued.
12. If the operation is a read, the MAC begins placing bytes onto the Z80/RI data bus. The Z80 reads these bytes through the Display Controller/Radial and Channel 15 Interfaces Mux and the Data Input Port (TPM 3.1E). If the operation is a write, the Z80 sends data to the MAC through the Data Output Port and RI Bus Driver.
13. After the data transfer is complete, the Z80 Function Decoder sends the Z80 Inactive signal to the MAC.
14. The Z80 Function Decoder sends the Z80 Disconnect signal to the MAC.
15. The MAC drops the Select RI to Z80 signal that goes to the Display Controller/Radial and Channel 15 Interfaces. This enables display controller data through the multiplexer in that network.

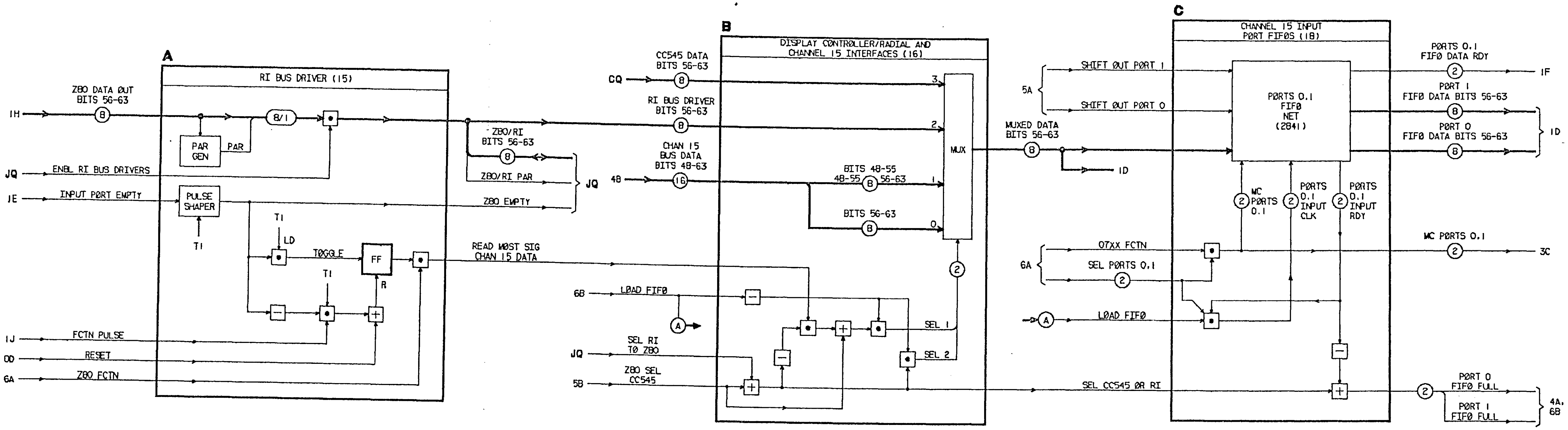
DISPLAY CONTROLLER/RADIAL AND CHANNEL 15 INTERFACES

This network controls which of the following four data paths is selected for the Z80 data bus.

- Bits 48 through 55 from channel 15
- Bits 56 through 63 from channel 15
- MAC data (JQ)
- Display controller data (CQ)

CHANNEL 15 INPUT PORT FIFO BUFFERS

These buffers hold data bytes coming from channel 15 until the Z80 is ready for them. The Z80 is much slower than channel 15 and takes at least 1.6 microseconds to execute an instruction. The FIFO buffers allow the transfer rate to become one megabit per second for up to 64 8-bit bytes. The Port 0 or 1 FIFO Full signal indicates at least one byte is available for the Z80. The $07XX_8$ function clears the FIFO buffers of all data.



CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JK)
CHANNEL 15 INTERFACE

60463540

A

TPN 3.2

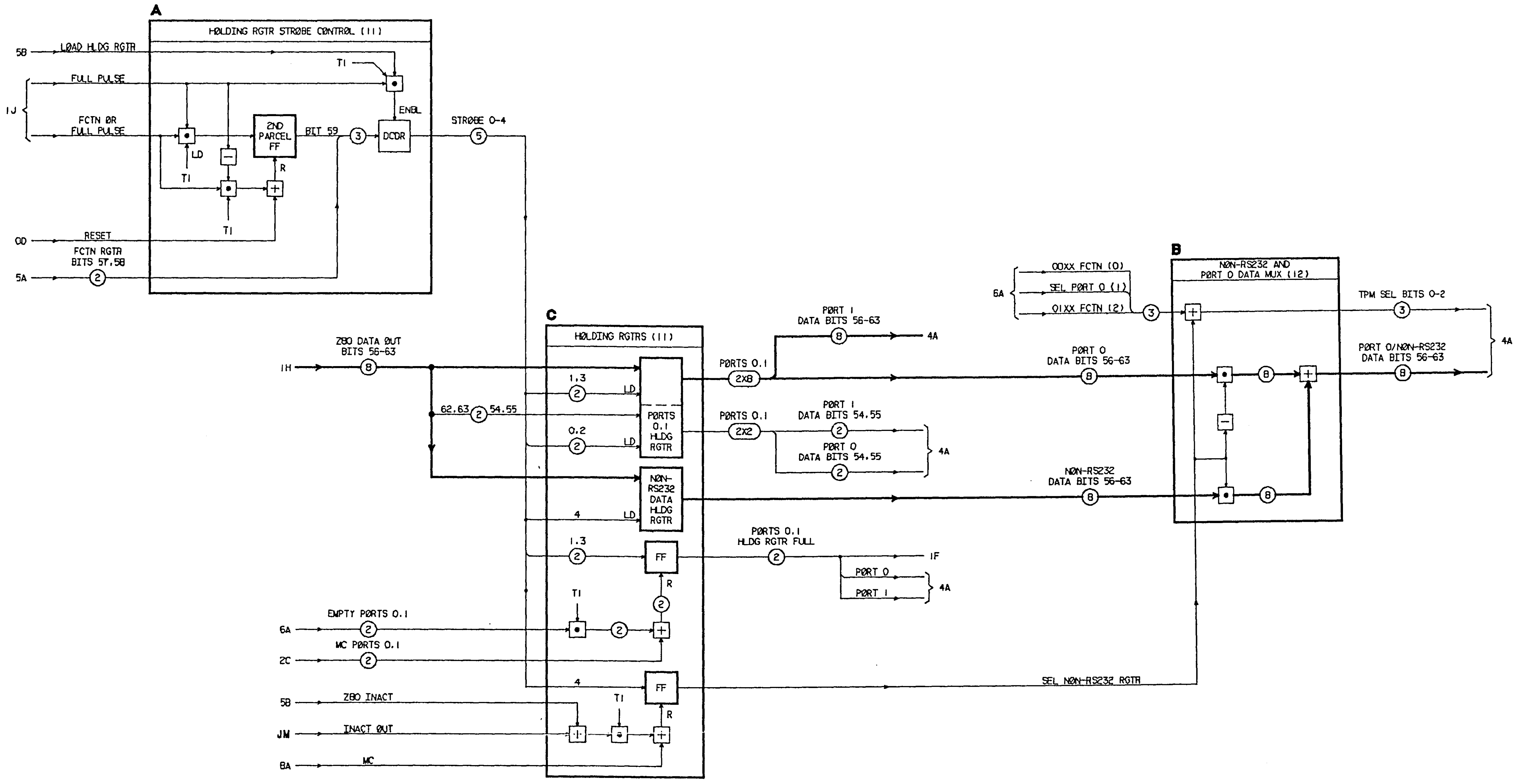
HOLDING REGISTER STROBE CONTROL

Holding register strobe control is needed because the Z80 has only an 8-bit data bus and 10 bits of data go to channel 15 from the Holding Register for either port 0 or port 1. This circuit assembles 8-bit bytes into 10-bit strings. First, a Function Pulse enables writing one of the Holding Registers. This clears the Second Parcel FF, which enables data bits 54 and 55 to be latched. These bits are the overrun and parity error status bits. Next, a Full Pulse sets the Second Parcel FF, which gates the next data byte into bits 56 through 63 of the selected Holding Register.

HOLDING REGISTERS

If data is not from port 0 or port 1, it goes into the Non-RS232 Data Holding Register. Types of non-RS232 data are calendar clock data, predeadstart copies of the P, K, Q, and A registers and predeadstart copies of channel status. In this case, a Function Pulse accompanies every byte of data and keeps the Second Parcel FF clear. This allows data to be constantly gated into the Non-RS232 Data Holding Register.

The Empty Port 0 and Empty Port 1 signals are controlled by channel 15. After a 10-bit string has been transferred, the appropriate empty signal clears the holding register full status to allow the Z80 to write another byte into that Holding Register.



CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

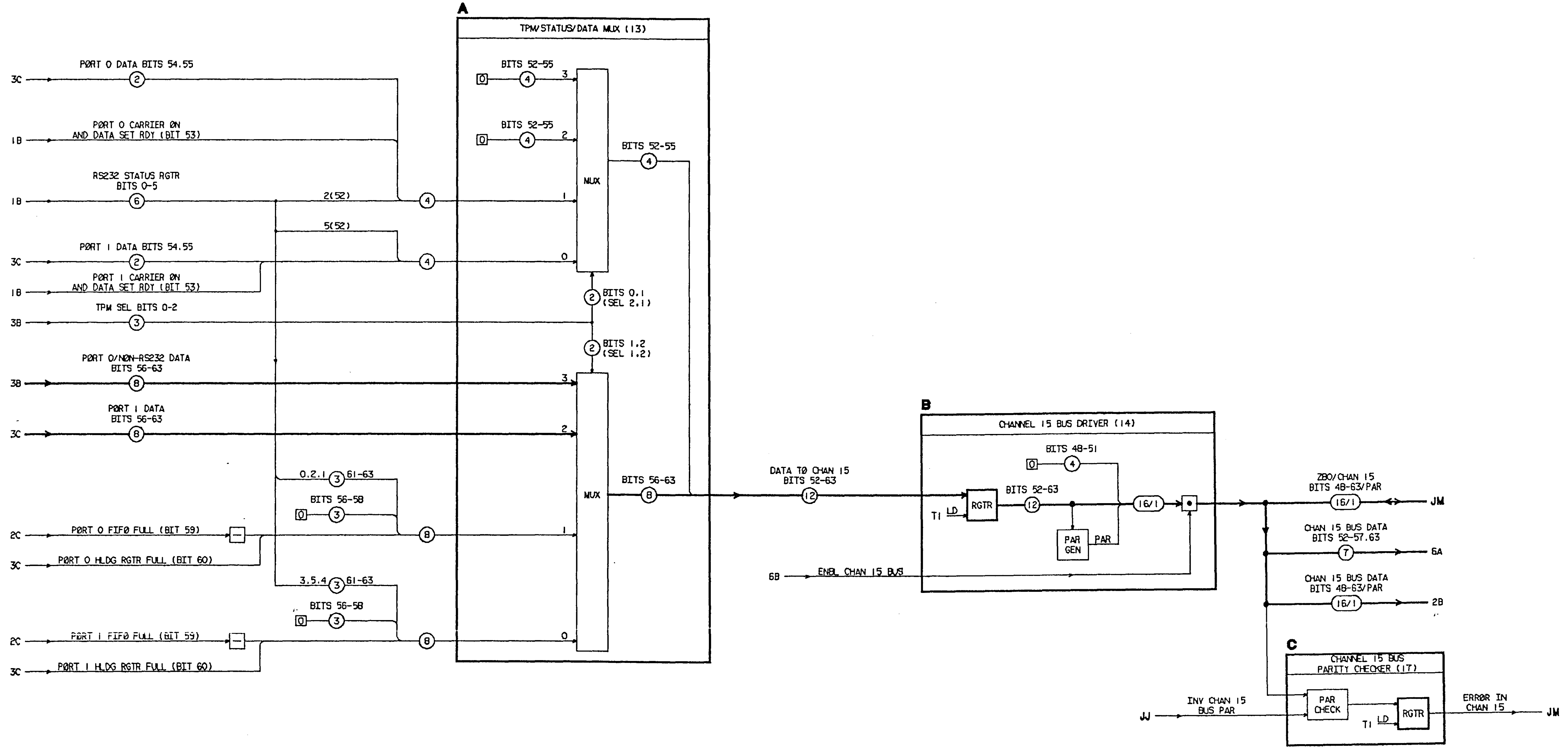
LEVEL 3 DIAGRAM (JK)
Z80 DATA OUT RGTRS,
NON-RS232 AND PORT 0 DATA MUX

DWG NO 60463540
REV A
SHEET TPM 3.3

TPM/STATUS/DATA MUX (JK) (TPM 3.4)

This multiplexer gates data to the Channel 15 Bus Driver from the Port 0 Holding Register, Port 1 Holding Register, and the Non-RS232 Data Holding Register. In addition, the multiplexer also gates the information for the status function ($00XX_8$) to the Channel 15 Bus Driver. Port data consists of eight data bits (56 through 63)and four status bits (52 through 55). Non-RS232 data consists of eight data bits (56 through 63) and four zero bits (52 through 55). Status function information consists of five status bits (59 through 63) and seven zero bits (52 through 58).

TPM Select Bits 0 through 2 determine which set of data is gated through the TPM/Status/Data Mux. If the Z80 issues a non-RS232 data function, data from the Z80 Data Out Port (TPM 3.1H) enters the Non-RS232 Data Holding Register (TPM 3.3C) and sets a FF (Select Non-RS232 Register) that gates that data from the Non-RS232 Data Holding Register through the TPM/Status/Data Mux. If Select Non-RS232 Register is not present, there are three other signals (TPM 3.3B) which determine the selection. These are the 00XX Function, 01XX Function, and Select Port 0. If the $01XX_8$ function is issued and port 0 is selected, data from the Port 0 Holding Register (TPM 3.3C) goes to channel 15. If port 0 is not selected, data from port 1 goes to channel 15. The Z80 issues functions through the Function Output Port (TPM 3.1H) only to gate data to the Port 0 or Port 1 Holding Registers. After data gets to the Holding Registers, the presence of the Select Port 0 and 01XX Function gates data through the multiplexer to the Channel 15 Bus Driver.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JK)
TPM/STATUS/DATA MUX

CODE IDENT	DWG NO	REV
	60463540	A

SHEET	PAGE
TPM 3.4	

Z80 FUNCTION CONVERTER AND TTL DECODER

This circuit handles functions on the transitor-transitor logic (TTL) side of the Z80.

Set System Initialized indicates that the Z80 has detected that +5-V power is good and has started the initialization routine. This signal remains set until +5-V power is turned off.

Clear Battery Failed clears the Battery Failed FF (TMP 3.1A).

Shift Out Port 0 and Shift Out Port 1 control the operation of the Channel 15 Input Port FIFO Buffers (TMP 3.2C). These signals generate the output clock that gates a data word out of the FIFO buffer onto the Z80 data bus.

Second Function Word is used only with the reconfiguration function. This signal alerts the Z80 to the presence of the reconfiguration byte, which is the second function word. The first function word indicates that a write to the PP Reconfiguration Register is to occur. The second function word is the byte that is written into that register.

Z80 FUNCTION DECODER

This decoder generates interface signals for channels 10, 15, and 17.

Z80 Next Full Is A Function is issued by the Z80 before it sends out a function code to the MAC through the RI Bus Driver (TMP 3.2A).

Load Holding Register enables loading a Holding Register (TPM 3.3A).

Z80 Connect establishes the data path between the MAC and the Z80.

Hold Function On Channel 17 disables any PP from issuing any function on channel 17 while the Z80 has control of it.

Hold Function On Channel 10 disables any function on channel 10 while the Z80 has control.

Deadstart Sequence In Progress indicates when the short deadstart is active. This signal generates the deadstart master clear. It is active while the 20_8 words are transferred from the Z80 to PP 0 to execute the short deadstart program.

Long Deadstart In Progress enables the execution of the long deadstart program.

Long Deadstart Status Bit is set when a long deadstart is performed, and remains set until the next deadstart.

Z80 Disconnect disables the data path from the Z80 to the MAC.

Z80 Active and Z80 Inactive are control signals that control the MAC.

Enable Unconditional Idle allows the Z80 to unconditionally idle any of the PPs.

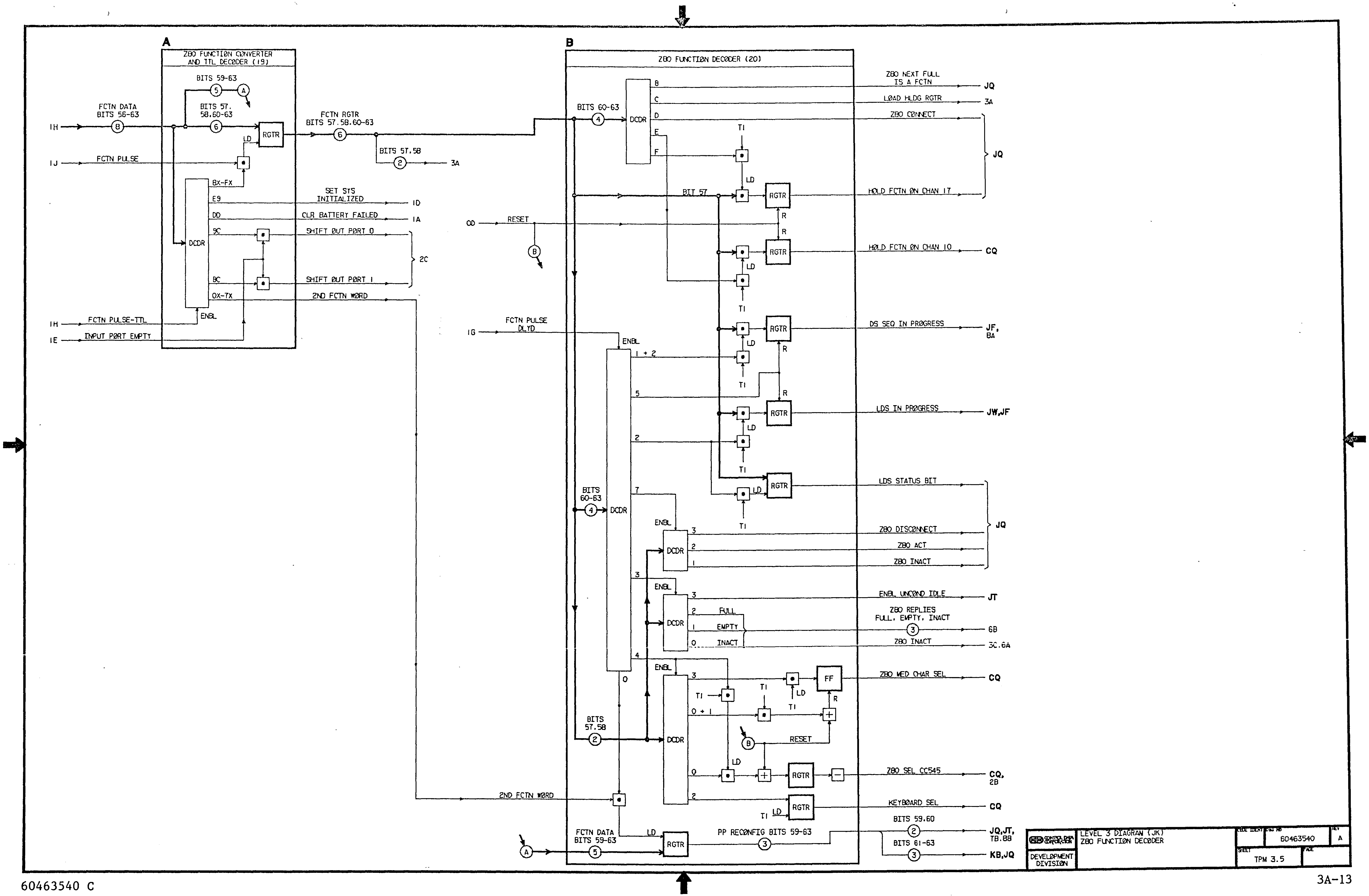
Z80 Reply Full, Z80 Reply Empty, and Z80 Reply Inactive control data transfers with channel 15. Z80 Reply Inactive is also used to respond to a slow channel 15 function.

Z80 Medium Character Select selects the medium size character set of the display controller. If this signal is absent, small characters are selected.

Z80 Select CC545 selects the Z80 data path to the display controller. This signal blocks channel 10 data from going to the display controller.

Keyboard Select allows the Z80 to read keyboard buffer data from the display controller. This signal generates a strobe on the display controller that gates data from the keyboard buffer into a register that is read by the Z80. The Z80 determines whether a key was pressed by checking the data itself. If no key is pressed, the least significant seven bits of the ASCII data are zero. If nonzero, the Z80 knows that a key was pressed and the Z80 brings the data byte into the RAM (TPM 3.0) and begins assembling a word until a carriage return appears. The Z80 then decodes the character string that has come in from the display controller.

PP Reconfiguration Bits 59 through 63 determine which BAS is BAS 0 and which PP is PP 0. Bits 59 and 60 identify BAS 0; bits 61 through 63 identify PP 0. If bits 61 through 63 are zero, physical PP 0 is logical PP 0; or if they decode to one, then physical PP 1 is logical PP 0, and so forth. PP Reconfiguration Bits 59 and 60 also generate the selects for the Deadstart Number Counters (TPM 3.7A).



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JK)
Z80 FUNCTION DECODER

CODE IDENT	DWG NO	REV
	60463540	A

SHEET	PAGE
TPM 3.5	

TPM FUNCTION DECODER

This circuit decodes fast and slow function codes from channel 15. Fast functions are shown in the upper right side. The $7XXX_8$ function is not shown as a separate line but is also decoded. The $7XX1_8$ or $7XX0_8$ function generates the Connected and Select Port 1 or 0 signal. These signals are needed to accomplish the signal interchange (handshaking) for any functions that follow. The Z80 is unable to send inactives, actives, or fulls without the Connected signal.

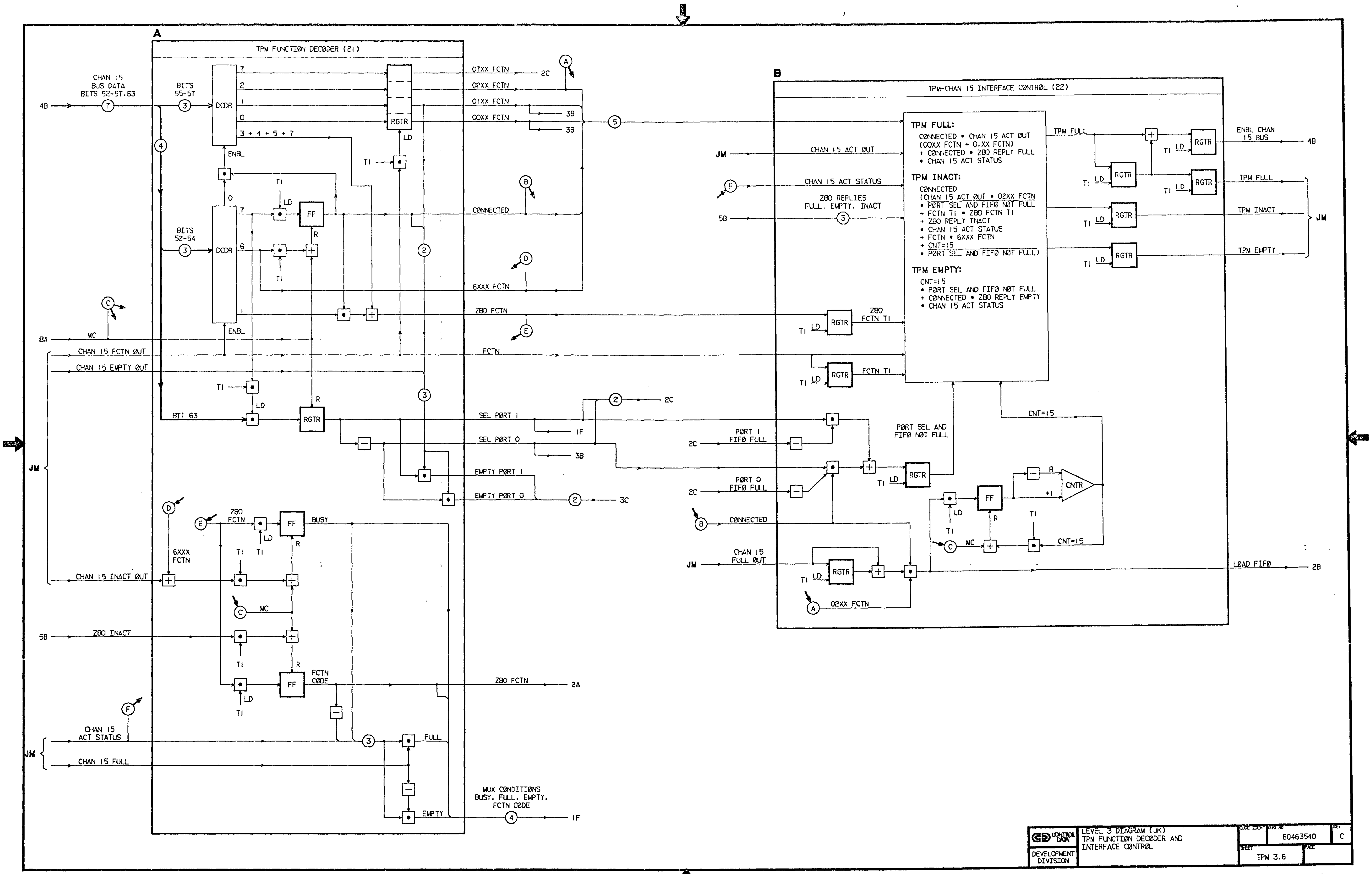
If a function code from channel 15 is not decoded as a fast function, it is considered to be a slow function requiring decoding by the Z80. In this case, the TPM Function Decoder generates the Mux Condition Function Code signal, which the Z80 reads through the Status Input Port (TPM 3.1F). This alerts the Z80 to the presence of a slow function. When the Z80 detects this bit set, it reads the function code on the 12-bit channel 15 data bus. First, the Z80 reads the upper four bits. Then, it reads the least significant eight bits and decodes that function and executes the appropriate microcode routine for the slow function.

The TPM Function Decoder also monitors some channel 15 interface conditions that occur while processing slow functions. These include Channel 15 Active Status, Channel 15 Full, and Channel 15 Empty and Busy.

TPM - CHANNEL 15 INTERFACE CONTROL

The inputs to this circuit are generated by hardware (fast function), by microcode (slow function), or a data transfer. The Connected signal must be present for any signal interchange to take place on the TPM/channel 15 interface.

The counter shown at the bottom determines whether the Channel 15 Input Port FIFO Buffers (TPM 3.2C) can accept more data. This counter increments for 800 nanoseconds. After 800 nanoseconds, the circuit samples the FIFO Full signal. If a FIFO buffer is still full after 800 nanoseconds, that FIFO buffer is completely full. The 800 nanoseconds should have been enough time for the word just written into the FIFO buffer to advance to the next location and drop the FIFO Full signal. In this case, 64 words have been written into the buffer and TPM Inactive is generated instead of TPM Empty. However, if by the end of 800 nanoseconds the FIFO is not full, the byte has advanced and TPM Empty is generated. Channel 15 is then able to send another word to the FIFO buffer. The byte that fills up the FIFO buffer generates TPM Inactive.



CD CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JK)
TPM FUNCTION DECODER AND INTERFACE CONTROL
DWG NO 60463540
REV C
SHEET TPM 3.6

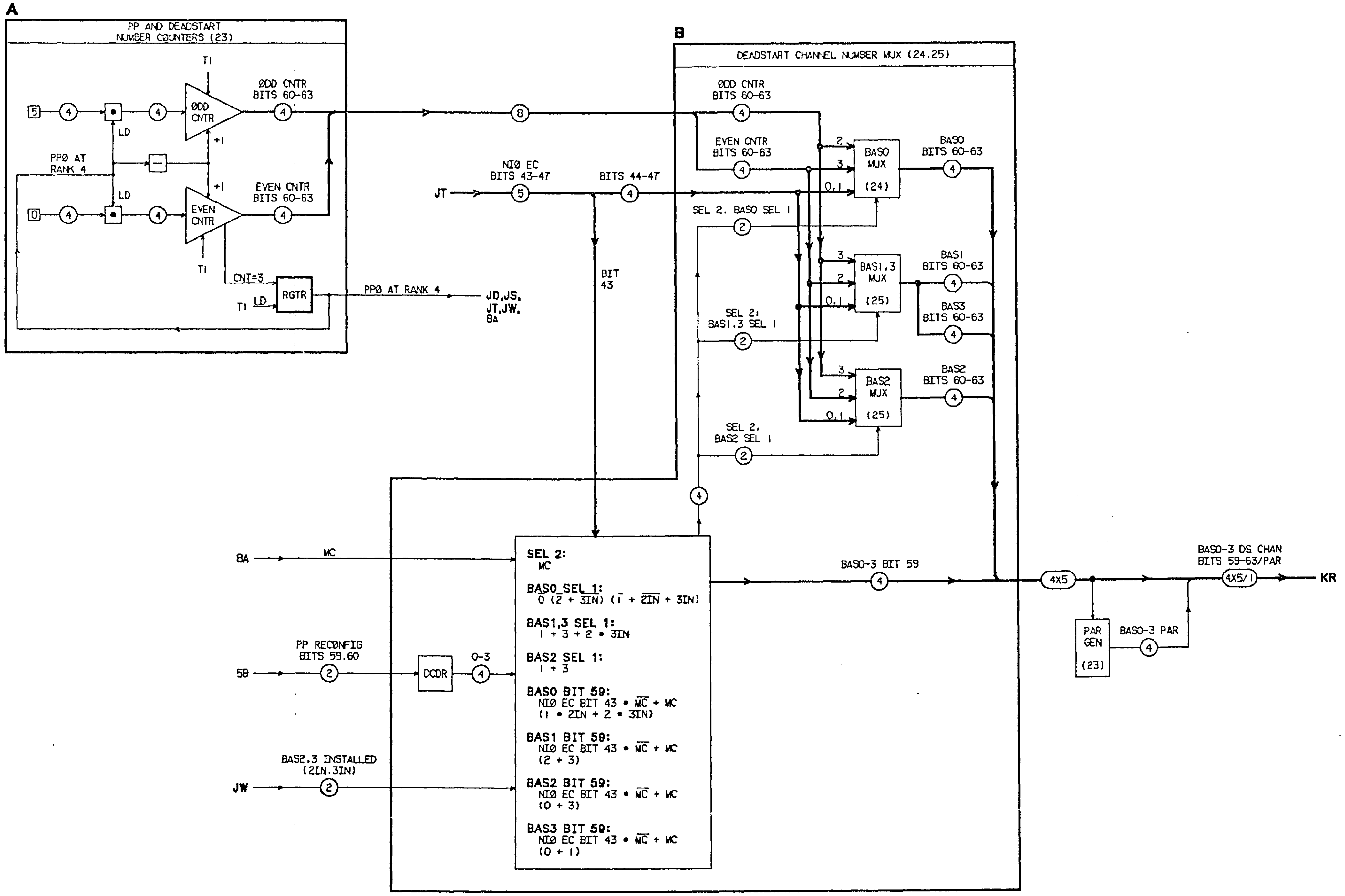
PP AND DEADSTART NUMBER COUNTERS

These are free-running counters that operate constantly. The outputs of these counters are gated out to the PP Q registers when Deadstart Master Clear is generated during the deadstart sequence. Two different combinations of numbers can be gated out. Odd Counter Bits 60 through 63 contain numbers for the odd barrels. These are numbers 5_8 through 11_8. Even Counter Bits 60 through 63 are for even barrels and correspond to the numbers 0 through 4_8. Bit 59 is determined completely by PP reconfiguration bits 59 and 60. Numbers 0 through 4_8 remain the same or change to 20_8 through 24_8. Likewise, numbers 5_8 through 11_8 may change to 25_8 through 31_8.

The PPO At Rank 4 signal (a 4-MHz clock pulse) synchronizes all barrels and slots.

DEADSTART CHANNEL NUMBER MUX

This multiplexer determines which PP numbers go to which physical barrels and are entered into the Q bits for the PPs in those barrels. When no Deadstart Master Clear is present, the channel number bits are gated through from the NIO Environmental Control bits 43 through 47. When Deadstart Master Clear is present, the channel number bits come from the PP and Deadstart Number Counters.



CONTROL DATA CORPORATION

DEVELØPMENT DIVISIØN

LEVEL 3 DIAGRAM (JK)
DEADSTART CHANNEL
NUMBER SELECTØR

CODE IDENT | DWG NO 60463540 | REV A
SHEET TPM 3.7 | PAGE

MASTER CLEAR GENERATOR

Master Clear determines whether the channel number bits are going to be gated from the JT board or from the Deadstart Number Counters (TPM 3.7A). The Deadstart Sequence In Progress signal produces Master Clear.

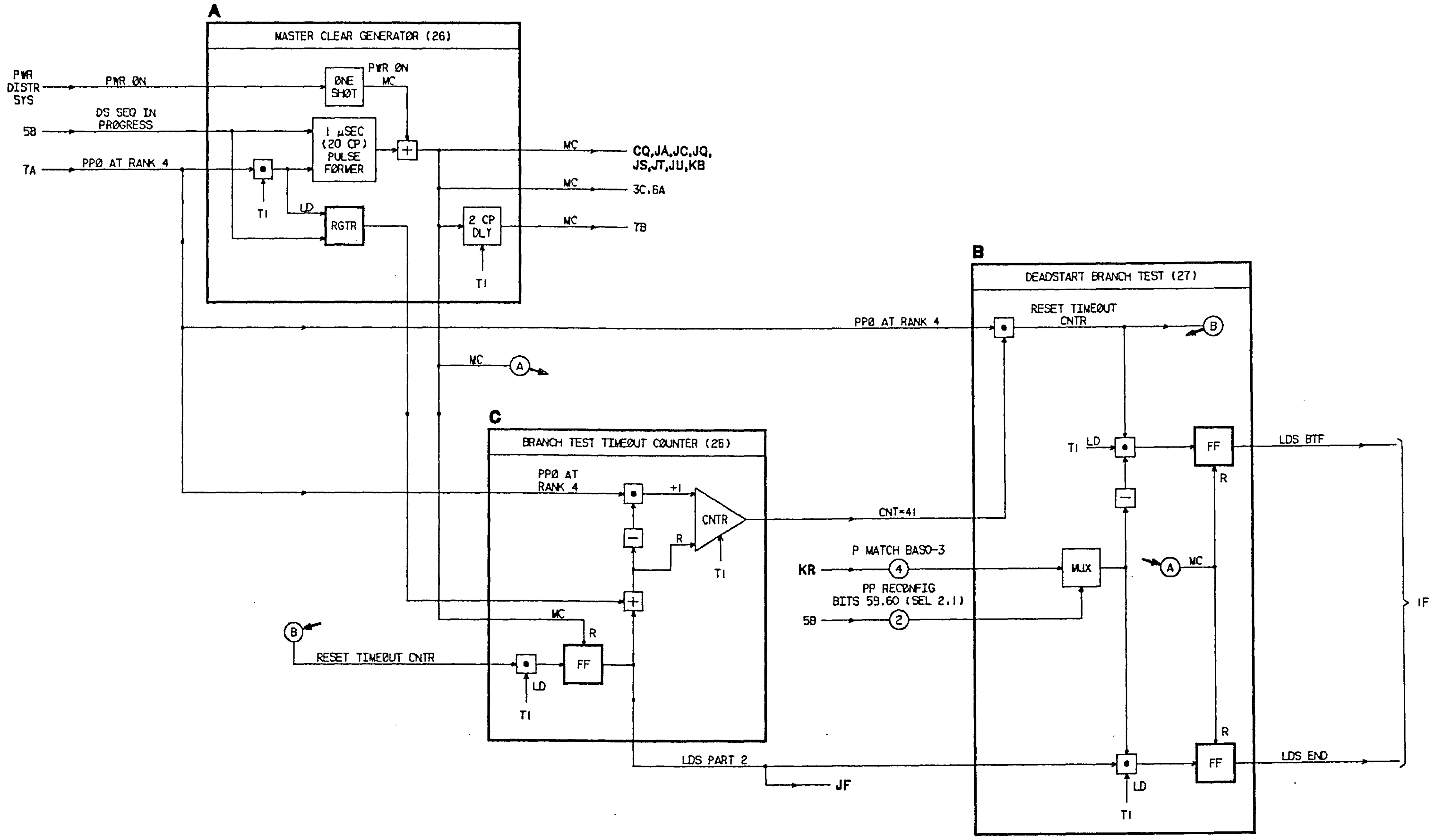
BRANCH TEST TIMEOUT COUNTER

This counter counts to 41. By the time it reaches 41, the long deadstart program should reach address 6200_8 in the unconditional branch test and send back a P Match signal. These conditions generate Reset Timeout Counter.

DEADSTART BRANCH TEST

P Match (BAS 0 through 3) enables the Long Deadstart Branch Test Failed FF. If the count of the Branch Test Timeout Counter goes to 41 and P Match exists, no long deadstart branch test failure occurred. The P Match signals originate from physical BAS 0 through 3. Only one of these is selected, depending on PP Reconfiguration Bits 59 and 60. These bits select the physical BAS, which is logical BAS 0. Count Equals 41 generates the Reset Timeout Counter signal, which then generates Long Deadstart Part 2, which enables the second part of a long deadstart sequence. It also generates the Long Deadstart End signal.

While a long deadstart is running, the Z80 checks for errors. First the Z80 checks whether the long deadstart program has successfully been transferred from the Z80 EPROMs (TPM 3.0) to PPM 0. This occurs after the Z80 transfers that program. A transfer error prevents a short deadstart from being executed after the attempted long deadstart program. If no transfer error occurred in the long deadstart, the Z80 checks for a Long Deadstart Branch Test Failure. If this failure has not occurred, Long Deadstart End is set and the Z80 checks for a status summary error. Then the Z80 checks for the PP address equal to 7761_8, which is the last address in the long deadstart program. The Z80 does this by having the MAC read the PP registers for BAS 0. Then the Z80 checks the P register for PP 0 and BAS 0 for address 7761_8. The Z80 executes a short deadstart sequence when P equals 77618, no errors are detected, and Long Deadstart End is set.



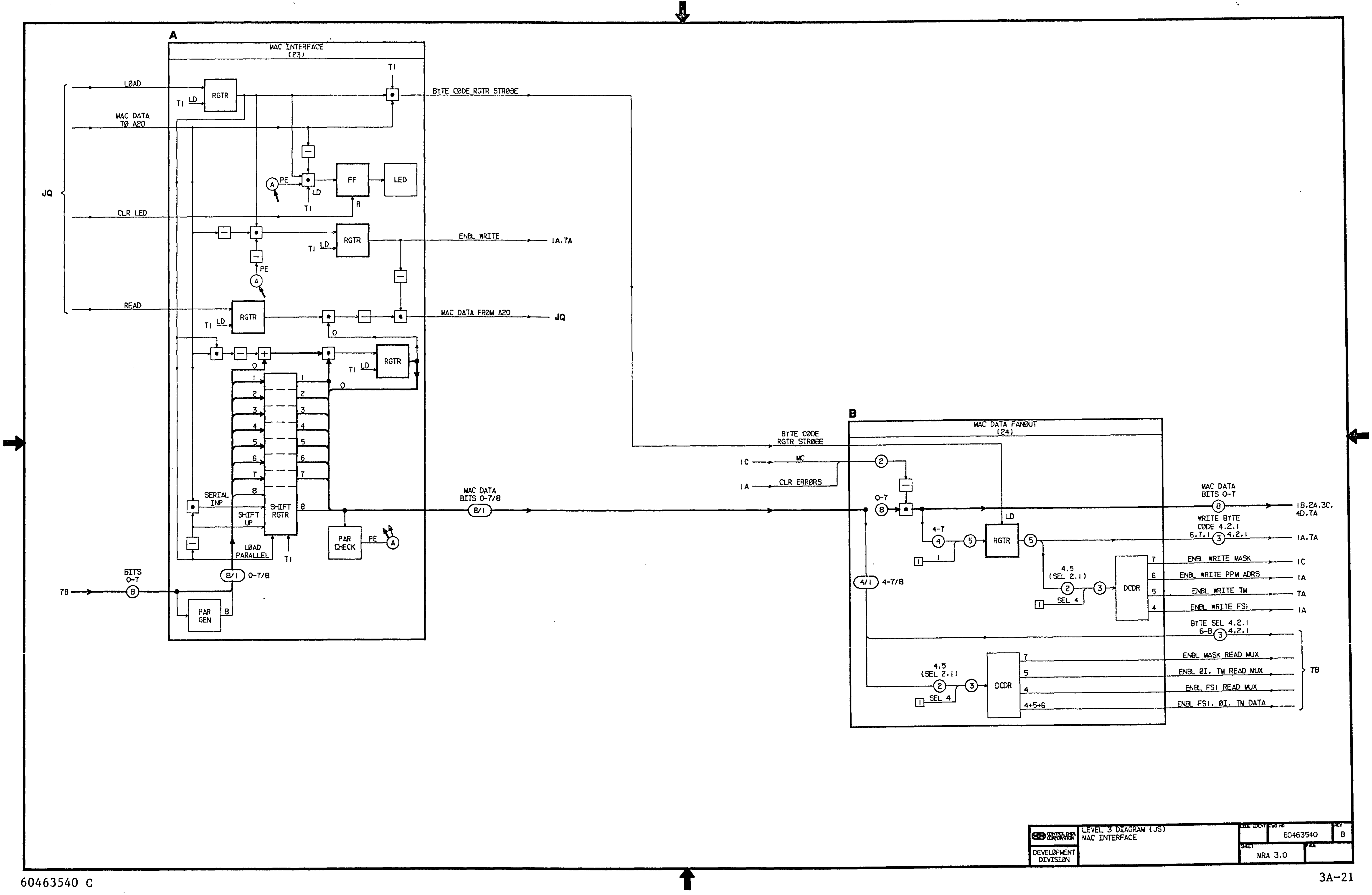
CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JK)
MASTER CLEAR GENERATOR
AND DEADSTART BRANCH TESTER

CODE IDENT	DWG NO	REV
	60463540	A

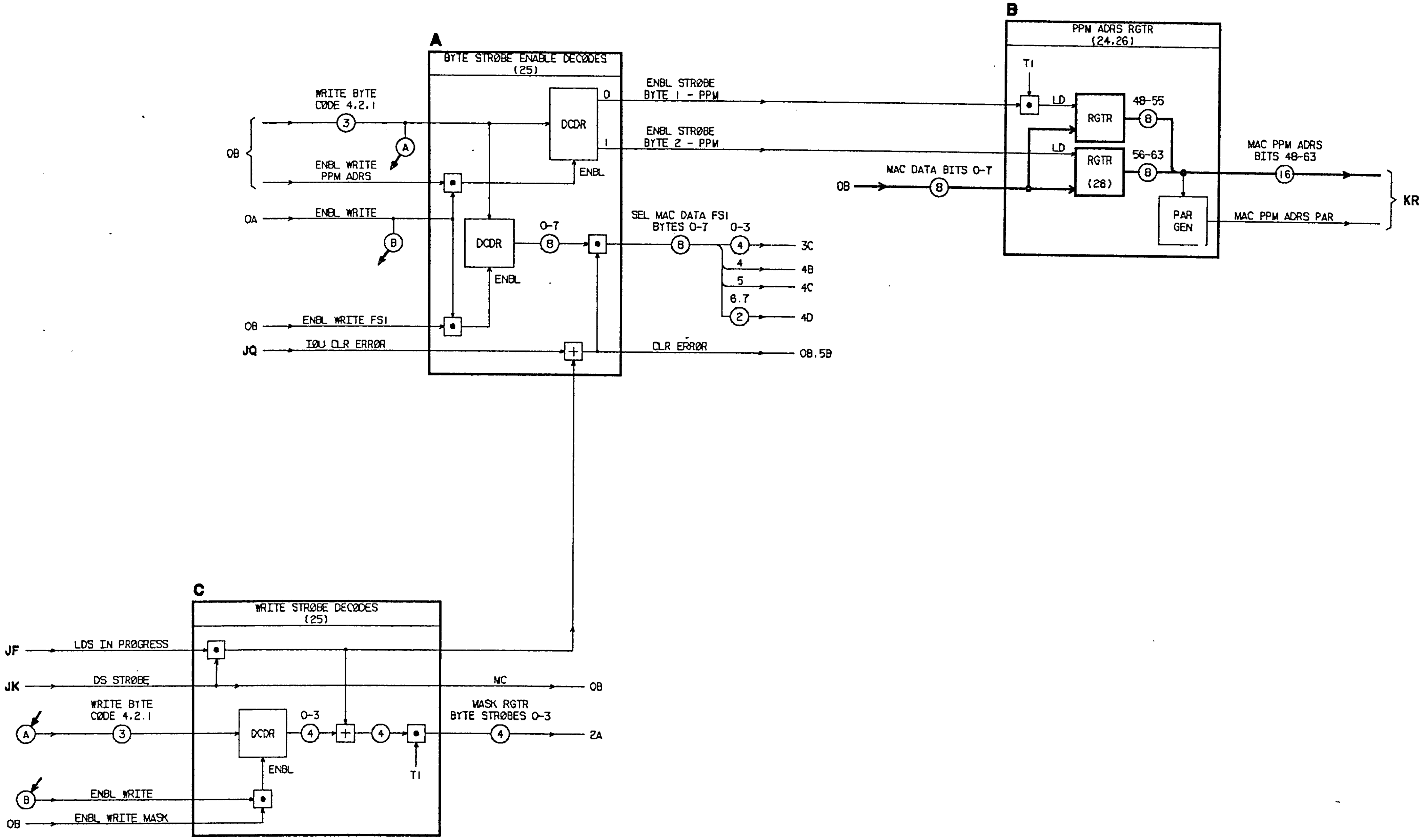
SHEET	PAGE
TPM 3.8	



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JS)
MAC INTERFACE

60463540
B
MRA 3.0

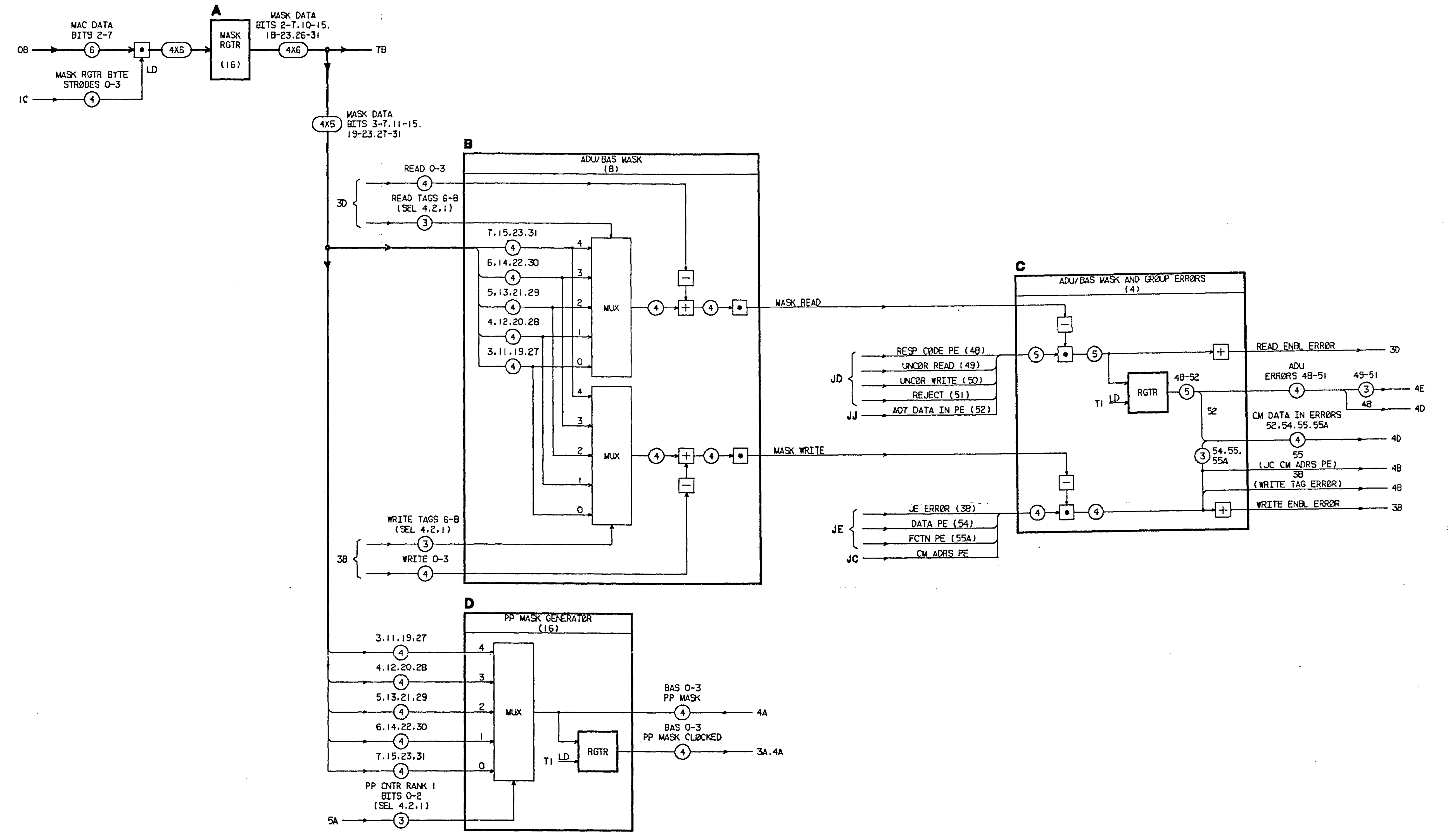


CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JS)
STROBE DECODERS AND
PPM ADRS RGTR

CODE IDENT	DWG NO	REV
	60463540	A

SHEET	PAGE
MRA 3.1	

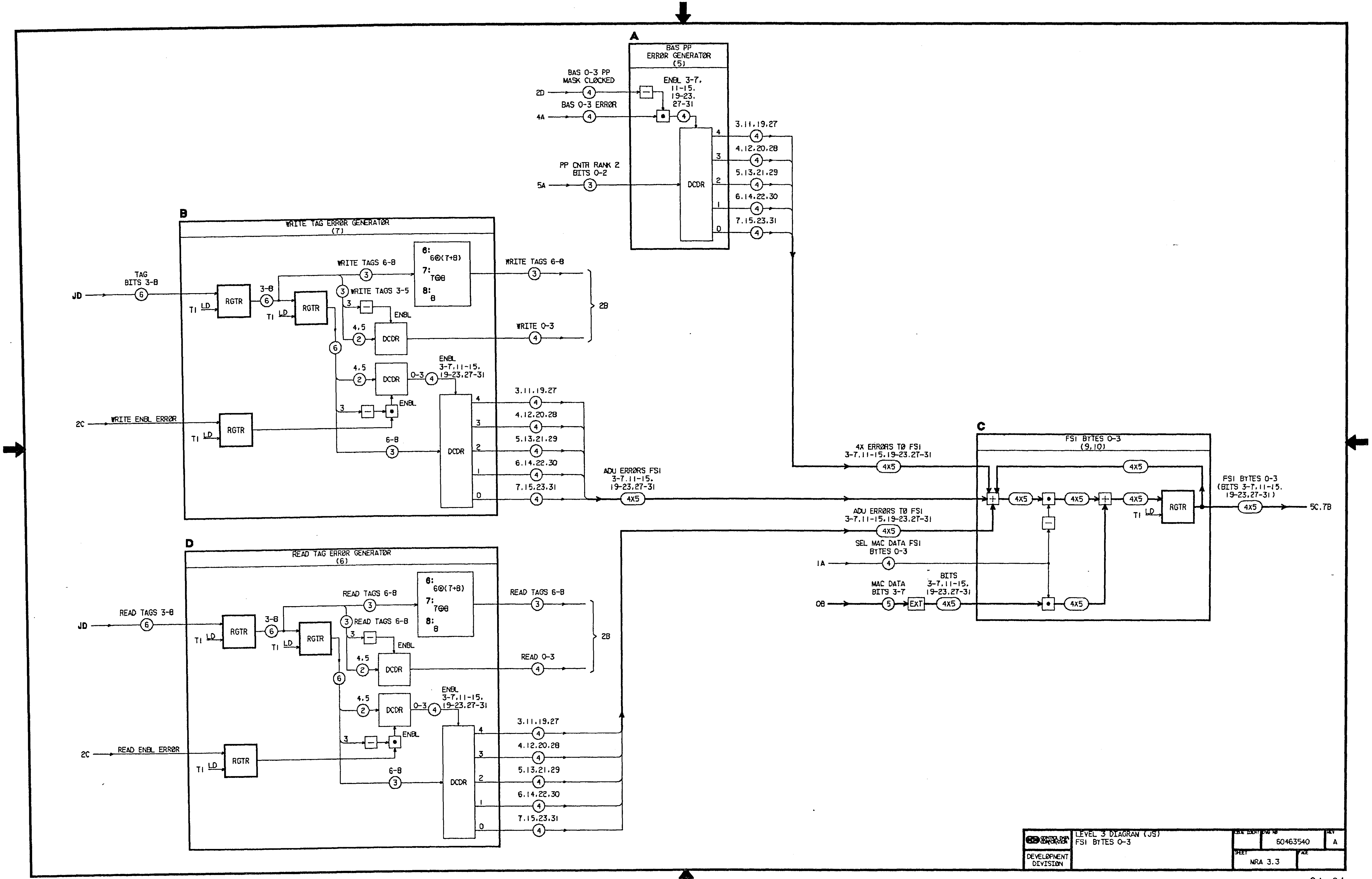


CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

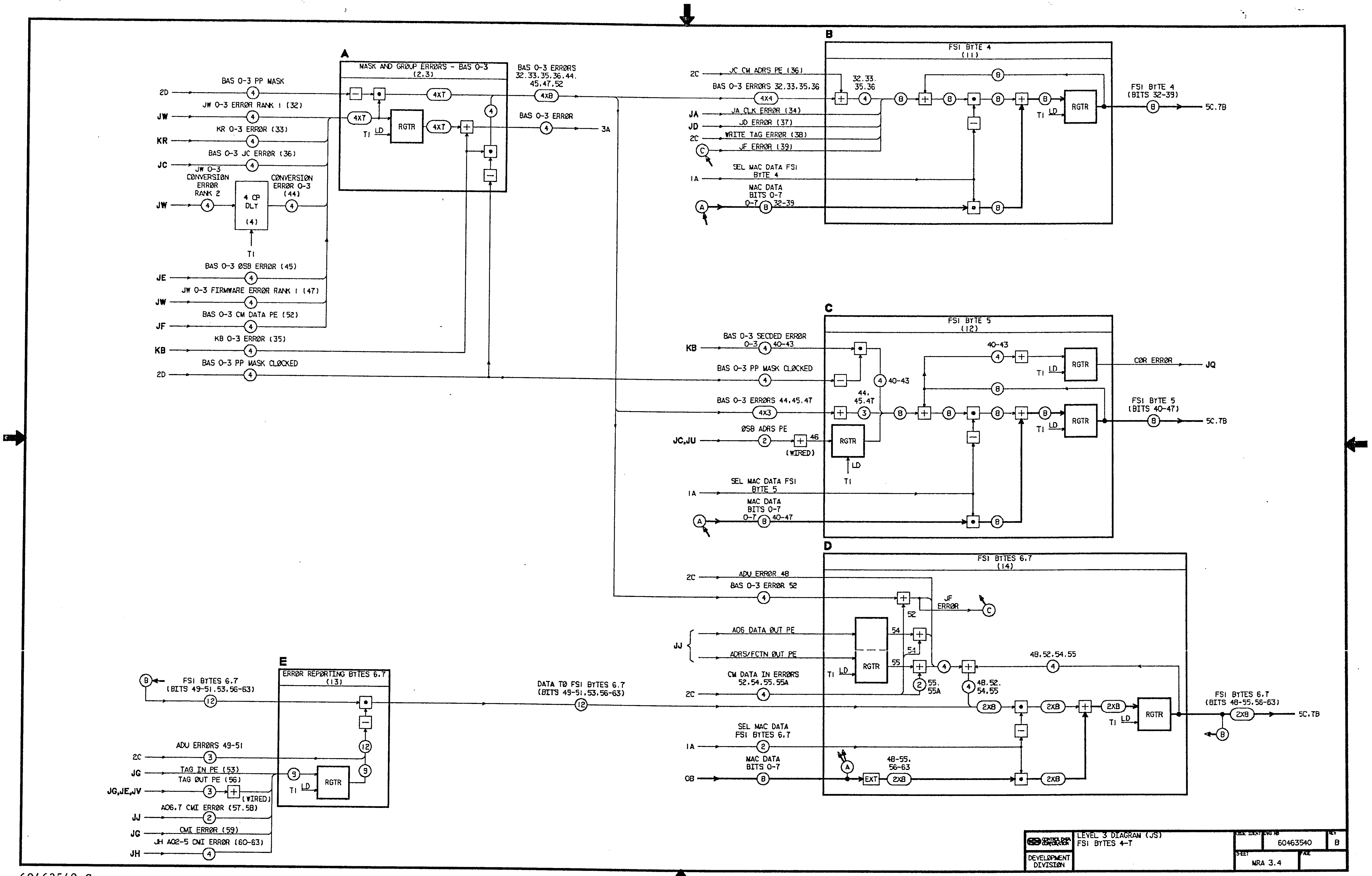
LEVEL 3 DIAGRAM (JS)
MASK NETWORK

CODE IDENT	DWG NO	REV
	60463540	B

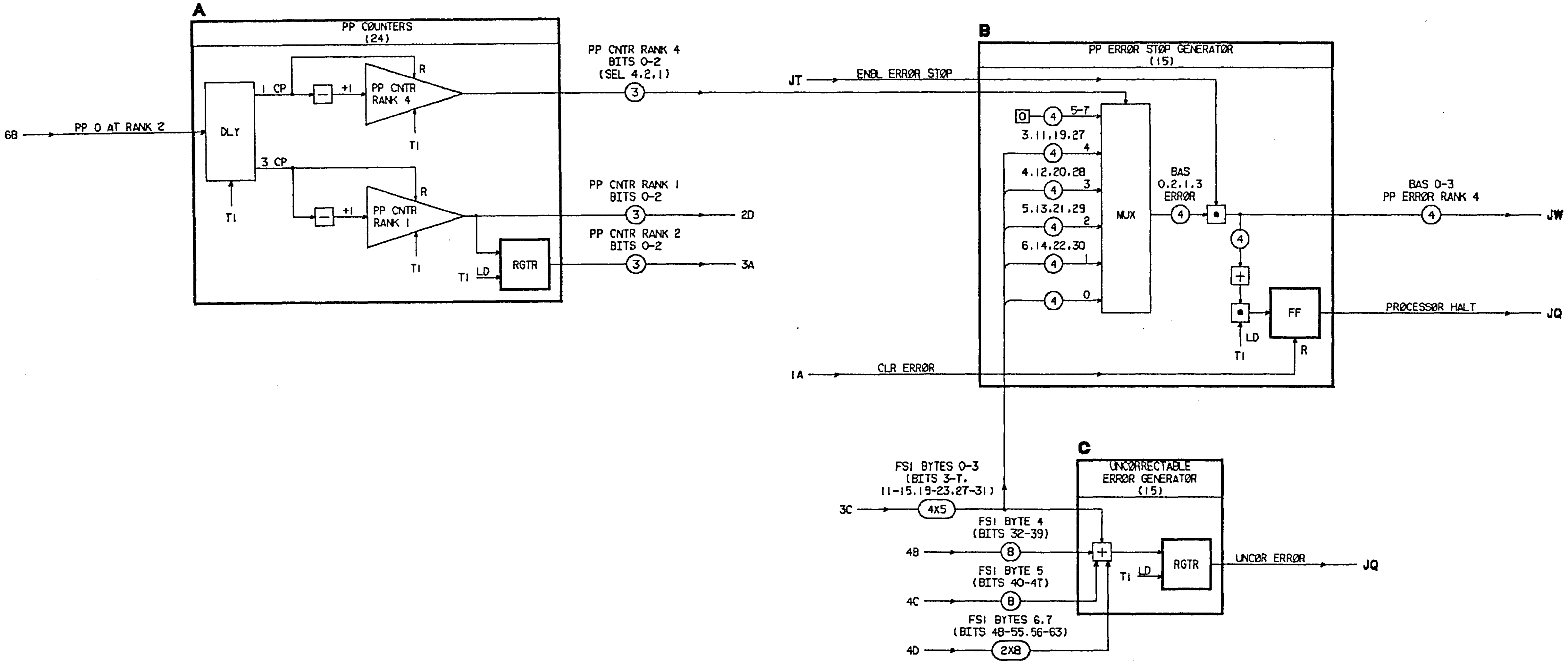
SHEET	PAGE
MRA 3.2	


A
BAS PP ERRØR GENERATØR (5)
BAS 0-3 PP MASK CLØCKED
2D
BAS 0-3 ERRØR
4A
ENBL 3-7, 11-15, 19-23, 27-31
PP CNTR RANK 2 BITS 0-2
5A
DCDR
3,11,19,27
4,12,20,28
5,13,21,29
6,14,22,30
7,15,23,31
B
WRITE TAG ERRØR GENERATØR (7)
TAG BITS 3-8
JD
RGTR
TI LD
3-8
WRITE TAGS 6-8
WRITE TAGS 3-5
6: 6⊕(7+8)
7: 7⊕8
8: 8
ENBL
4,5
DCDR
WRITE 0-3
2B
ENBL 3-7,11-15, 19-23,27-31
0-3
2C
WRITE ENBL ERRØR
6-8
ADU ERRØRS FSI 3-7,11-15, 19-23,27-31
4X5
C
FSI BYTES 0-3 (9,10)
4X ERRØRS TØ FSI 3-7,11-15,19-23,27-31
ADU ERRØRS TØ FSI 3-7,11-15,19-23,27-31
SEL MAC DATA FSI BYTES 0-3
1A
MAC DATA BITS 3-7
0B
EXT
BITS 3-7,11-15, 19-23,27-31
FSI BYTES 0-3 (BITS 3-7,11-15, 19-23,27-31)
5C,7B
D
READ TAG ERRØR GENERATØR (6)
READ TAGS 3-8
READ TAGS 6-8
READ 0-3
READ ENBL ERRØR

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 3 DIAGRAM (JS)
FSI BYTES 0-3
60463540
A
NRA 3.3



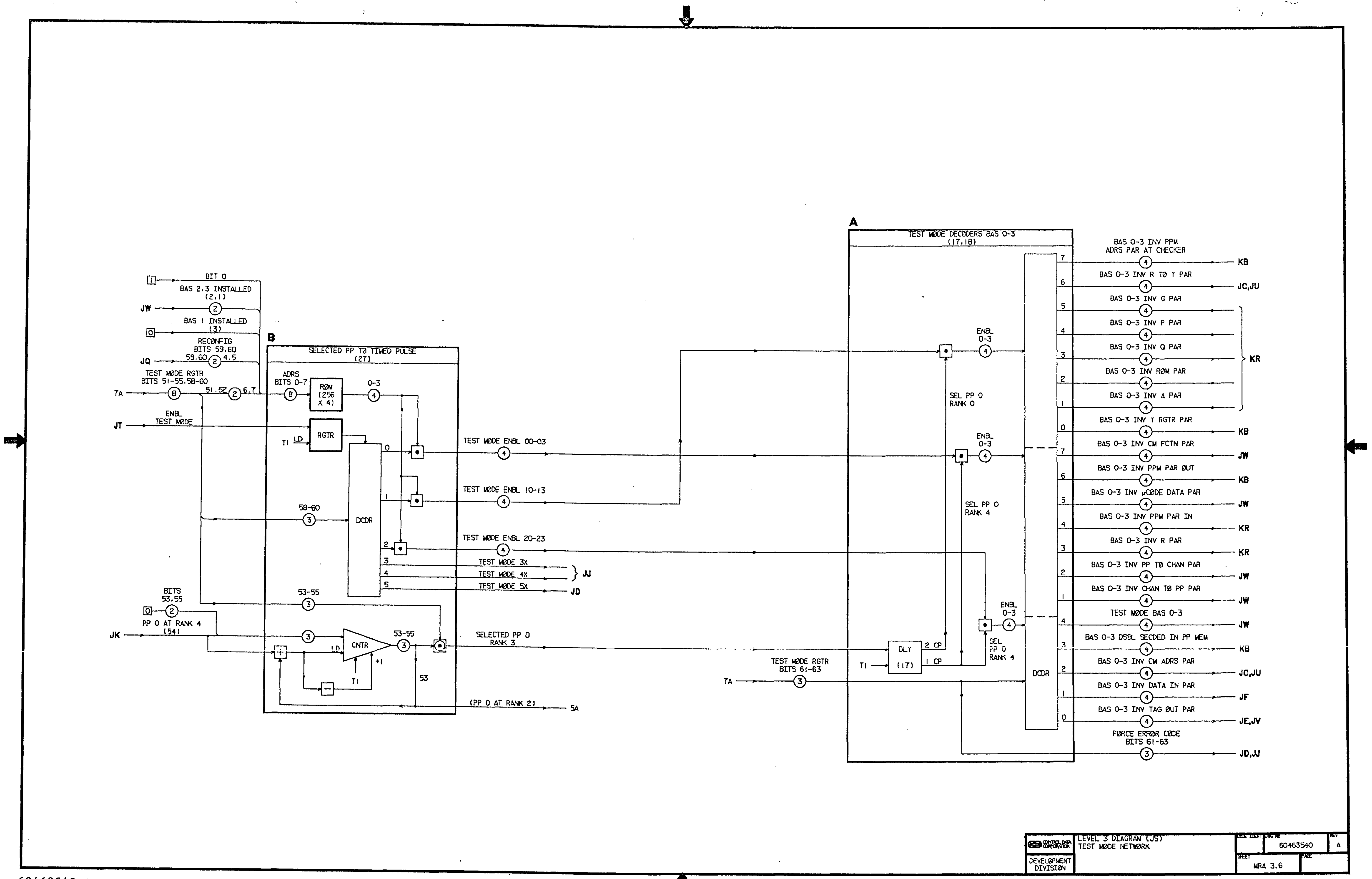
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JS)
FSI BYTES 4-7
60463540
B
MRA 3.4



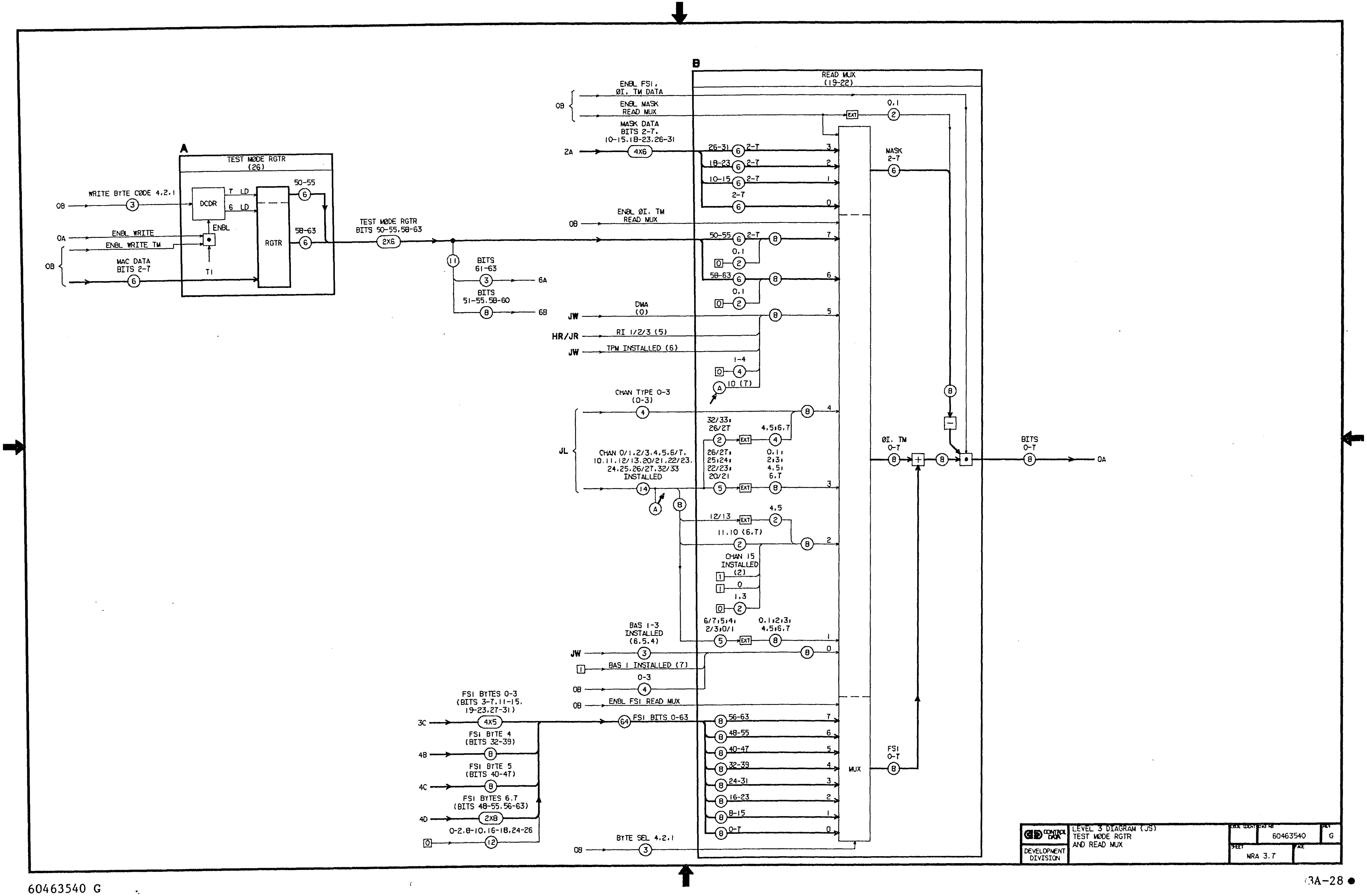
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JS)
PP COUNTERS AND ERROR
STOP GENERATOR

CODE IDENT	DWG NO	REV
	60463540	A
SHEET	PAGE	
MRA 3.5		



CONTROL DATA CORPORATION
LEVEL 3 DIAGRAM (JS)
TEST MODE NETWORK
DEVELOPMENT DIVISION
60463540
A
NRA 3.6



CONTROL DATA

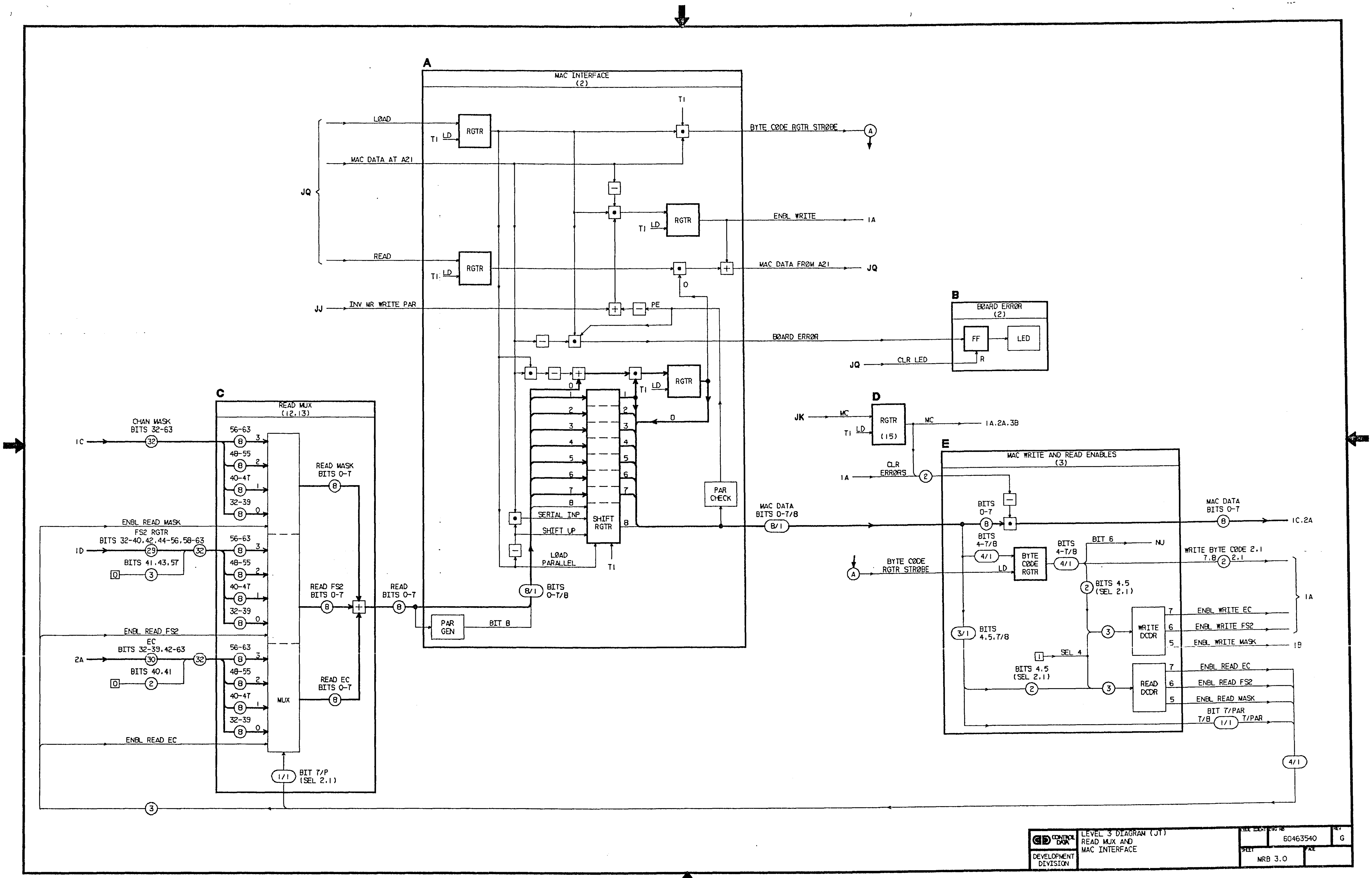
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JS)
TEST MODE RGTR
AND READ MUX

60463540

G

SHEET NRA 3.7

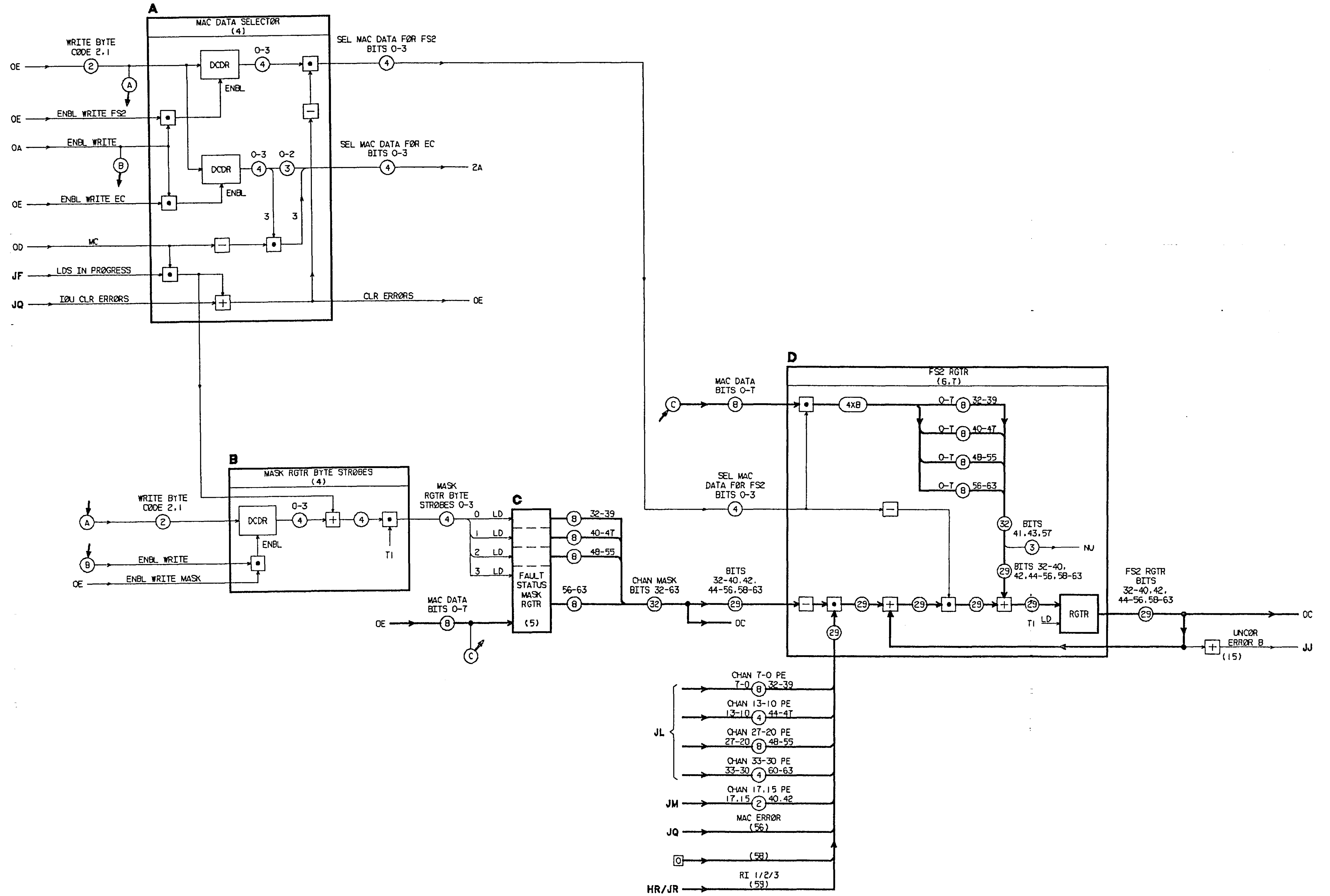


CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
READ MUX AND
MAC INTERFACE

60463540 G

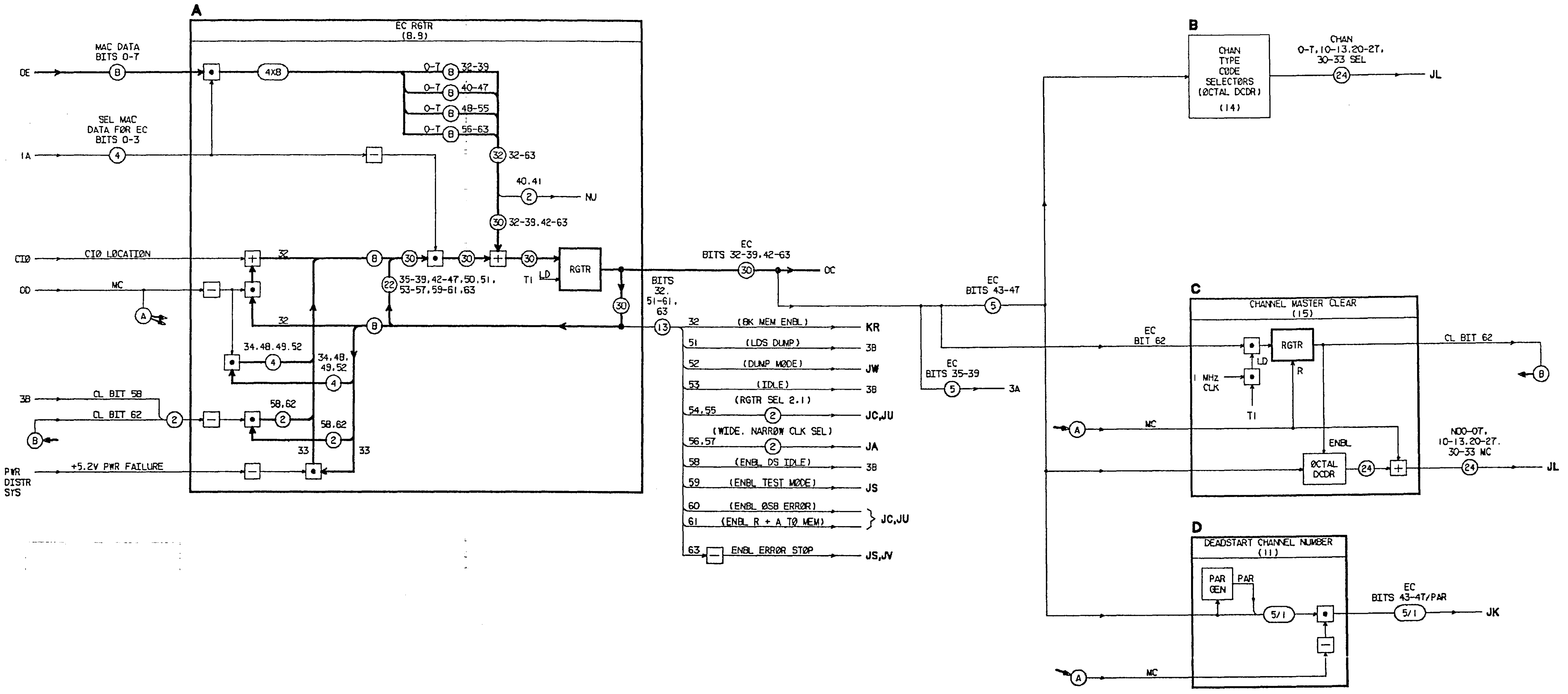
MRB 3.0



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
MASK NETWØRK AND
FS2 RGTR

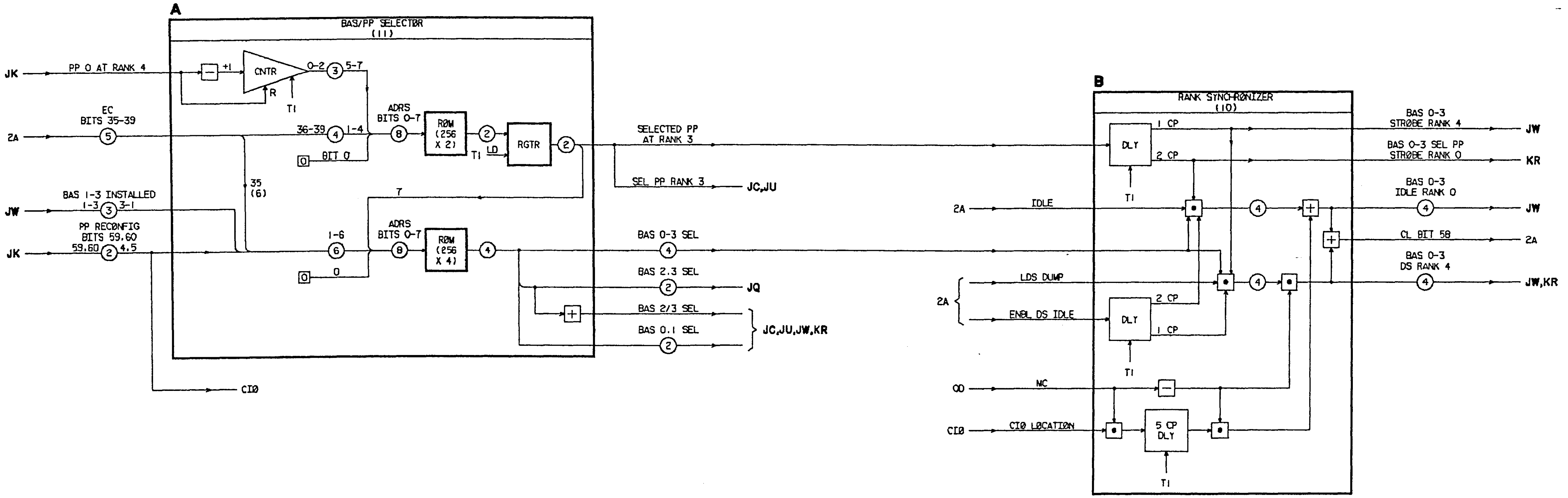
60463540 G
MRB 3.1



CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 3 DIAGRAM (JT)
EC RGTR AND
CHANNEL SELECTIØN

CODE IDENT
DWG NO 60463540
REV A
SHEET MRB 3.2
PAGE



CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
BAS/PP SELECTOR AND
RANK SYNCHRONIZER

60463540

A

NRB 3.3

To present the information in this chapter in a structured format, this page has been left blank.

CONNECT CODE REGISTER

The Connect Code Register circuits determine when a connect code requiring MAC intervention is being issued. Such a condition exists when:

- The Channel 17 Function signal is active. This signal from the JM board indicates that a PP is issuing a function word over channel 17. Assuming no Hold Function On Channel 17 is being generated, this results in the Function In and Strobe Select Code signals being generated. These signals cause the MAC to recognize the function word and decode the connect code within bits 52 through 55 of the word (MAC 3.2B). If Hold Function On Channel 17 is being generated, the TPM is using the MAC and channel 17 functions are disabled.

- The Z80 Connect To RI signal is active. This signal from the TPM indicates it is connecting to the MAC. This and an accompanying Z80 Full signal generates the Strobe Select Code signal. Strobe Select Code enables the decoding of the connect code from the TPM. In addition, the Z80 Connected, Select RI, Z80 Select, and Select Z80 signals are generated. These signals condition various circuits for the pending data exchange. These signals remain set until the transfer has been completed and the TPM disconnects from the MAC.

Z80 AND MCH CONTROL MUX

This circuit provides the Z80 Response Control circuits (MAC 3.1A) with the current I/O status from either channel 17 or the TPM. The multiplexer provides the I/O status from channel 17 except when the TPM connects to the MAC. Then the multiplexer provides the I/O status of the TPM until the TPM disconnects. The I/O status information provided includes full, empty, active, and inactive indications plus the following.

- Z80 Inactive Reset - Generated during a MAC operation with the TPM when the TPM is sending a function word or when it generates the Z80 Active signal. The Z80 Active signal instructs the MAC to start the function that the TPM has specified.

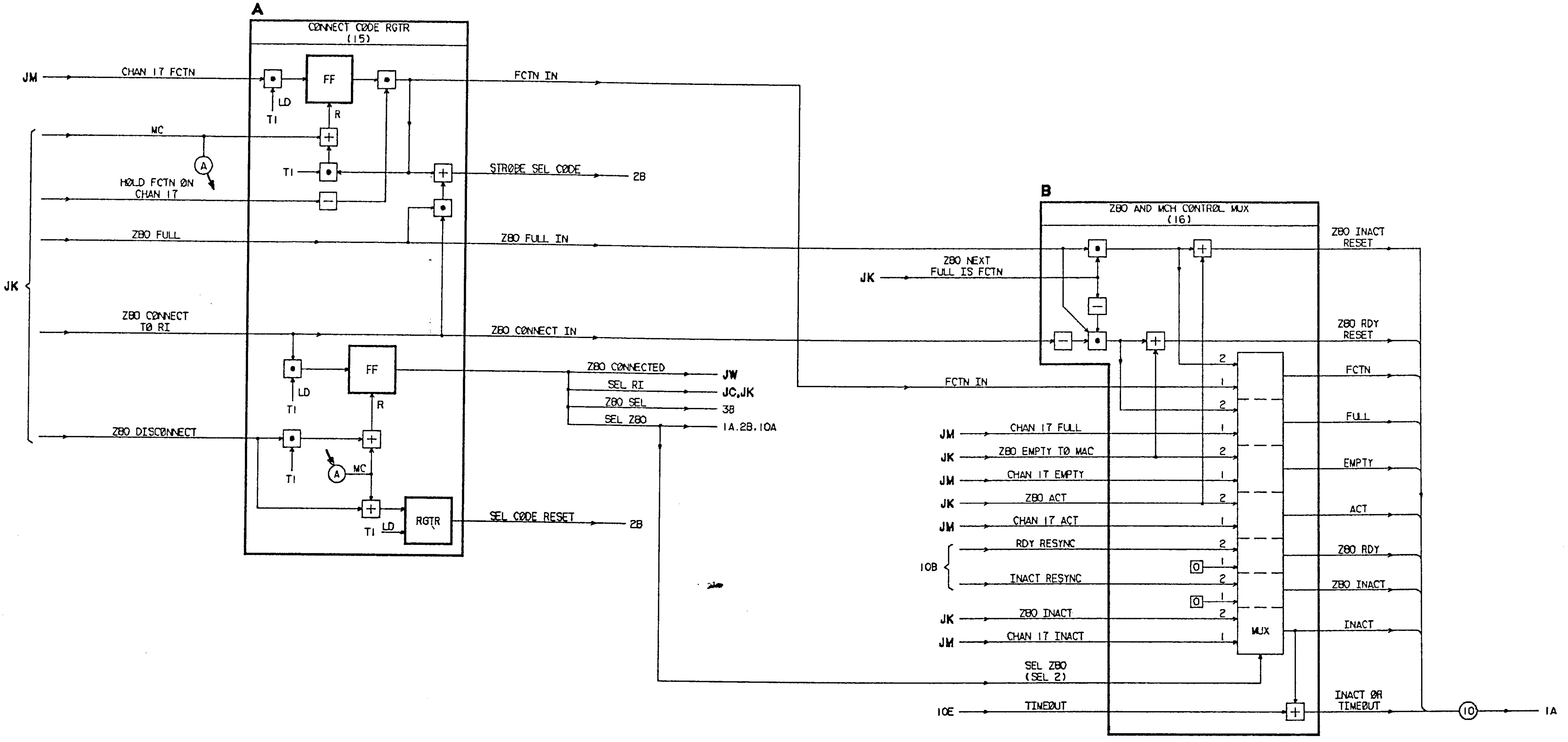
- Z80 Ready Reset - Generated during a MAC operation with the TPM when the TPM is sending/receiving a data word.

- Function - Generated during a MAC operation with the TPM when the TPM is sending a function word (Z80 Full In signal active and Z80 Next Full Is Function signal active); or generated when a PP addresses channel 17 and issues a function word.

- Z80 Ready - Generated when the MAC has either accepted a word or is sending a word during a data exchange.

- Z80 Inactive - Generated during a MAC operation with the TPM after the TPM has sent the MAC a function word.

- Inactive or Timeout - Generated during a MAC operation with the TPM or with a PP when the TPM or connected PP has sent an inactive indication following the last control or data word in the exchange; or generated when the MAC has not received a response from the connected PP for 100 milliseconds.



CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JQ)
CONNECT CODE RGTR.
Z80 AND MCH
CONTROL MUX

CODE IDENT	DWG NO	REV
	60463540	A

SHEET	PAGE
MAC 3.0	

Z80 RESPONSE CONTROL

These circuits send responses to the TPM, pass I/O status to the RIs, and determine whether the device accessing MAC is in input or output mode.

RESPONSES SENT TO TPM

The responses sent to the TPM include:

- Ready Response - Currently not used by the TPM.
- Inactive Response - Currently not used by the TPM.
- Enable RI Bus - Enables data from the MAC to be transferred to the TPM during a TPM/MAC operation.

I/O STATUS PASSED TO RIS

The Z80 Response Control circuits pass the I/O status indicators that follow to the HR/JR board. Effectively, these indicators reflect the I/O status of a PP that is connected to channel 17 for the purpose of performing an I/O exchange with the CPU MAC unit or memory MAC unit. The HR/JR board contains RIs 1 through 3. The RI, which has been enabled by the connect code from the PP, transfers these indications to the interconnected CPU or memory MAC unit.†

- Function to RI - Set when a function word is being issued by the PP.
- Ready to RI - Set when the PP is sending data or has received data.
- Active to RI - Set when the PP is to begin sending data or when the PP is ready to receive data.
- Inactive to RI - Set after the PP has sent the last control or data word in an exchange.

TRACKING OF INPUT/OUTPUT MODE

The Z80 Response Control circuits use the Input Mode and Output Mode signals to indicate whether a PP or the TPM is about to input information from the MAC (Input Mode active) or output information to the MAC (Output Mode active). When no I/O is occurring with the MAC, Input Mode is kept active and Output Mode inactive. This disables the receiving circuits of the MAC (MAC 3.3A) so no false parity errors occur.

MCH SIGNALS IN - FF RESET CONTROL

These circuits pass I/O status indications within the MAC when it is performing an operation with a connected PP or the TPM. Under these conditions, the signal Enable RI 0 is active. This allows indications similar to those previously described for RIs 1 through 3 to be distributed through the MAC.

These circuits also distribute signals that reset the MAC for a new operation after the present operation has been completed or when a power on or deadstart occurs.

CONTROL WORD REQUEST CONTROL

These circuits determine when a PP or the TPM is sending the second control word to the MAC at the start of an operation. The MAC ignores the first control word of an operation and latches and decodes only the second control word. Table 3A-1 lists the signal interchange sequences that start a MAC read/write operation. Similar sequences are used for an echo operation. A request summary status operation does not require control words and, therefore, has a much shorter starting sequence.

Upon receipt of the first control word of a MAC read/write operation, the First Ready Seen FF sets. The Control Word Register (MAC 3.3A) does not latch this word. When the second control word is received, the signal Load Control Load Register is generated to latch that word and the Control Word Full FF sets. The latched control word is decoded to establish a starting address in the MAC nanocode. When the next active indication is received from channel 17 or the TPM, the MCH Request Nanocode signal is generated to start the nanocode sequencing. The nanocode provides the control for accessing the specified register. When the I/O exchange is complete, the First Ready Seen and Control Word Full FFs clear.

---

†Currently, no I/O exchanges involving the TPM occur over RIs 1 through 3.

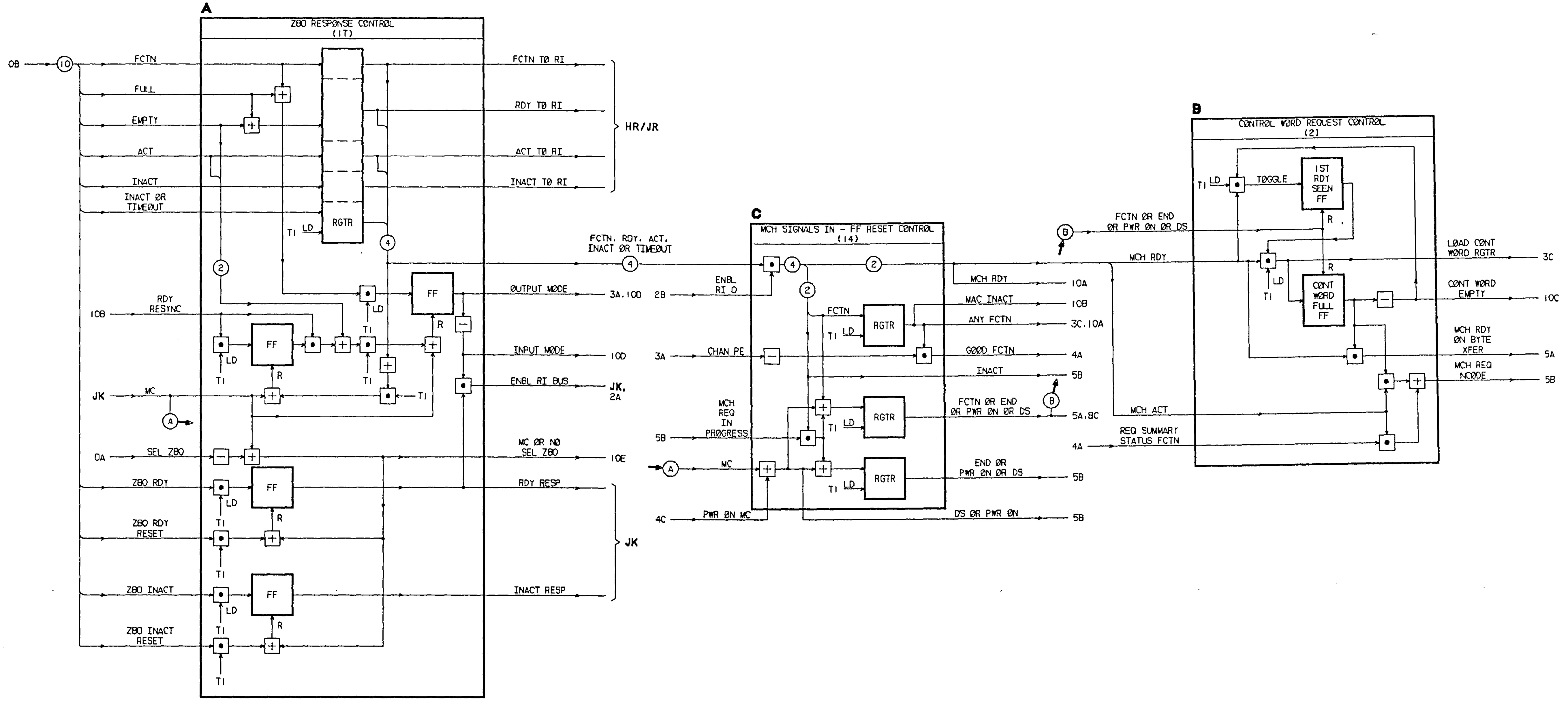
Table 3A-1. Start of a MAC Read/Write Operation (Sheet 1 of 2)

Sequence with a PP via MCH	Sequence with the TPM†
MCH: Channel 17 Function signal sent to MAC along with function word containing RI 0 connect code (bits 52-55), opcode (bits 56-59), and type code (bits 60-63).	TPM: Z80 Connect To RI signal sent to MAC. MAC: Select RI signal sent to TPM. TPM: RI 0 connect code sent to MAC via data bits 60-63
MAC: MAC Inactive signal sent to MCH.	TPM: Z80 Inactive and Z80 Next Full signals are a function sent to MAC.
MCH: Channel 17 Active signal sent to MAC.	TPM: Z80 Full signal sent to MAC along with function word containing opcode (bits 56-59) and type code (bits 60-63).
MCH: Channel 17 Full signal sent to MAC along with first control word (control word ignored by MAC).	MAC: Inactive Response signal sent to TPM (signal ignored by TPM).
MAC: MAC Empty signal sent to MCH.	TPM: Z80 Active signal sent to MAC.
MCH: Channel 17 Full signal sent to MAC along with second control word (bits 56-63).	MAC: Enable RI Bus signal sent to TPM.
MAC: MAC Empty signal sent to MCH.	TPM: Z80 Full signal sent to MAC along with first control word (control word ignored by MAC).
MCH: Channel 17 Inactive signal sent to MAC.	

Table 3A-1. Start of a MAC Read/Write Operation (Sheet 2 of 2)

Sequence with a PP via MCH	Sequence with the TPM†
MCH: Channel 17 Active signal sent to MAC. MAC prepares for read/write from/to register specified in second control word.	MAC: Ready Response signal sent to TPM (signal ignored by TPM). TPM: Z80 Full signal sent to MAC along with second control word (bits 56-63). MAC: Ready Response signal sent to TPM (signal ignored by TPM). TPM: Z80 Inactive signal sent to MAC. TPM: Z80 Active signal sent to MAC. MAC prepares for read/write from/to register specified in second control word.

†The TPM sets the signal Hold Function On Channel 17 before performing I/O exchanges with the MAC. The TPM keeps the signal set until it is done using the MAC.



CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JQ)
Z80 RESPONSE CONTROL
60463540
G
MAC 3.1

Z80 AND MCH INTERFACE

This circuit gates:

- RI Bits 56 through 63 and parity bit to channel 17. This occurs when a PP is connected to an RI to input data from a CPU or memory MAC unit and the unit has a full condition.
- MAC Data Bits 0 through 7 and parity bit to channel 17. This occurs when a PP is connected to the MAC (RI 0) to input data and the MAC has a full condition.
- MAC Data Bits 0 through 7 and parity bit to the TPM. This occurs when the TPM is connected to the MAC and a data path is established between them.

The Invert RI Parity signal from the JJ board allows parity errors to be deliberately generated for testing purposes.

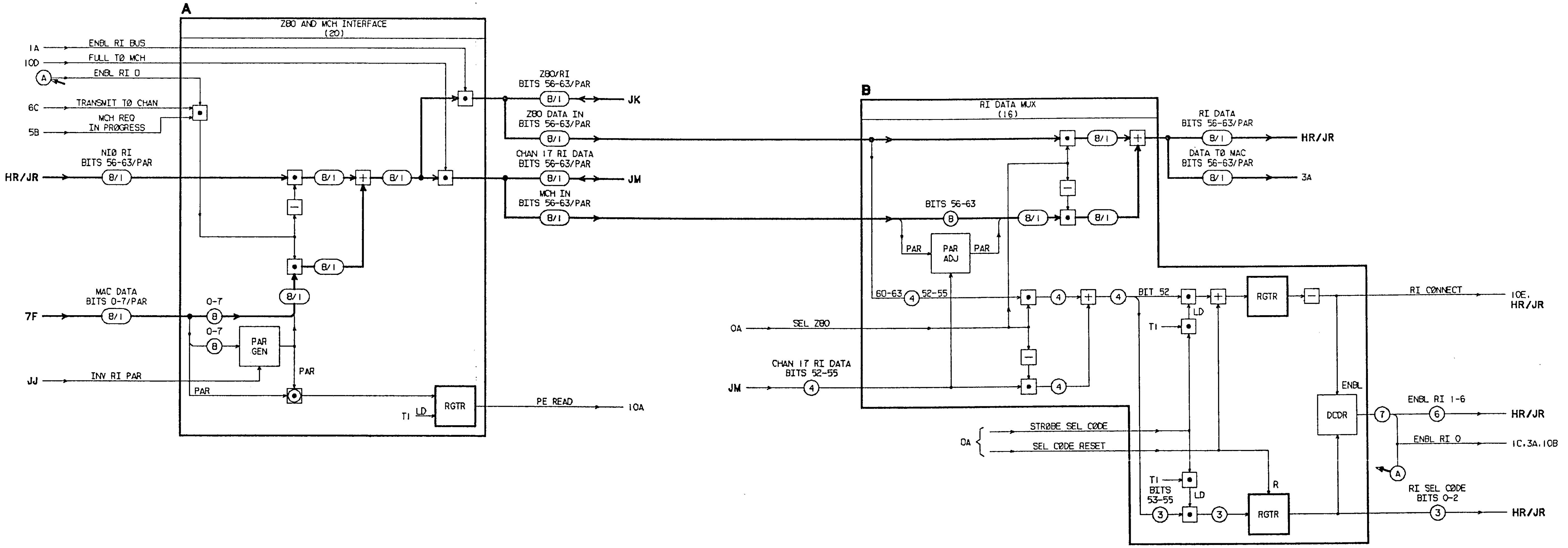
RI DATA MUX

The RI Data Mux circuits multiplex data from the TPM and channel 17 and decode RI connect codes. The data from the TPM and channel 17 is handled as follows.

- Z80 Data In Bits 56 through 63 and parity bit go to the MAC Channel Receiver (MAC 3.3A) when the TPM is connected to the MAC.
- MCH In Bits 56 through 63 and parity bit go to the MAC Channel Receiver and the JR board when the TPM is not connected to the MAC.

The RI Data Mux circuits also receive Channel 17 RI Data Bits 52 through 55. These bits carry a connect code when a PP is issuing a function word on channel 17. When this occurs, the Strobe Select Code signal causes these bits to be latched and decoded. If the connect code selects an RI other than RI 0, an enable for the selected RI is sent to the HR/JR board. If the connect code selects RI 0, the MAC prepares for an operation with channel 17. If the TPM is connected to the MAC when a function word is issued on channel 17, the connect code (and the rest of the function word) are ignored until the TPM disconnects.

The Strobe Select Code signal is also generated to latch and decode the connect code sent by the TPM. The TPM places a connect code on Z80 Data In Bits 60 through 63 before an operation between it and the MAC is to occur. The connect code from the TPM always selects RI 0.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JQ)
Z80 AND MCH INTERFACE.
RI DATA MUX

60463540 G
MAC 3.2

CHANNEL RECEIVER, TYPE CODE REGISTER, AND CONTROL WORD REGISTER

These circuits latch the type code and control word for a MAC operation and receive the data destined for maintenance registers during a MAC write. At the beginning of a MAC operation, the Type Code Register latches the type code sent by the TPM or a PP on bits 60 through 63. The type code is part of the function word. The bits carrying the opcode of the function word are passed to the Function Decoder (MAC 3.4A).

Later, the Control Word Register latches the second control word sent for the operation. The type code and control word remain latched until replacement occurs during the next operation. With an echo operation, the second control word is the word that is to be echoed back to the connected unit. With a request summary status operation or any of the MAC clear operations (clear LEDs, clear ADU/CMI, or clear fault status registers), no control words are involved, and therefore, control word latching does not apply.

Data to be written into maintenance registers is received in 8-bit bytes. After a parity check, the data is passed to the Data Mux (MAC 3.7C).

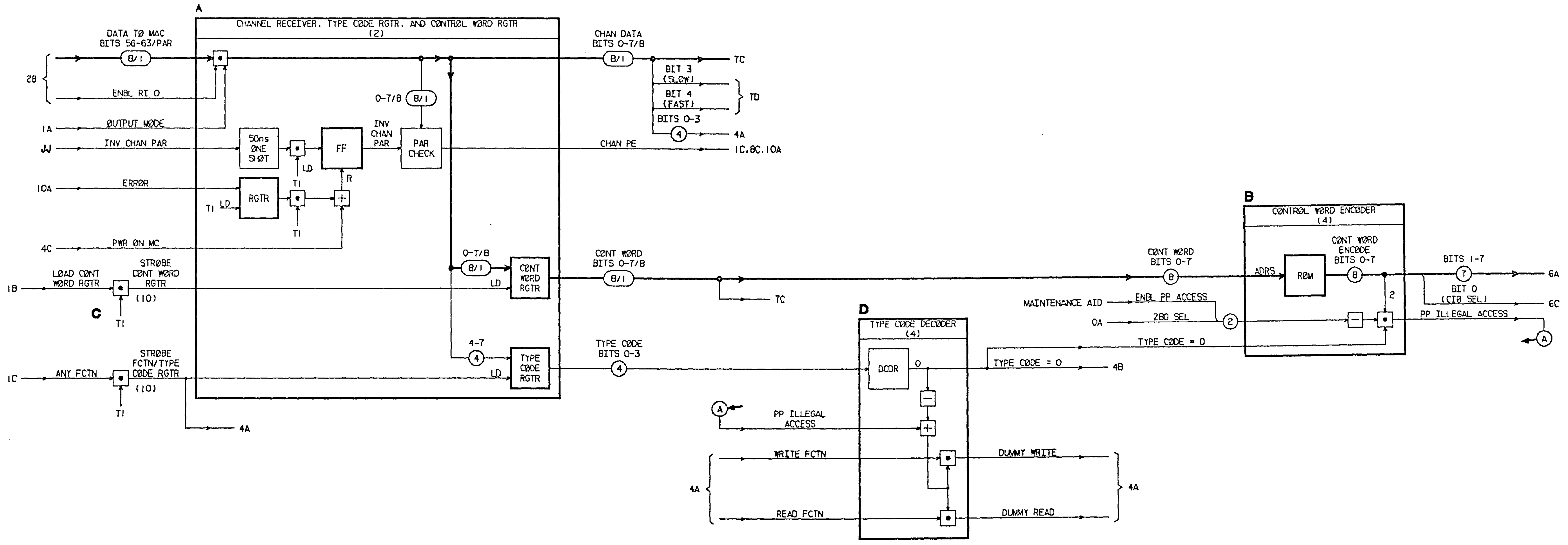
TYPE CODE DECODER

The Type Code Decoder checks that the type code for a MAC read/write operation is zero. If any other type code is received, only a dummy read/write operation is permitted. With a dummy read operation, the MAC returns zeros instead of reading from a register. With a dummy write operation, the MAC accepts data but does not write the data into a register.

CONTROL WORD ENCODER

This circuit produces nanocode address bits that are based on the second control word received during a MAC read/write operation. This second control word specifies the number of the maintenance register where the read/write is to occur.

The Control Word Encoder circuit also checks for an illegal PP access condition. An illegal PP access condition exists when a control word from a PP specifies a register that is not to be accessed by PPs (such as the NIO or CIO Channel Status Registers). This causes a dummy read/write to be performed. However, if the test signal Enable PP Access is set, the access by the PP is allowed. The TPM is allowed access to all maintenance registers.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JO)
CONTROL WORD AND
TYPE CODE RGTRS AND
DECODERS

CODE IDENT	DWG NO	REV
	60463540	A

SHEET	PAGE
MAC 3.3	

FUNCTION DECODER AND STARTING ADDRESS ENCODER

These circuits decode the opcode portion of a function word and generate a starting nanocode address for the MAC operations that require nanocode execution. Table 3A-2 defines the MAC operations, lists their opcodes, and indicates which require nanocode execution.

Table 3A-2. MAC Operations and Opcodes

Opcode (Hex)	Operation	Nanocode Required
3	Clear LEDs - MAC clears all LEDs in IOU that are error indicators.	No
4	Read - MAC reads from the maintenance register specified in second control word and transfers the data to the connected unit (a PP or the TPM).	Yes
5	Write - MAC writes the data received from the connected unit into the maintenance register specified in second control word.	Yes
6	Master Clear ADU/CMI - MAC master clears the ADUs, CMI, and the R barrels in BASs.	No
7	Clear Fault Status Registers - MAC clears the Fault Status 1 and Fault Status 2 Registers.	No
8	Echo - MAC sends a data pattern to the connected unit upon each empty indication. The data pattern is stored in the Control Word Register (MAC 3.3A) and is the second word that the connected unit sent at the beginning of the operation.	Yes
C	Request Summary Status Byte - MAC sends the contents of its IOU Status Summary Register (MAC 3.7D) to the connected unit.	Yes

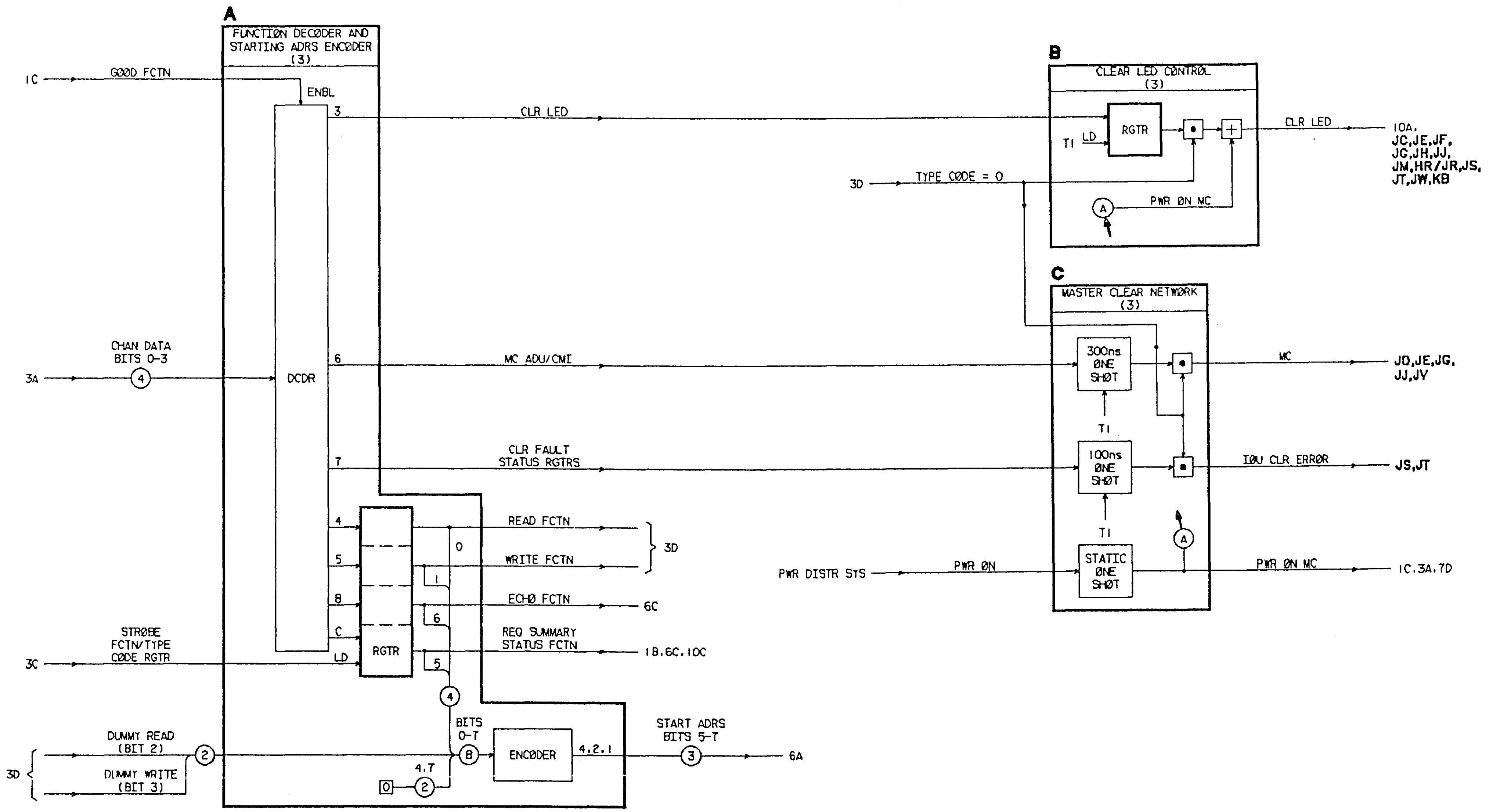
CLEAR LED CONTROL

This circuit generates the Clear LED signal upon a power on or when an opcode of 3 has been received along with a type code of 0. The Clear LED signal clears all error indication LEDs in the IOU.

MASTER CLEAR NETWORK

This network generates:

- The Power On Master Clear signal upon a power on. This signal prepares the MAC for operation and generates the Clear LED signal.
- The IOU Clear Error signal when an opcode of 7 has been received along with a type code of 0. This signal clears the Fault Status 1 and Fault Status 2 Registers.
- The Master Clear signal when an opcode of 6 has been received along with a type code of 0. This signal clears the ADUs, CMI, and the R barrels in the BASs.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JQ)
FUNCTIØN DECØDER

CODE IDENT
DWG NO 60463540
REV G
SHEET MAC 3.4
PAGE

NANOCODE REQUEST CONTROL

This circuit generates the signal Start Nanocode when a MAC operation requiring nanocode execution is to be performed. This is when either:

- The second control word for a read/write or echo operation has been received and an active is present.
- The opcode for a request summary status operation has been received and an active is present.

The signal Start Nanocode starts the timing chain in MAC Timing Control and causes the starting nanocode address to be presented to the Nanocode ROMs (MAC 3.6C). This starts the nanocode sequence for the pending data transfer.

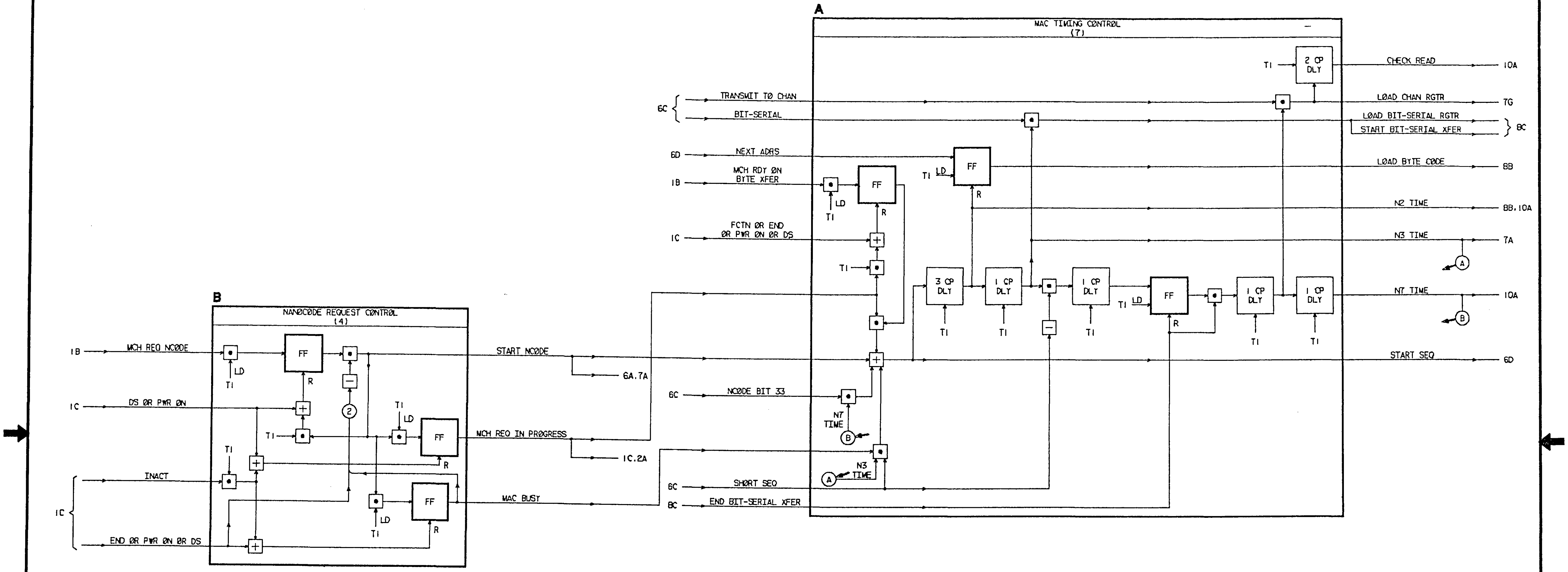
While data is being transferred, the signals MCH Request In Progress and MAC Busy are set. The signal MCH Request In Progress enables data to be transferred from the MAC to either the TPM or channel 17 and blocks the data path from the radial interfaces to channel 17 (MAC 3.2A).

MAC TIMING CONTROL

The MAC Timing Control circuits interact with the Bit-Serial Control circuits (MAC 3.8C) to provide the following described timing during a MAC read/write operation. The MAC Timing Control circuits also provide the timing for echo and request summary status operations. The timing for those operations basically consist of a short N0 through N3 sequence where the corresponding starting nanocode is addressed, followed by one N0 through N7 sequence where the nanocode at address DF_{16} (echo) or DE_{16} (request summary status) control the routing of the echo byte or status summary byte into the Channel I/O Register (MAC 3.7F).

Timing for read/write operations:

1. At the start of an operation, the signal Start Nanocode starts the timing chain in MAC Timing Control and causes the starting nanocode address to be presented to the Nanocode ROMs.
2. The nanocode at the starting address prepares the MAC for the subsequent data transfer and generates the signal Short Sequence. This and the signal N3 Time generated from the timing chain restarts the timing chain and generates the signal Start Sequence. At this point, Start Sequence causes a new nanocode address to be selected that is derived from the second control word.
3. The selection of a new nanocode address generates the signal Next Address. This signal sets the Load Byte Code FF. Load Byte Code loads new byte code bits into the Byte Code Incrementor (MAC 3.8B) that are generated by the newly selected nanocode.
4. At N2 Time, the Load Byte Code FF clears.
5. At N3 Time, the signals Load Bit-Serial Register and Start Bit-Serial Transfer are generated. Load Bit-Serial Register causes a parallel load of byte code bits (and data bits if a write) into the Serial/Parallel Shifter (MAC 3.8A). Start Bit-Serial Transfer enables the Bit Serial Control Counter (MAC 3.8C) to increment on each succeeding clock pulse. These conditions start the serial transfer.
6. When the serial transfer of a data byte is complete, the Bit Serial Control circuits generate End Bit-Serial Transfer. This signal enables N6 and N7 Times to occur.
7. At N6 Time, the signal Load Channel Register is generated to load the Channel I/O Register (MAC 3.7F) if the serial transfer was a read. The byte read is loaded into this register.
8. At N7 Time, the Error Detector circuits (MAC 3.10A) check for a parity error on the transfer and a MAC ready condition is established. If a read from an A, P, Q, or K register is occurring, Nanocode Bit 33 will be set to restart the timing chain (such a read requires the transfer of two sets of byte code bits).
9. An empty indication from the connected unit if a read or a full indication if a write generates the signal MCH Ready On Byte transfer. This sets a FF and the timing chain starts again for the next byte to be read/written.
10. At N2 Time, the Byte Code Incrementor adds a one to the byte code it loaded after the nanocode address change. This causes the next byte location within the selected register to be read/written next. However, if that byte location register is on a different board than the previous byte, a new nanocode address is selected at the start of the timing chain and the Byte Code Incrementor loads a new byte code instead.
11. Steps 5 through 9 repeat.
12. The cycle continues until all byte locations in the selected register are read/written or until the connected unit issues an inactive to end the operation.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	LEVEL 3 DIAGRAM (JO) NANOCODE REQUEST AND MAC TIMING CONTROL	CODE IDENT DWG NO 60463540 SHEET MAC 3.5	REV A PAGE

NANOCODE ADDRESS MUX REGISTER

These circuits provide the address that accesses the nanocode during read, write, echo, and request summary status operations. The first nanocode address used in these operations is the start address carried on input port 0 of the Address Select Mux. Table 3A-3 lists the values of start addresses for each type operation.

Table 3A-3. Nanocode Starting Addresses

Operation	Starting Address (Hex)
Read	30
Write	31
Echo	36
Request summary status	35

The second nanocode address used in read/write operations is carried on input port 1 of the multiplexer. This address is based on the second control word sent by the connected unit and on the value of Nanocode Bit 0. The second control word specifies which maintenance register that data is to be read from or written to. Nanocode Bit 0 is set if the operation is a write and clear if the operation is a read.

The third and subsequent addresses normally used read/write in operations are the nanocode generated addresses on input port 2 of the multiplexer. However, the control word based address on port 1 is also used in some cases as a return address.

The second (last) addresses for echo and request summary status operations are set DF_{16} and DE_{16} values respectively. These addresses are nanocode generated on input port 2.

The Nanocode Address Register latches the address gated by the multiplexer and presents the address to the Nanocode ROMs. This latching occurs as follows:

- Starting address - For read, write, or echo operations, when the second control word has been received and an active is present. For a request summary status operation, when the opcode has been received and an active is present.
- Second address - When the short sequence that follows the loading of the starting address is complete.
- Third and subsequent addresses (only applies to read/write operations) - When the byte count of the Byte Counter (MAC 3.7A) equals the end code and an empty indication has been received if a read or a full indication received if a write.

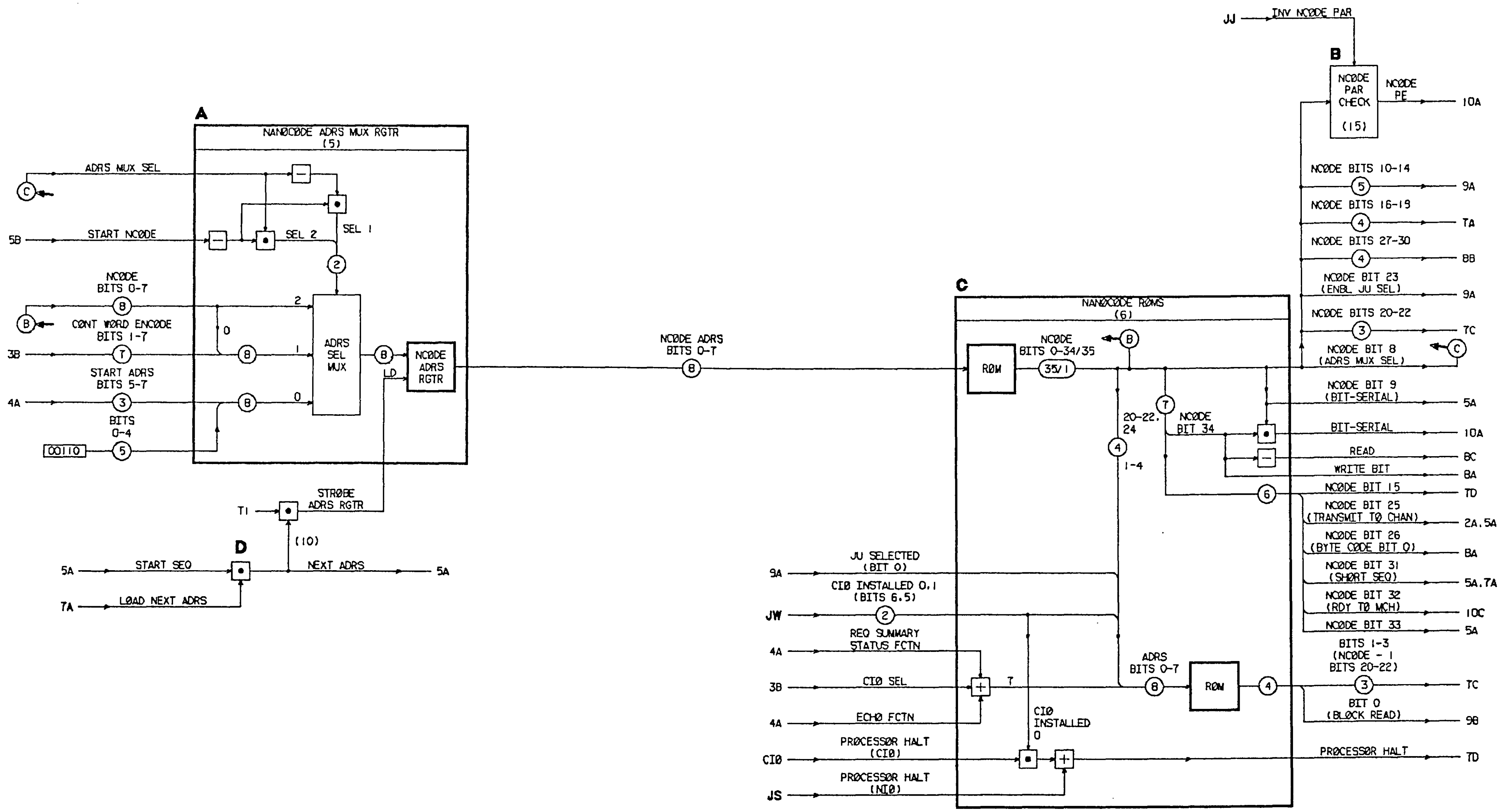
NANOCODE ROMS AND PARITY CHECK

The nanocode residing in the ROM controls the execution of read, write, echo, and request summary status operations. The nanocode consists of 36 bits (including a parity bit). Table 3A-4 defines the function of these bits.

If an attempt is made to read a nonexistent CIO register, the operation is blocked to avoid invalid parity errors from occurring. The signals CIO Installed 0 and 1 establish which CIO registers are present.

Table 3A-4. Nanocode Bits

Bit	Use or Function
0-7	Contain the next branch address; if bit 0 = 0, a read function is indicated, if bit 0 = 1, a write function is indicated.
8	Indicates which branch select option to use. If bit is high, nanocode branches to next address as indicated by bits 0 through 7. If bit is low, nanocode branches to address determined by Control Word Encoder (MAC 3.3B).
9	Enables bit serial transfer to take place.
10-14	Select appropriate board to be read from or written to.
15	When low, allows Fast/Slow Clock FFs (MAC 3.7D) to be set during a register D3 write.
16-18	Three-bit value determines when to end the byte transfer when bit 19 is low.
19	When low, byte counter is loaded with bits 16 through 18.
20-22	Select data gated by Data Mux (MAC 3.7C).
23	When this bit is high, the JU or JC board selection is determined by the Bit-Serial Pak Selector (MAC 3.9A) rather than from the nanocode bits.
24	When high, an OS bounds read is in progress and the MAC does a dummy read if the JU board A09 is not present.
25	When low, generates the signal Transmit to Channel.
26-30	Identify a particular register and byte on a board.
31	Indicates a short sequence for the MAC Timing Control logic (MAC 3.5A) during a read/write operation.
32	Indicates that a transfer of a byte of data has occurred from the maintenance channel and causes the MAC Ready signal (MAC 3.10C) to occur.
33	Allows continuation of nanocode progression between write and read operations, using only one function code. This occurs during a read A, P, Q, or K register operation, where the MAC must write two bytes of address and then read the register.
34	When low, indicates write serial data is available for the chosen serial line.
35	Even parity bit.



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LEVEL 3 DIAGRAM (JQ)
NANØCØDE CØNTRØL

CODE IDENT
DWG NO 60463540
REV A
SHEET MAC 3.6
PAGE

BYTE COUNTER

The Load Next Address signal generated by this circuit causes a new nanocode address to be loaded into the Nanocode Address Register (MAC 3.6A). The starting address for an operation is loaded when the Start Nanocode signal is generated. If the operation is an echo or a request summary status, the Byte Counter takes no further action. If the operation is a read or write, the following occurs:

1. The nanocode at the starting address loads the Byte Counter with a value of seven.
2. At N3 Time, the signal Short Sequence causes the address based on the second control word to be loaded into the Nanocode Address Register and the Byte Counter increments by one. This incrementing cycles the Byte Counter to zero in preparation of the read/write.
3. At each N3 Time that follows, the Byte Counter increments by one to count the number of bytes transferred.
4. When the byte count equals the end flag value on Nanocode Bits 16 through 18, it indicates that the next byte to be read/written is on a different board, and a new nanocode address is loaded into the Nanocode Address Register.
5. The nanocode generates a new end flag value and the Byte Counter continues counting at each N3 Time. If the byte count and end flag value become equal again, a new nanocode address is loaded.
6. This cycle continues until all data in the selected maintenance register is read/written or until the connected unit sends an inactive to end the read/write.

ELEMENT ID MUX

The Element ID Mux uses Byte Count Bits 1 and 2 to sequentially select the four bytes of element ID data for the IOU. Bits 48 through 63 of this data reflect a hardwired serial number; bits 40 through 47 indicate model type (code of 40_{16}), and bits 32 through 39 indicate the type of mainframe unit (code of 02 for IOU). This data is presented to the Data Mux for when a connected unit reads element ID.

IOU STATUS SUMMARY REGISTER

A request summary status operation reads bits 2 through 6 from the IOU Status Summary Register (this register may also be read as maintenance register 00). Bits 3 through 6 reflect error conditions in the IOU and power distribution system. Bit 2 is the Status Summary bit. This bit is set when an error exists within the mainframe. The error may be in the IOU or in the processor or memory area.

Bits 0 and 1 are the Fast and Slow Clock bits. These bits are distributed to the JA board where clock frequency is selected and to the Data Mux for maintenance register 40_{16} information. Nanocode Bit 15 must be set at N3 Time for a reselection of clock frequency to be made.

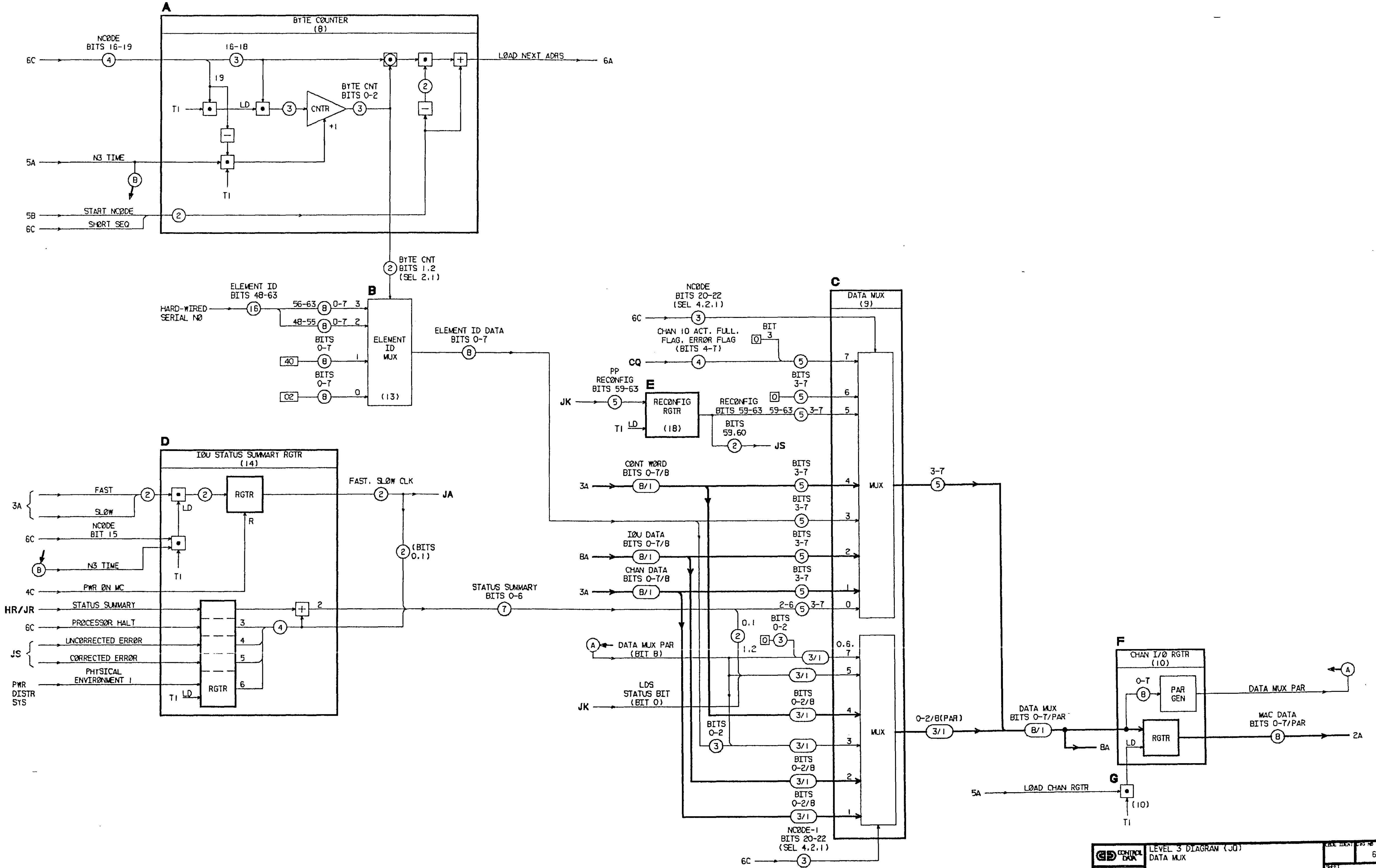
DATA MUX

The two-section Data Mux is the focal point of the MAC data path. The Data Mux is controlled by Nanocode Bits 20 through 22, which select the data that is gated. The selections include:

- Input 0 - Status summary data
- Input 1 - Channel 17 data or TPM data
- Input 2 - Maintenance register data
- Input 3 - Element identifier data
- Input 4 - Echo data latched in Control Word Register (MAC 3.3A)
- Input 5 - Maintenance register 40_{16} data (reconfiguration bits and Fast/Slow Clock bits)
- Input 6 - All zeros for when a dummy read is performed
- Input 7 - Channel 10 status

CHANNEL I/O REGISTER

This register latches the output of the Data Mux that is destined for channel 17 or the TPM.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JO)
DATA MUX

CODE IDENT	DWG NO	REV
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SHEET	PAGE
MAC 3.7	

BYTE CODE INCREMENTOR

The Byte Code Incrementor provides four of the five bits that make up the byte code. The byte code is loaded into Ranks 12 through 16 of the Serial Parallel Shifter and sent to the affected board before the exchange of each data byte during read/write operations. Byte Code Bits 0 and 1 indicate which maintenance register is to be accessed and Byte Code Bits 2 through 4 indicate which byte location within that register is to be read/write next.

The byte code is derived from Nanocode Bits 26 through 30. Nanocode Bit 26 (Byte Code 0) goes directly to Rank 16 of the Serial Shifter, while Nanocode Bits 27 through 30 (Byte Code Bits 1 through 4) are loaded into the Byte Code Incrementor when:

- The nanocode address based on the second control word has replaced the starting nanocode address. At this point, Nanocode Bits 26 through 30 reflect the first byte location to be read/written in the selected register. This information goes to the board containing that portion of the register. Portions of a maintenance register may be on several boards.

- A new nanocode address is going into effect. This occurs when the next byte location of the selected register is on a different board than the previous byte. At this point, Nanocode Bits 26 through 30 reflect the initial byte location to be read/written in that portion of the selected register. This information goes to the board containing that portion of the register.

Between loadings, the Byte Code Incrementor increments the previously loaded Nanocode Bits 27 through 30 by one at each N2 Time. N2 Time occurs one clock period before the start of the next serial transfer of a data byte. This incremented value causes the selected board to read from or write into the next succeeding byte location.

SERIAL/PARALLEL SHIFTER

The Serial/Parallel Shifter serializes the data bytes being passed to the selected board during a write and converts the serial data bytes from the selected board into parallel bits during a read. In addition, during either a read or write, the Serial/Parallel Shifter loads and serializes the byte code that goes to the selected board before each byte is read/written.

The loading of Byte Code Bits 0 through 4 into Ranks 12 through 16 and the loading of the set Load Byte Code Bit into Rank 11 occurs on the clock pulse following the activation of the signal Load Bit-Serial Register (N4 Time). Each clock pulse following this loading shifts one bit from the Serial/Parallel Shifter onto the Bit-Serial Data Out line in ascending order. Once the set Load Byte Code bit propagates from the Serial/Parallel Shifter, the signal Read Bit-Serial blocks any further propagation if the operation is a read.

If a write is occurring, the bits of the data byte to be written and its parity bit propagate from the Serial/Parallel Shifter immediately after the set Load Byte Code bit. In a write operation, a data byte and parity bit are loaded into the Serial/Parallel Shifter in parallel with the associated byte code. In addition, a set load data bit is loaded into Rank 1. This bit and the set Load Byte Code bit (loaded at Rank 11) verify the byte and byte code that the selected board is to load.

If a pause indication is received from the JC board, the loading and shifting of the Serial/Parallel Shifter is disabled and the read/write operation is halted. Such a pause is used to match the slot time of a PP with the reading of its A, P, Q, and K registers.

After shifting out a byte code for a read, the Serial/Parallel Shifter receives the requested data byte in serial form on the Bit-Serial Data In line. These serial bits enter at Rank 1 and propagate into Ranks 2 through 10 (Rank 2 contains parity bit). The contents of these ranks are then gated by the Data Mux (MAC 3.7C) and latched into the Channel I/O Register (MAC 3.7F). The timing for the assembly of the serial data byte and its latching is provided by the Bit Serial Control circuits and MAC Timing Control (MAC 3.5A).

BIT-SERIAL CONTROL

These circuits provide timing and control for the data transfers that occur between the MAC and an selected board during read/write operations. The overall timing for read/write operations is handled by the MAC Timing Control circuits (MAC 3.5A).

The control signals generated by the Bit-Serial Control circuits include:

- End Bit Serial Transfer - Indicates to MAC Timing Control that a byte of serial data has been transferred from/to the selected board. This enables N6 and N7 Times to occur in succession. At N6 Time, the Channel I/O Register latches the byte from the selected board if a read is occurring. At N7 Time, the MAC assumes a ready condition for either transferring the byte read to the connected unit or for receiving another byte to be written from the connected unit.

- Load - Causes the selected board to latch the serial bits being sent by the MAC. The bits being sent may be a byte code or a data byte to be written into the selected register.

- Read - Instructs the selected board to read the register data in the byte location specified by the byte code and send the data to the MAC.

- Read Bit-Serial - Blocks propagation from the Serial/Parallel Shifter after the byte code for a data byte to be read has propagated from the shifter.

The timing cycle of the Bit-Serial Control circuits for the read/write of a data byte is as follows:

1. The signal Start Bit-Serial Transfer from MAC Timing Control going active at N3 Time enables the Bit-Serial Control Counter to increment by one on each succeeding clock. The first increment changes the count from F_{16} to 0. The counter contains a loaded F value at the end of each serial transfer of a data byte.

2. When the count reaches 3, the Load signal is enabled on the next clock. On the next clock, Byte Code Bit 4 for the read/write will be propagating from the Serial/Parallel Shifter.

3. If a read is to be performed, the Read signal is enabled a clock period after the count of 4. Upon the setting of the Read signal, the set Load Byte Code bit will be propagating from the shifter.

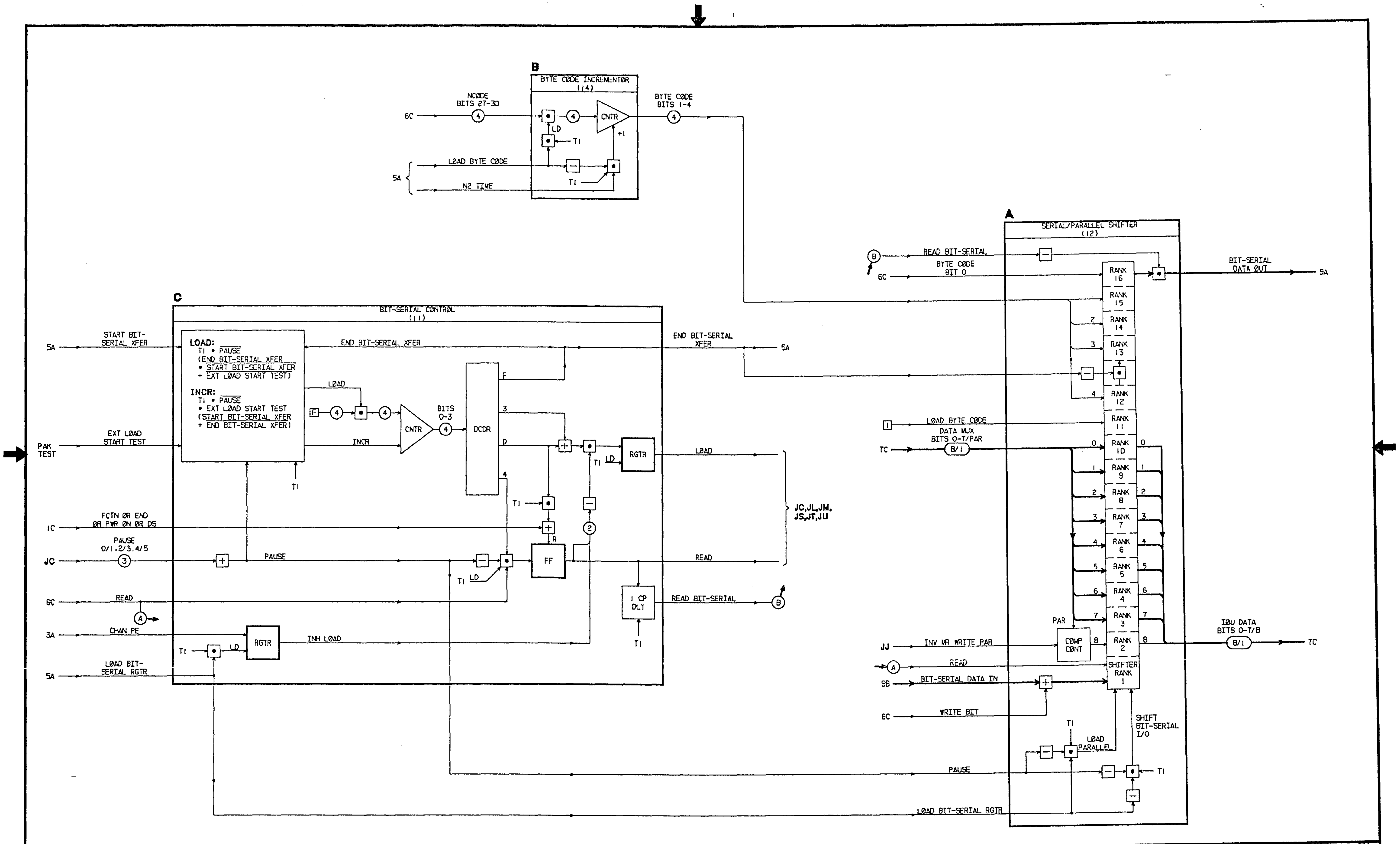
4. If a read is to be performed, the Read Bit-Serial signal is generated one clock period after the Read signal has gone active.

5. If a write is to be performed, the Load signal is enabled again at a clock period after the count of D_{16}. At the time of this Load signal, the set load data bit for the byte to be written will be propagating from the shifter.

6. When the count reaches F, the signal End Bit-Serial Transfer is generated to end the cycle.

If a pause indication is received from a JC board, the counter halts until the pause indication clears.

If a parity error is encountered on a data byte to be written, its load is inhibited.



LEVEL 3 DIAGRAM (JQ)
BIT-SERIAL CONTROL
AND SHIFTER

DEVELOPMENT DIVISION

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MAC 3.8

BIT-SERIAL PAK SELECTOR

The Bit-Serial Pak Selector circuits route the serial output bits from the Serial/Parallel Shifter onto the serial interface line specified by Nanocode Bits 10 through 14. Nanocode Bits 10 through 14 carry a value that selects the appropriate serial interface line for the register byte that is to be read or written. Only one serial interface line may be selected at a given time. Table 3A-5 lists the selection values for the available serial interface lines.

Table 3A-5. Serial Interface Line Selection

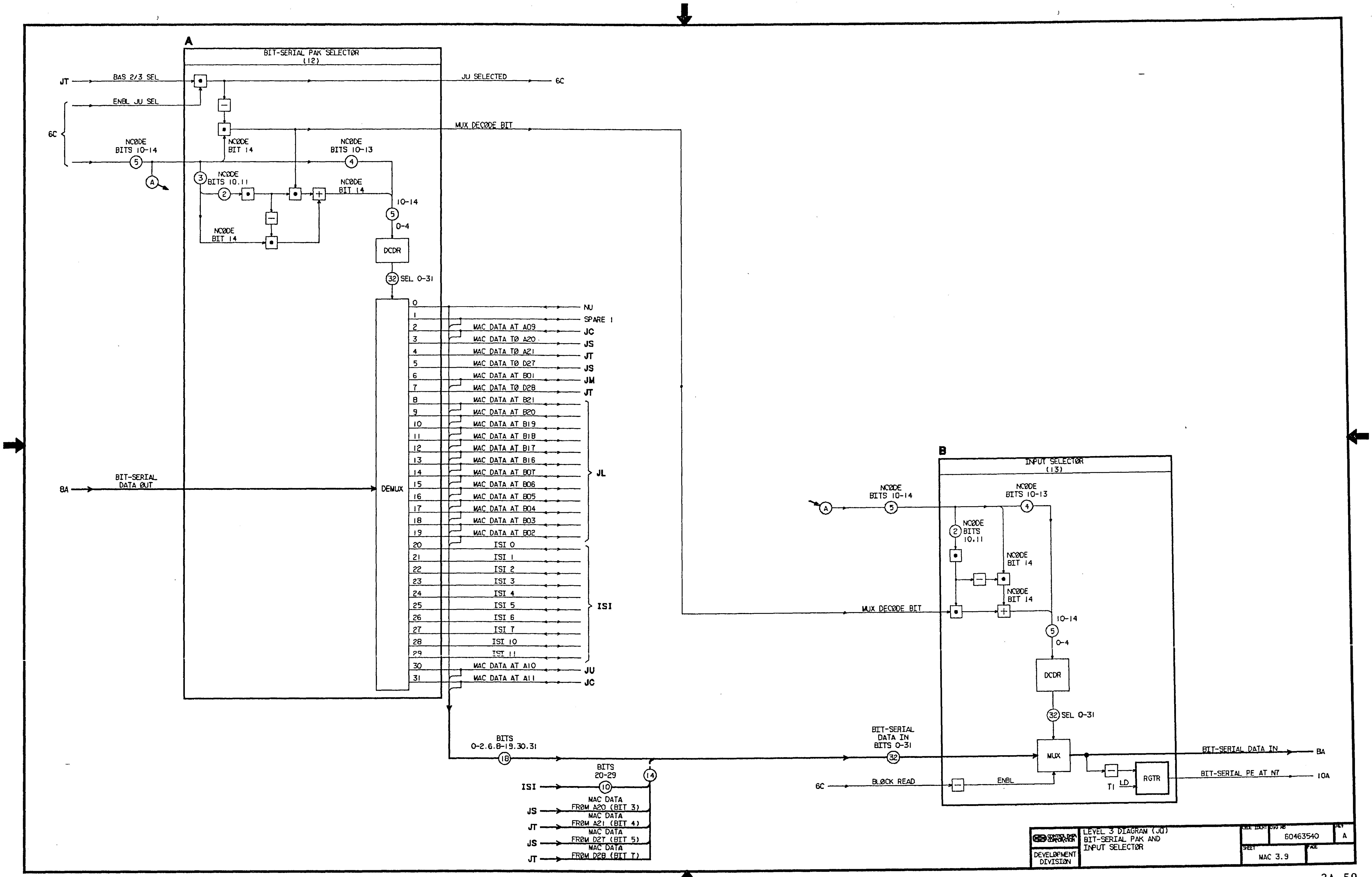
Nanocode Bits 10-14 (Hex)	Serial Interface Line
0	Not used
1	Not used
2	JU at A09
3	JS at A20
4	JT at A21
5	JS at D27
6	JM at B01
7	JT at D28
8	JL at B21
9	JL at B20
A	JL at B19
B	JL at B18
C	JL at B17
D	JL at B16
E	JL at B07
F	JL at B06
10	JL at B05
11	JL at B04
12	JL at B03
13	JL at B02
14	ISI 0
15	ISI 1
16	ISI 2
17	ISI 3
18	ISI 4
19	ISI 5
1A	ISI 6
1B	ISI 7
1C	ISI 10
1D	ISI 11
1E	JU at A10
1F	JC at A11

The serial output routed by the Bit-Serial Pak Selector circuits include byte code bits and if a write operation is occurring, the data bytes to be written into the selected register. A byte code consisting of five coded bits and a set load flag bit are sent over the selected serial interface line before the transfer of each data byte. The byte code indicates which register and byte location is to be read/written next. If a write operation is being done the byte to be written immediately follows the associated byte code. For each byte code or byte sent, the Bit-Serial Control circuits (MAC 3.8C) issue a Load signal that causes the board on the selected line to latch the line′s contents.

INPUT SELECTOR

The Input Selector circuits perform the same function for serial input as the Bit-Serial Pak Selection circuits perform for serial output. The board on the selected serial line sends the register data from the specified byte location when the Bit-Serial Control circuits issue a Read signal. The Input Selector circuits pass the data received to the Serial/Parallel Shifter for assembly into parallel bytes.

If an attempt is made to read from a nonexistent CIO register, the nanocode generates the Block Read signal to avoid invalid parity errors from occurring.



CONTROL DATA CORPORATION

DEVELOPMENT
DIVISION

LEVEL 3 DIAGRAM (JQ)
BIT-SERIAL PAK AND
INPUT SELECTOR

CODE IDENT | DWG NO 60463540 | REV A

SHEET MAC 3.9 | PAGE

ERROR DETECTOR

These circuits monitor MAC operations for errors. The type errors checked for include:

- Parity error on serial data read from a maintenance register (N7 Time, Bit Serial PE at N7, and Bit Serial signals active).
- Parity error on a function word received from a PP or from the TPM (Any Function and Channel PE signals inactive). This does not include a channel 17 parity error, which is reported separately.
- Parity error on a data byte received from a PP or the TPM (MCH Ready delayed and Channel PE active and Channel 17 PE signals inactive). This also does not include a channel 17 parity error.
- Parity error on the nanocode in effect (Nanocode PE and N2 Time signals active).
- Parity error on a data byte that the MAC is to send to a PP or the TPM (PE Read and Check Read signals active).
- RI/MCH Error that includes all the preceding mentioned errors when the MAC is operating with a PP plus an Error In from the HR/JR board. The HR/JR board generates the Error In signal when a parity error occurs on data going to a PP via RI 1, 2, or 3.

CHANNEL COMMUNICATIONS CONTROLS

This circuit controls the MAC Ready signal. The MAC Ready signal is generated prior to each I/O transfer between the MAC and a PP or the TPM. The signal indicates that the MAC is ready for the transfer. The conditions that generate MAC Ready may be either of the following:

- At the start of a read, write, or echo operation, when the connected unit is about to send the first or second control word.
- At N7 Time of a read, write, echo, or request summary status operation, when Nanocode Bit 32 (Ready to MCH) is set.

INVERT AND RESYNCHRONIZE CONTROL

These circuits gate the proper set of ready, inactive, and error indications for the I/O taking place. When a unit is connected to the MAC, these indications originate from the MAC. When a unit is connected to RI 1, 2, or 3, these indications originate from the HR/JR board.

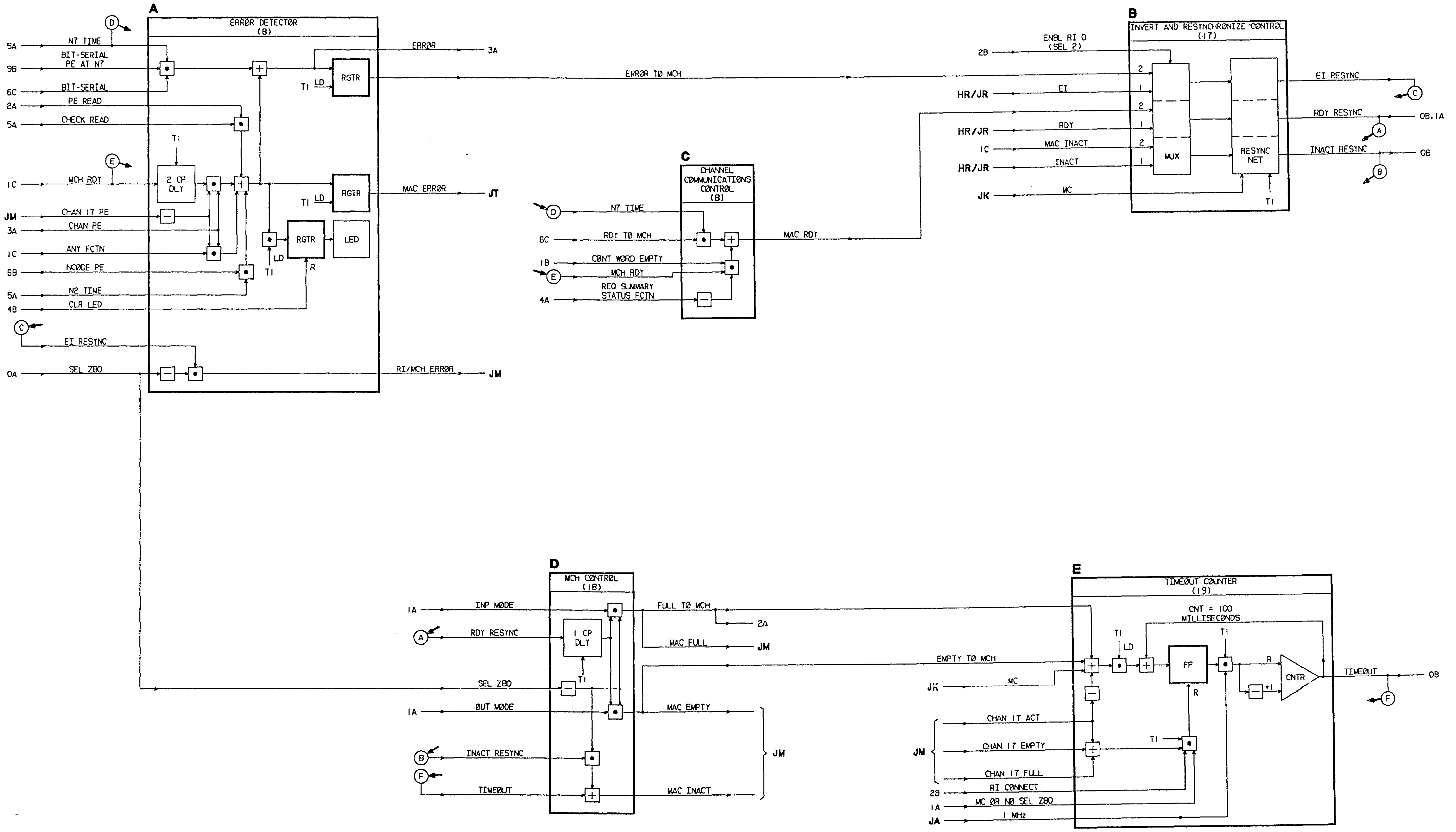
MCH CONTROL

The MCH Control circuits control the MAC interface signals sent to channel 17 during operations with a PP. These interface signals are:

- MAC Full - Generated when the MAC has a byte of data for the connected PP.
- MAC Empty - Generated when the MAC is ready to receive a data byte or control word from the connected PP.
- MAC Inactive - Generated following the receipt of a function word or when a timeout occurs.

TIMEOUT COUNTER

The Timeout Counter terminates an I/O transfer on channel 17 if the MAC or selected mainframe element on a radial interface fails to respond to I/O activity. The counter has a 100 millisecond counting cycle that starts when an active, empty, or full indication is received over channel 17. The counter then increments until a full or empty response is returned over channel 17. If no response occurs, the counting cycle completes and the Timeout signal is generated. This terminates the transfer and frees the PP that had been connected.



CONTROL DATA

DEVELOPMENT
DIVISION

LEVEL 3 DIAGRAM (JQ)
ERROR DETECTOR. MCH CONTROL.
TIMEOUT COUNTER

CODE IDENT DWG NO 60463540

REV G

SHEET MAC 3.10

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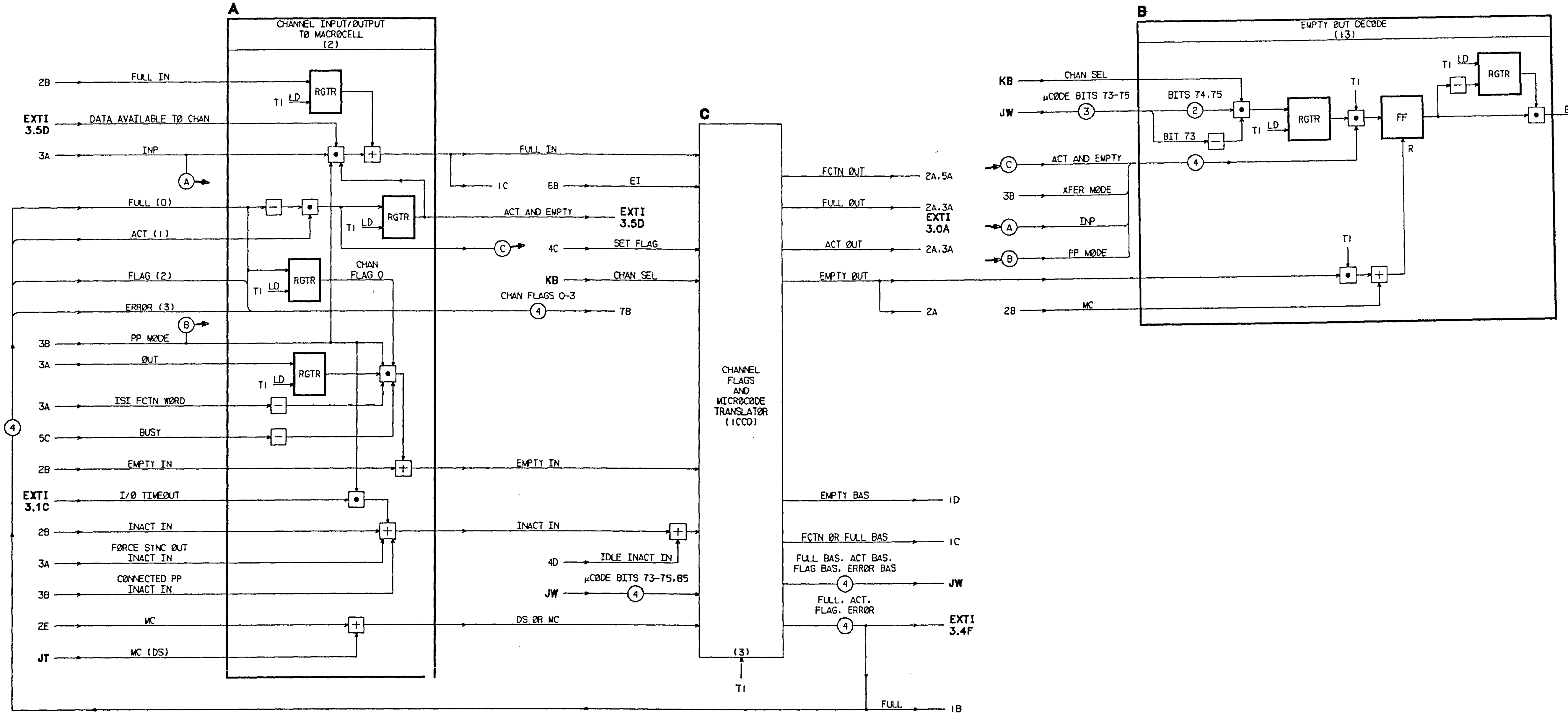

CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JX)
CHANNEL CONTROL

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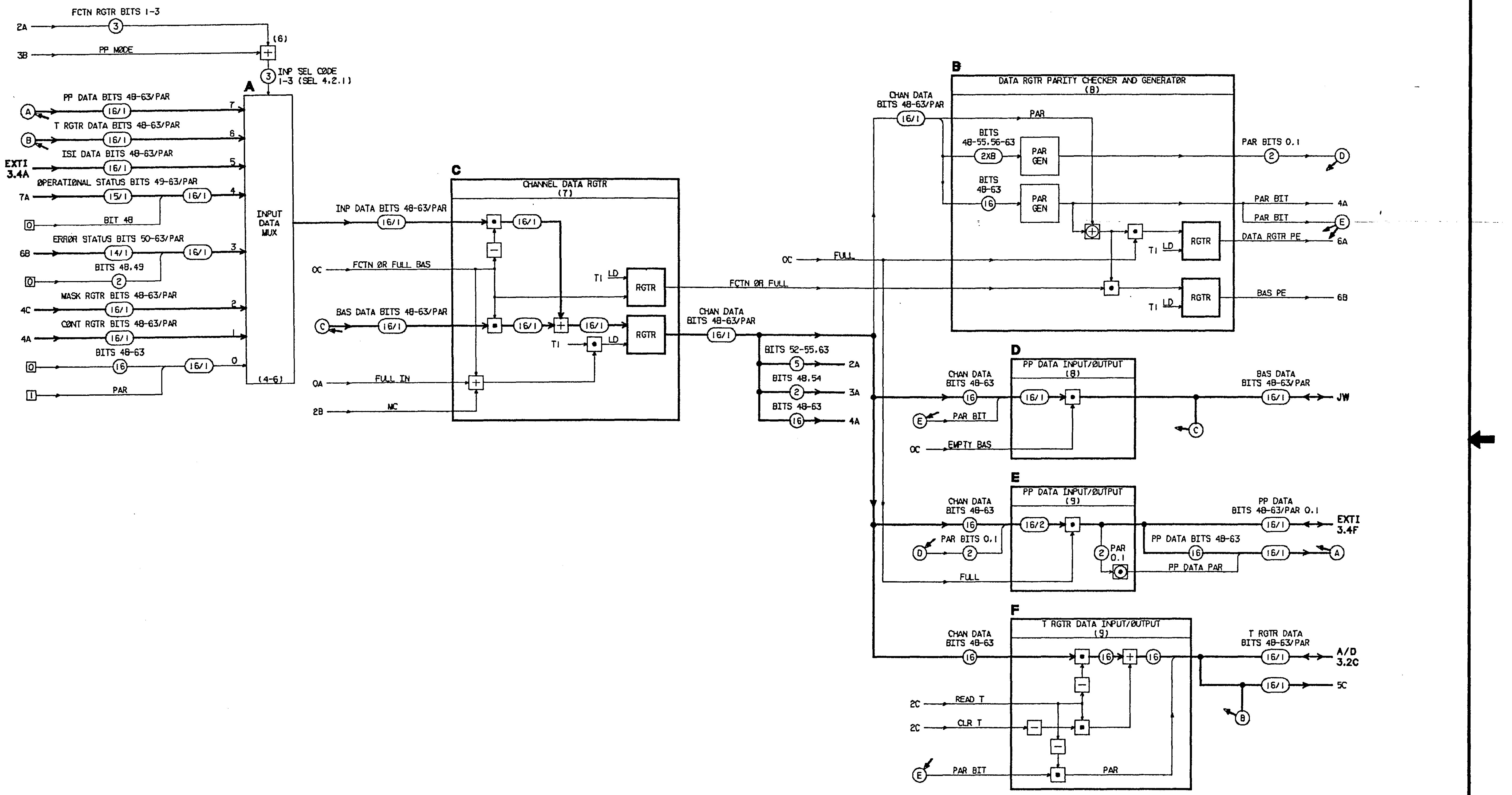

LEVEL 3 DIAGRAM (JX)
CHANNEL DATA INPUT/OUTPUT

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

DWG NO	60463540
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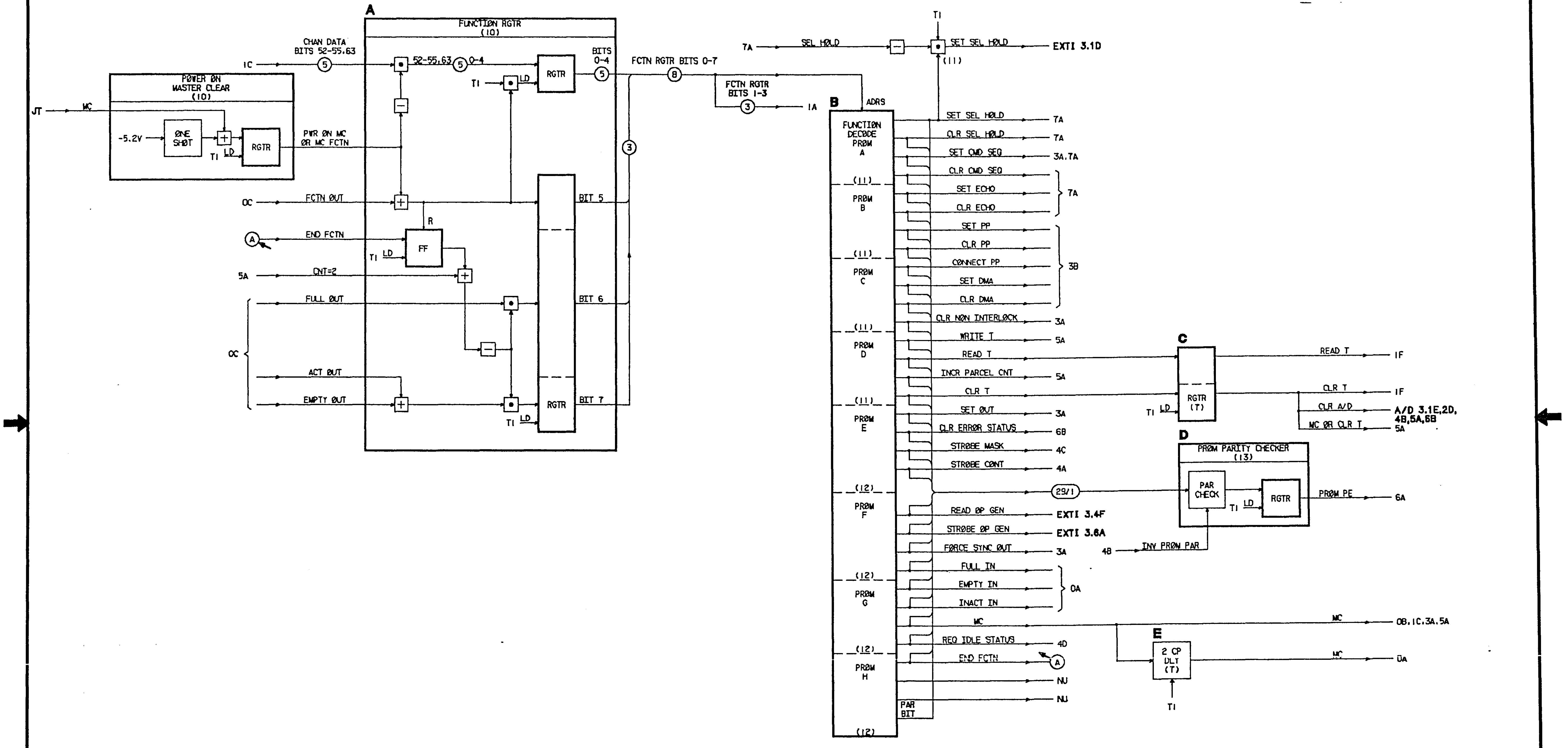

CONTROL DATA CORPORATION | LEVEL 3 DIAGRAM (JX)
FUNCTIØN RGTR AND DECØDE PRØMS

DEVELØPMENT DIVISIØN

DWG NO 60463540 | REV A

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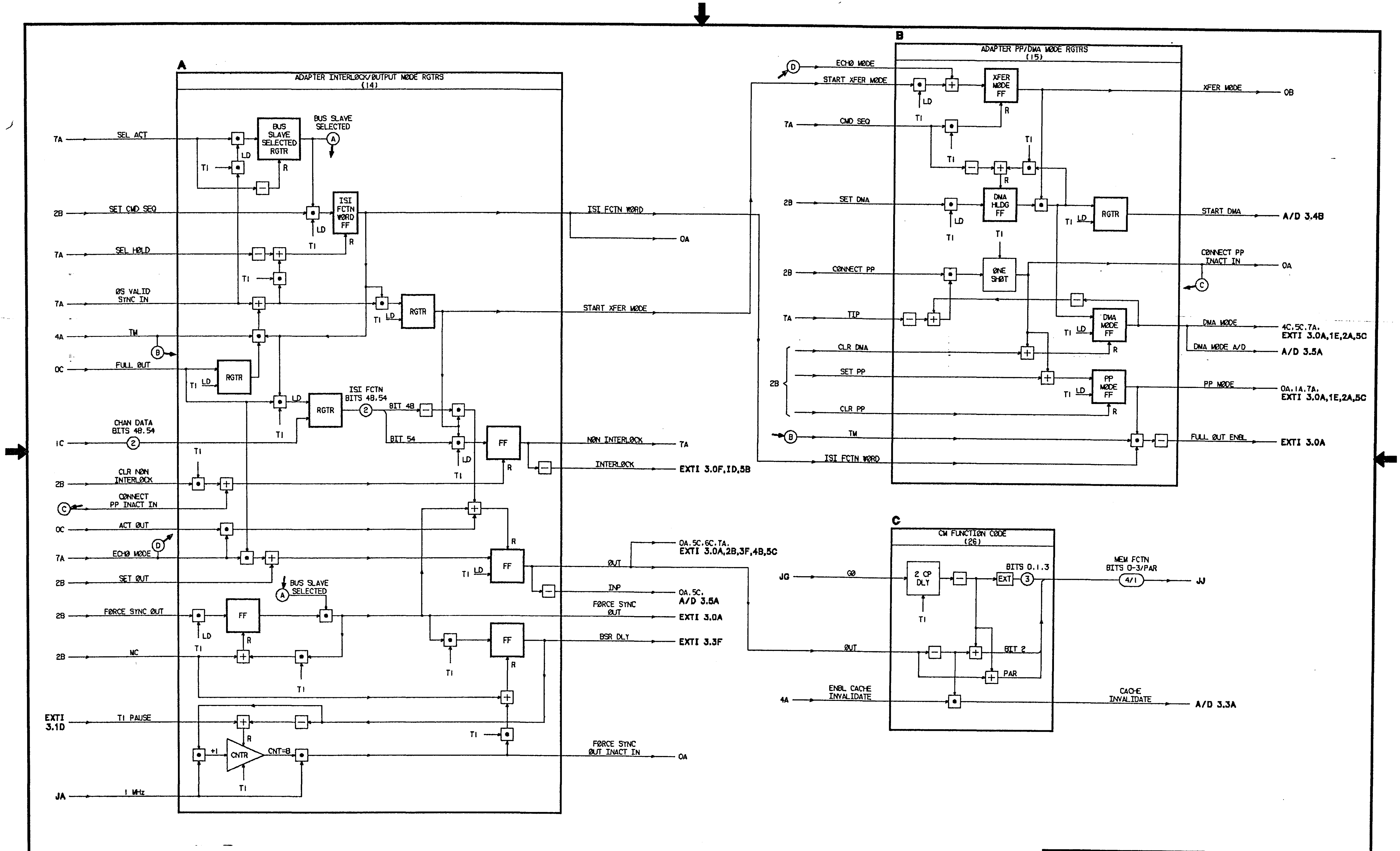

CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JX)
ADAPTER MODE RGTRS.
CM FUNCTION CODE

CODE IDENT

DWG NO
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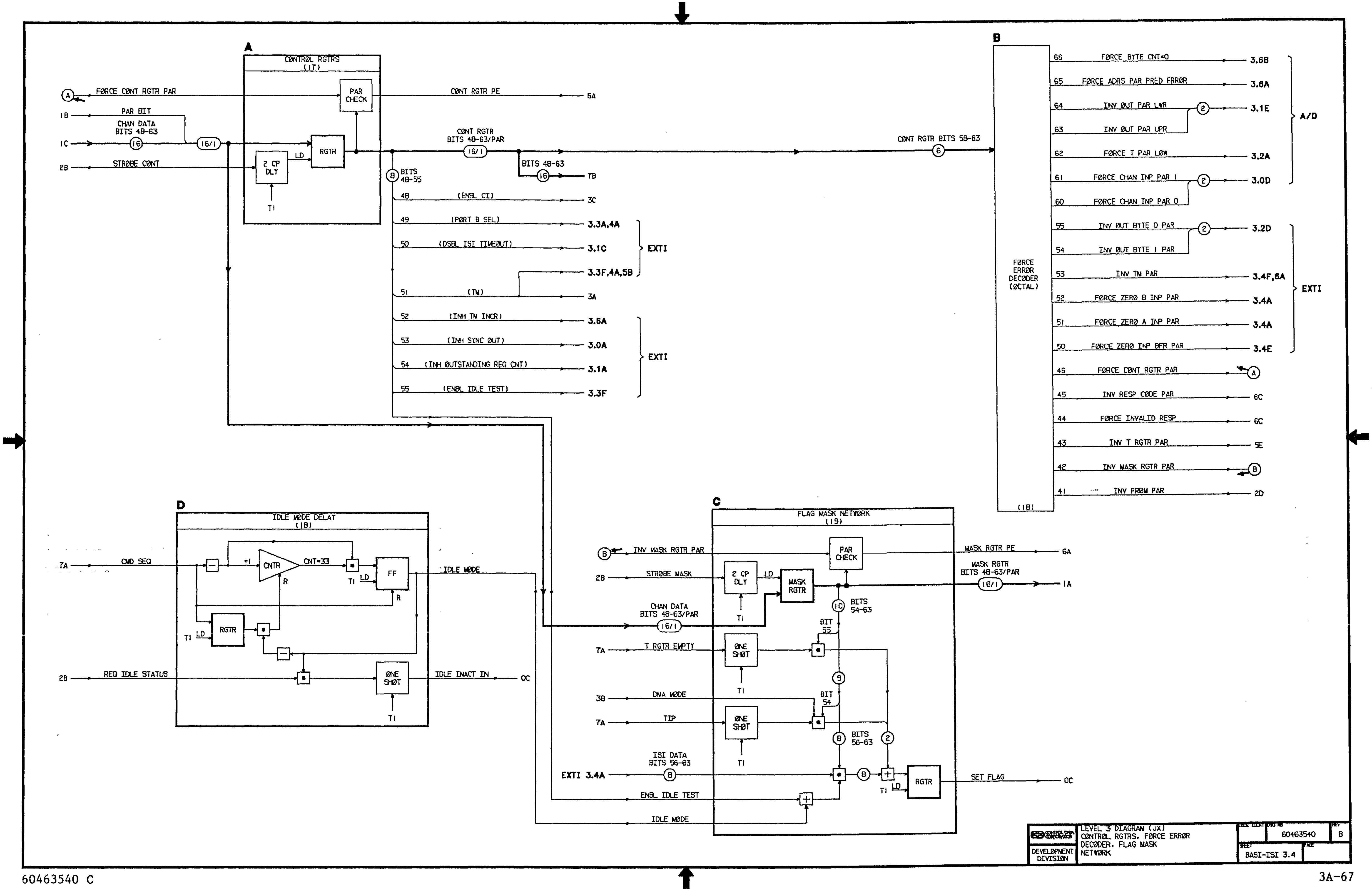
REV
A

SHEET
BASI-ISI 3.3

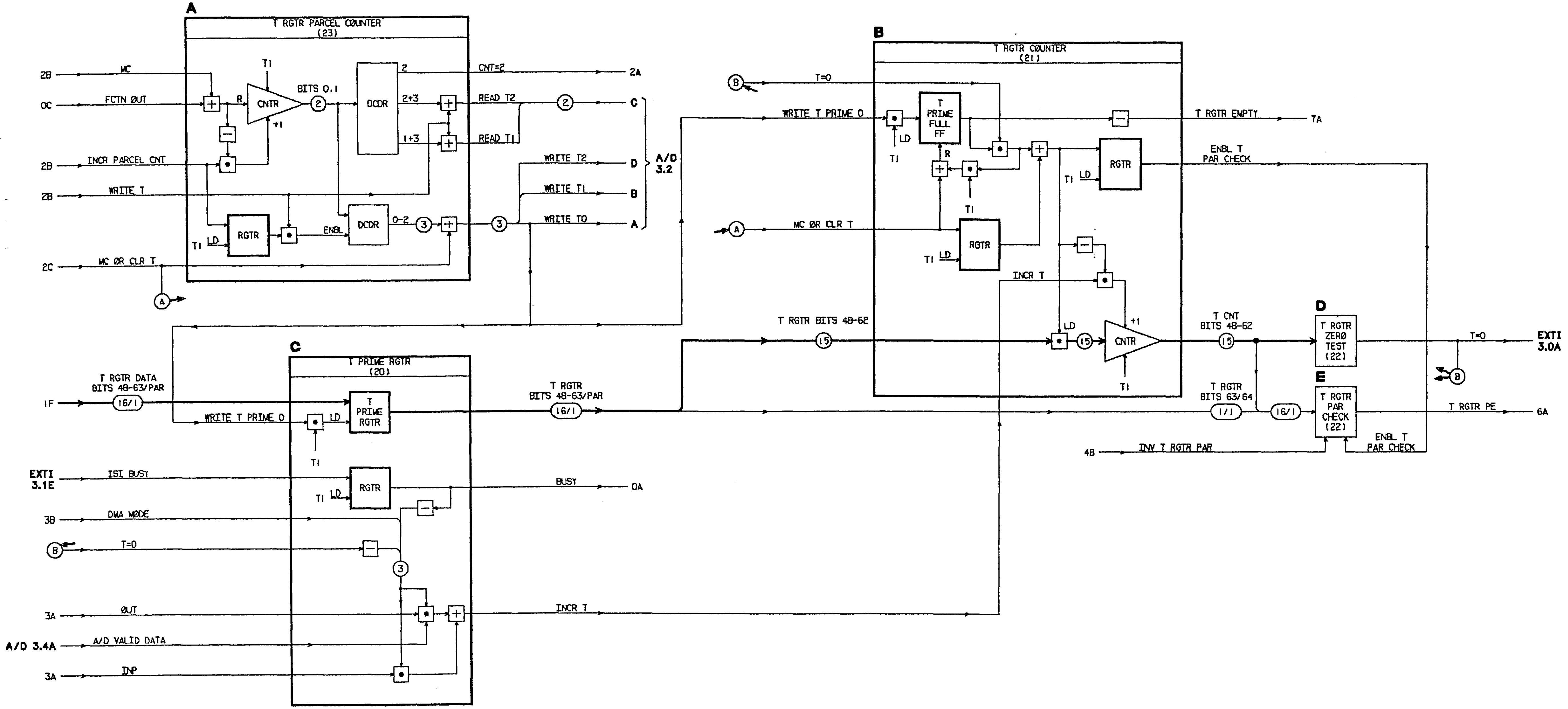
PAGE



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JX)
CONTROL RGTRS. FORCE ERROR
DECODER. FLAG MASK
NETWORK

CODE IDENT | DWG NO 60463540 | REV B
SHEET BASI-ISI 3.4 | PAGE



CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JX)
T RGTR NETWORK

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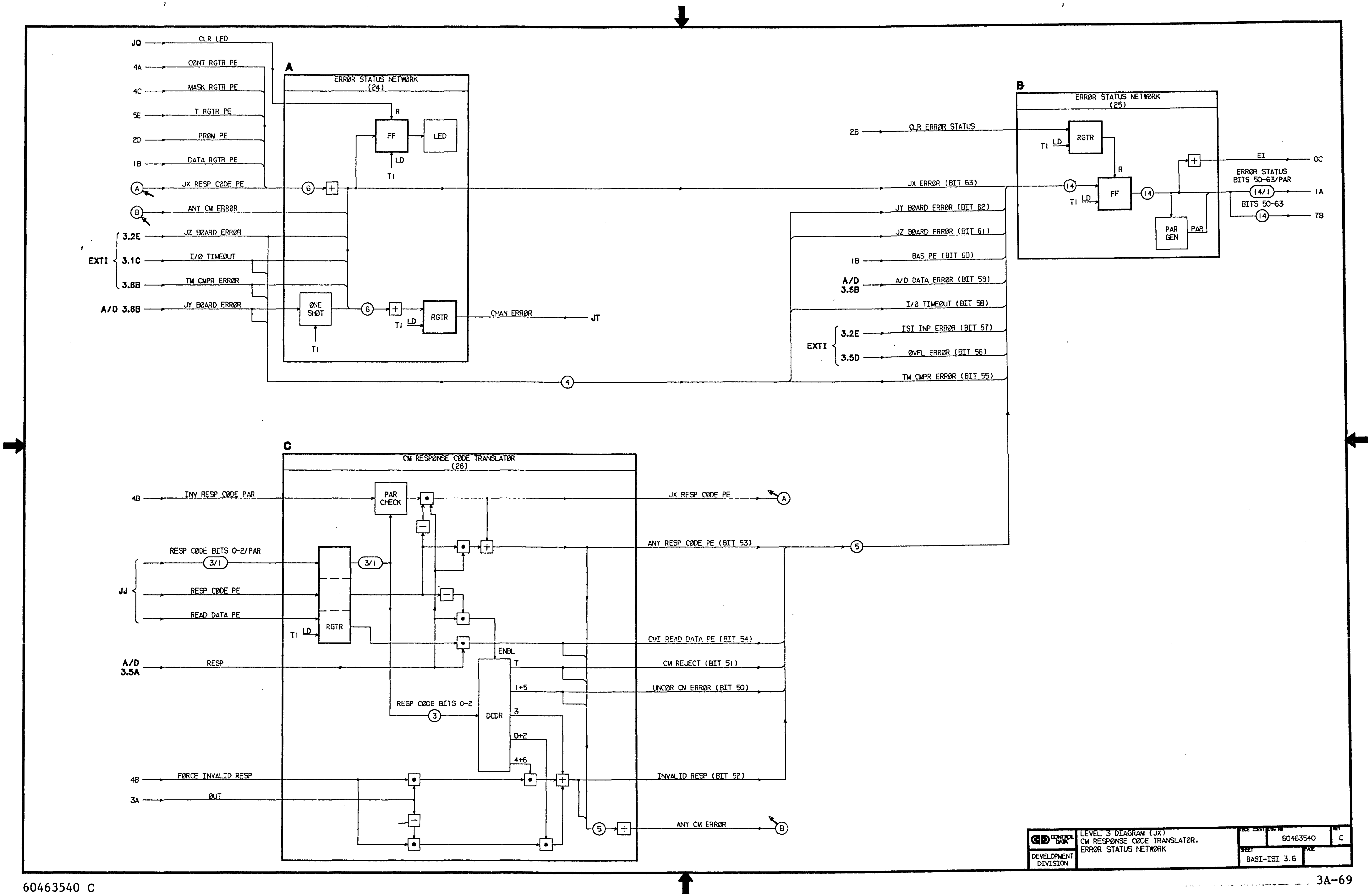
DWG NO 60463540

REV A

SHEET BASI-ISI 3.5

PAGE



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JX)
CM RESPONSE CODE TRANSLATOR.
ERROR STATUS NETWORK

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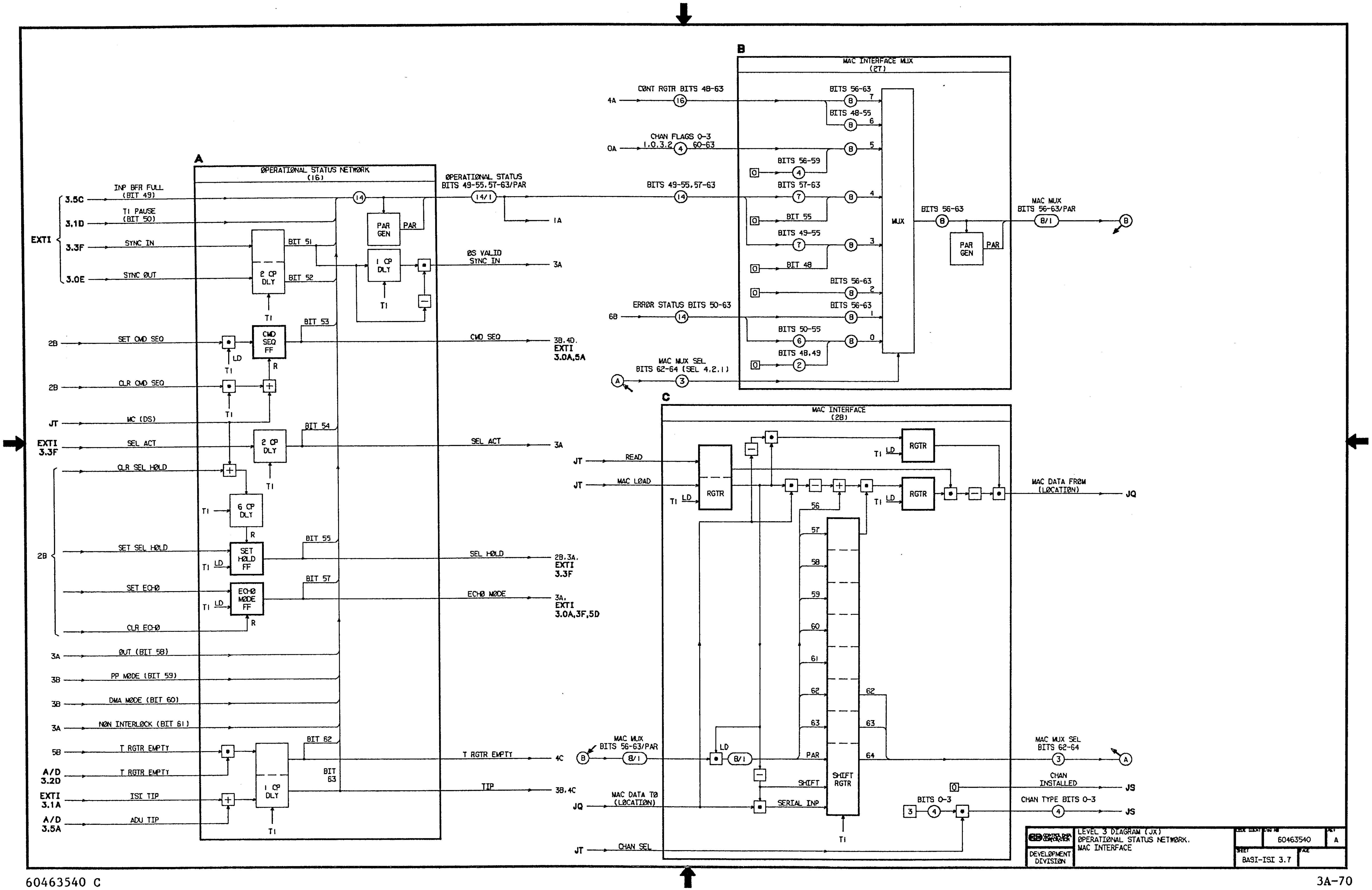
BASI-ISI 3.6



CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JX)
OPERATIONAL STATUS NETWORK.
MAC INTERFACE

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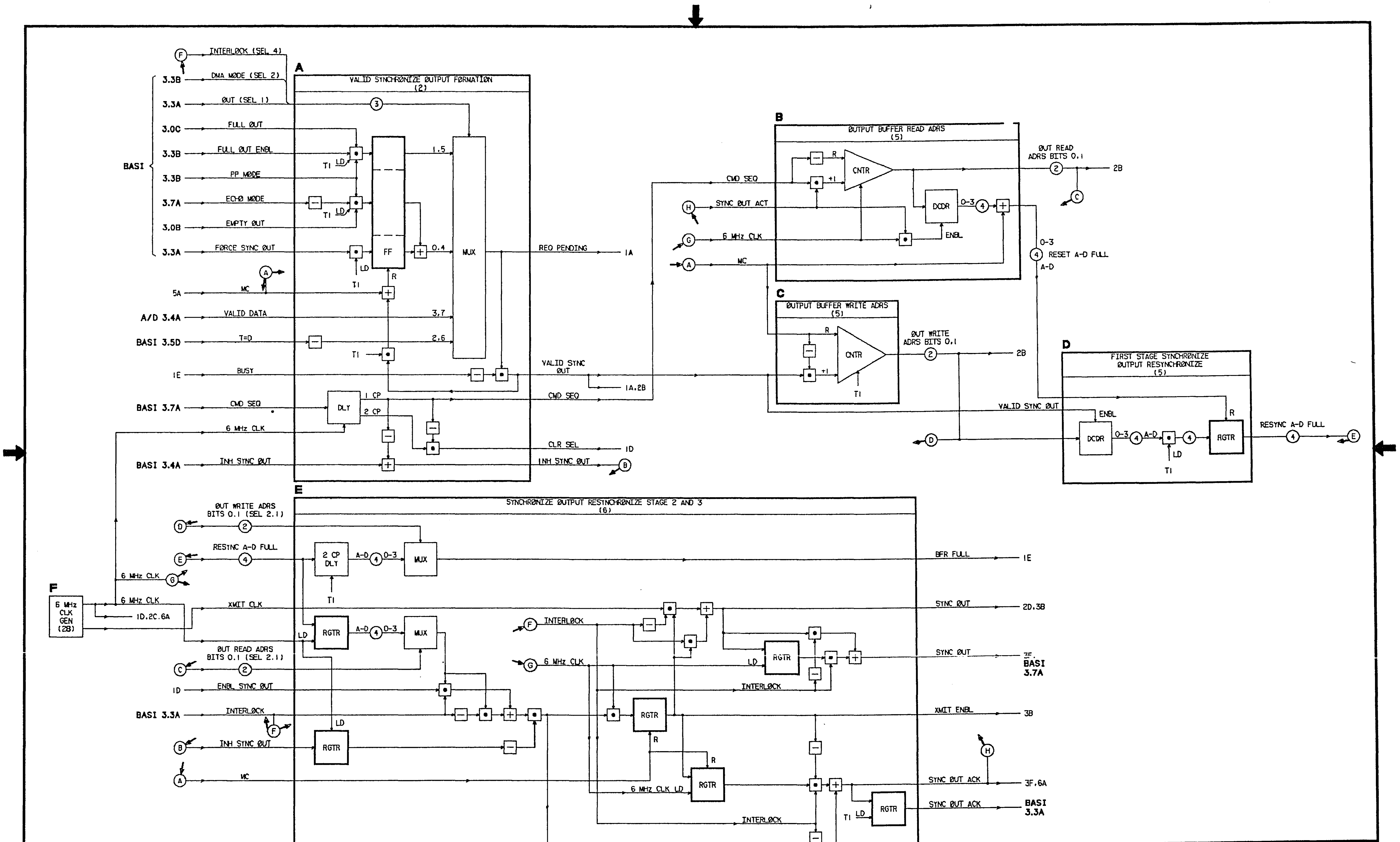
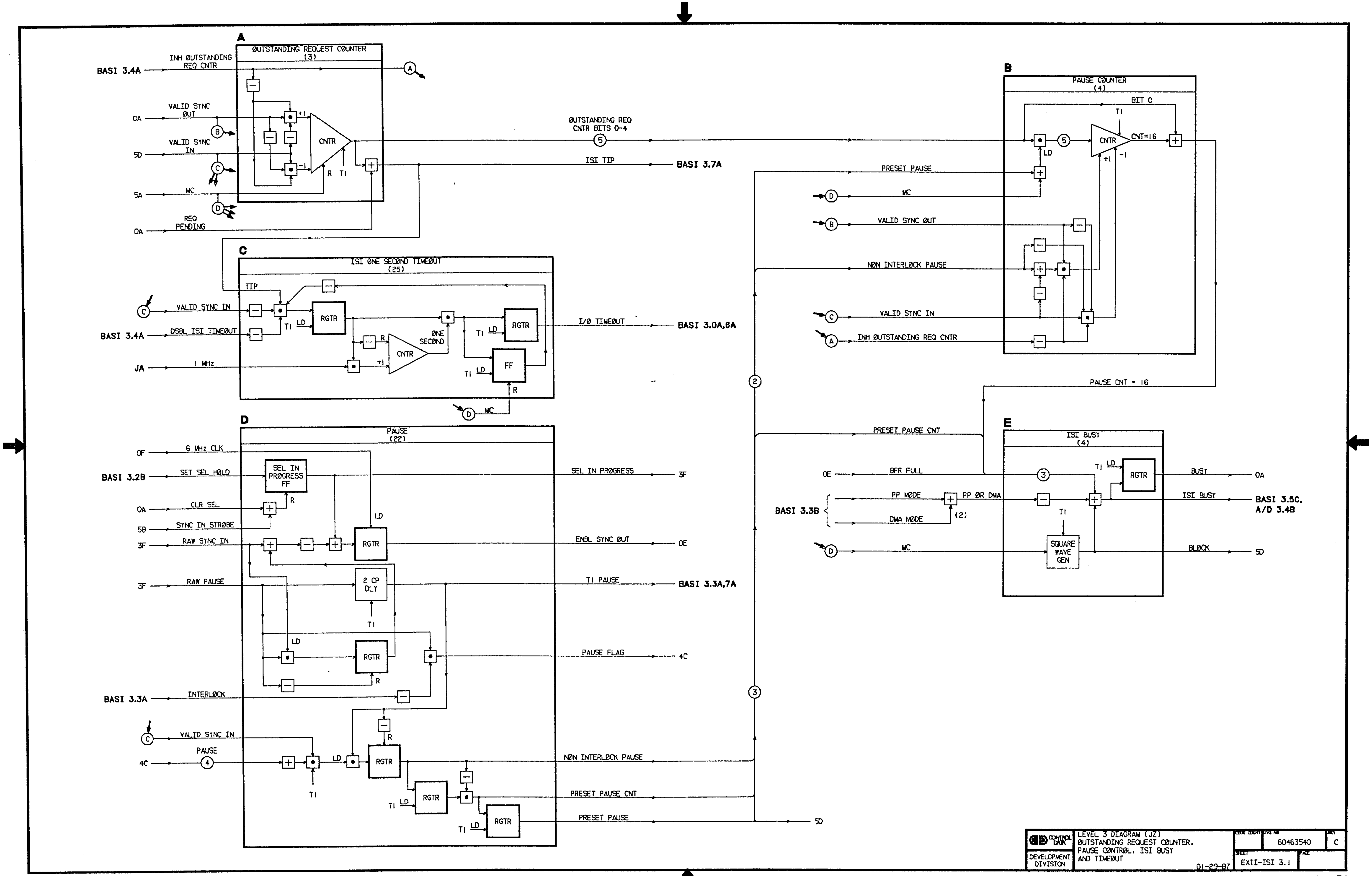
SHEET	PAGE
BASI-ISI 3.7	



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JZ)
OUTPUT BUFFER ADRS
COUNTERS. RESYNCRONIZER

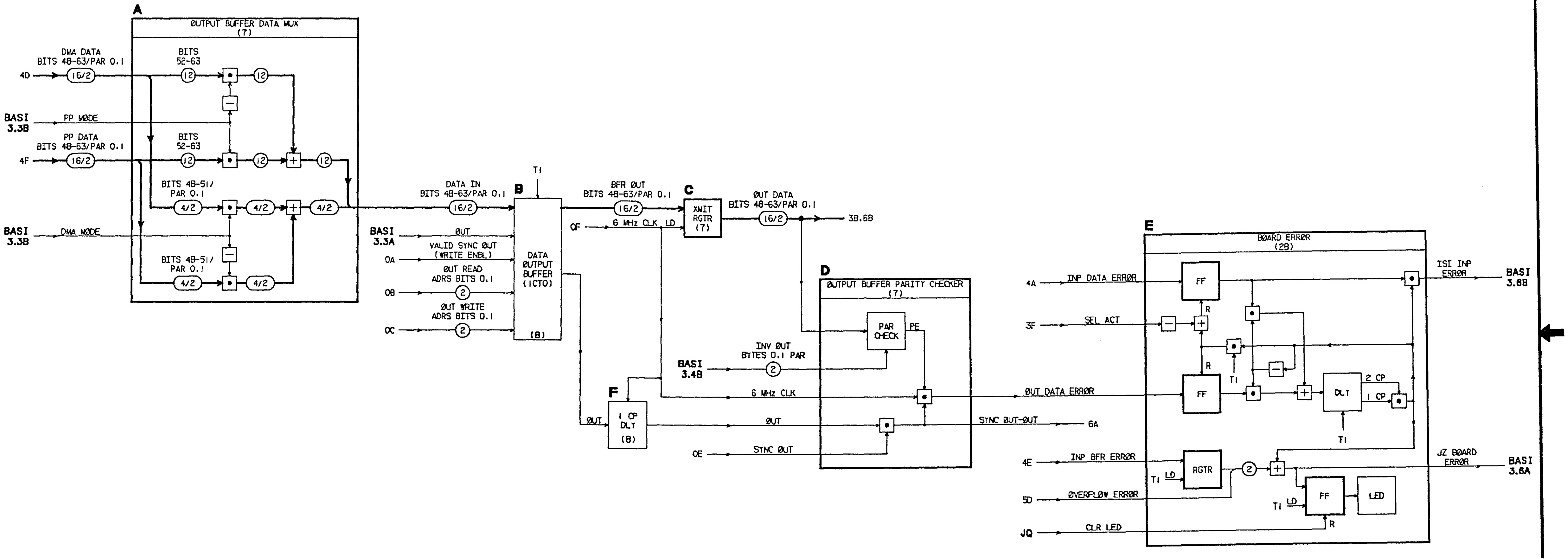
CODE IDENT
DWG NO 60463540
REV A
SHEET EXTI-ISI 3.0
PAGE



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JZ)
OUTSTANDING REQUEST COUNTER,
PAUSE CONTROL, ISI BUSY
AND TIMEOUT
01-29-87

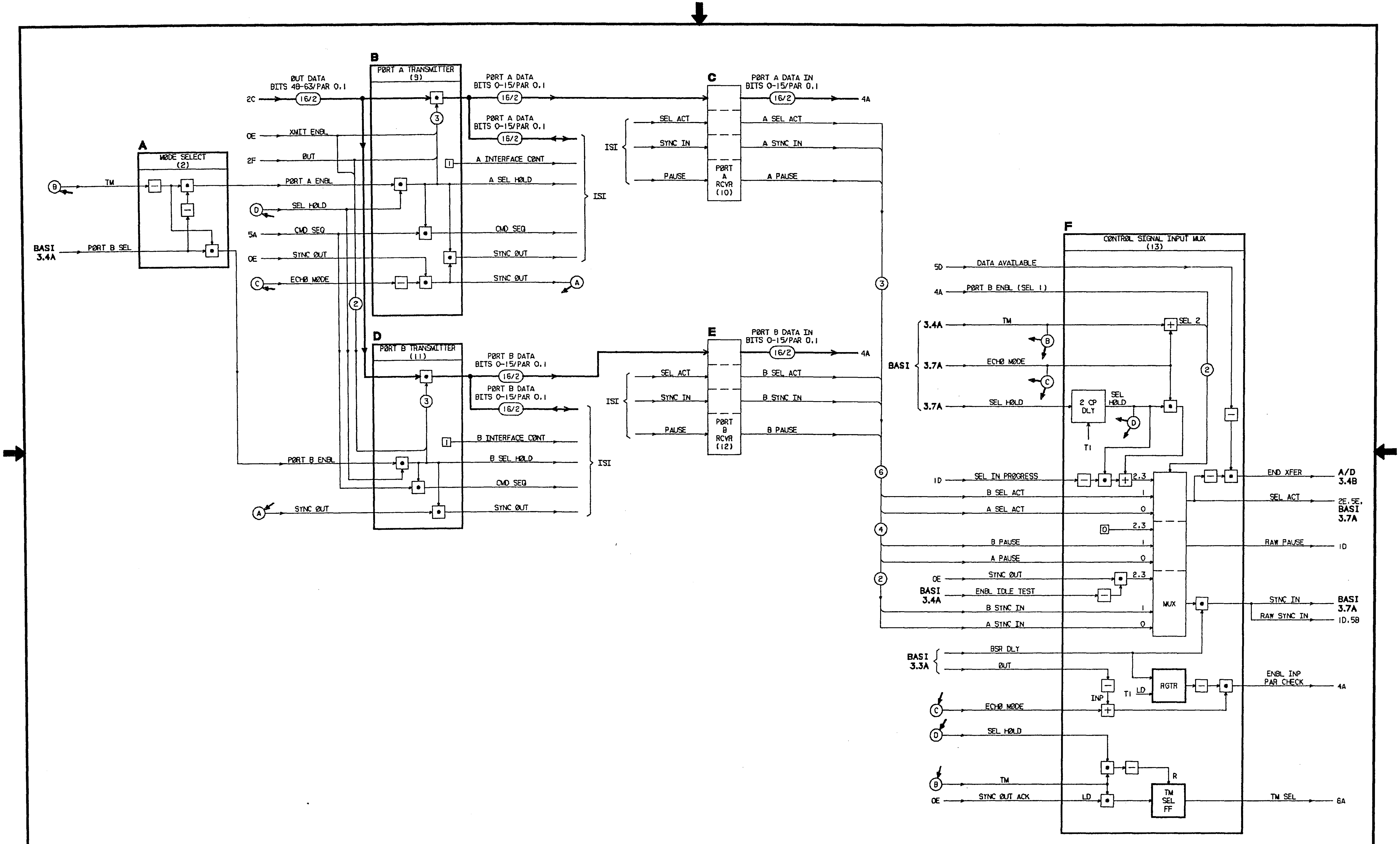
CODE IDENT
DWG NO 60463540
REV C
SHEET EXTI-ISI 3.1
PAGE



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JZ)
OUTPUT BUFFER, BOARD
ERROR DETECTOR

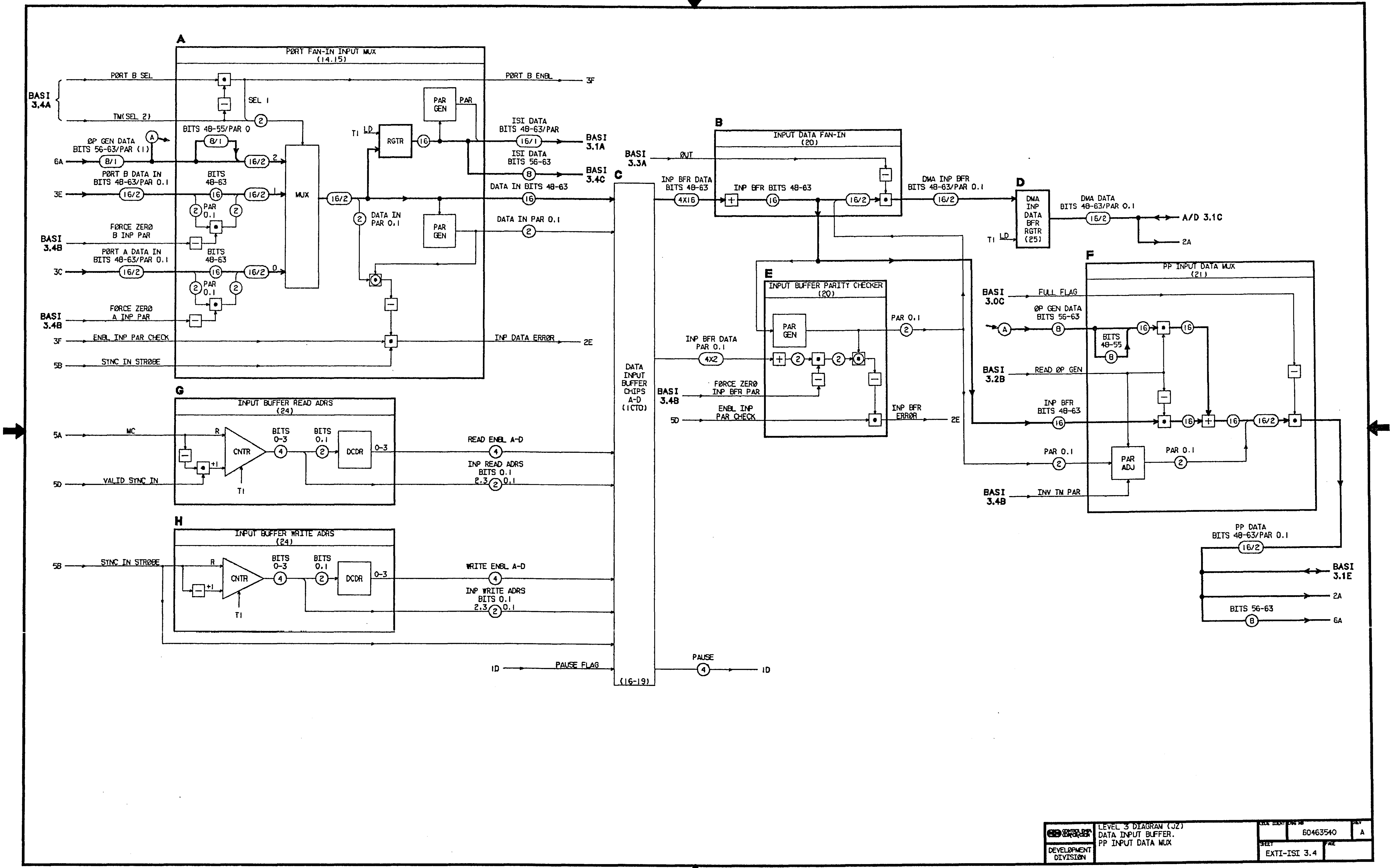
CODE IDENT
DWG NO 60463540
REV C
SHEET EXTI-ISI 3.2
PAGE



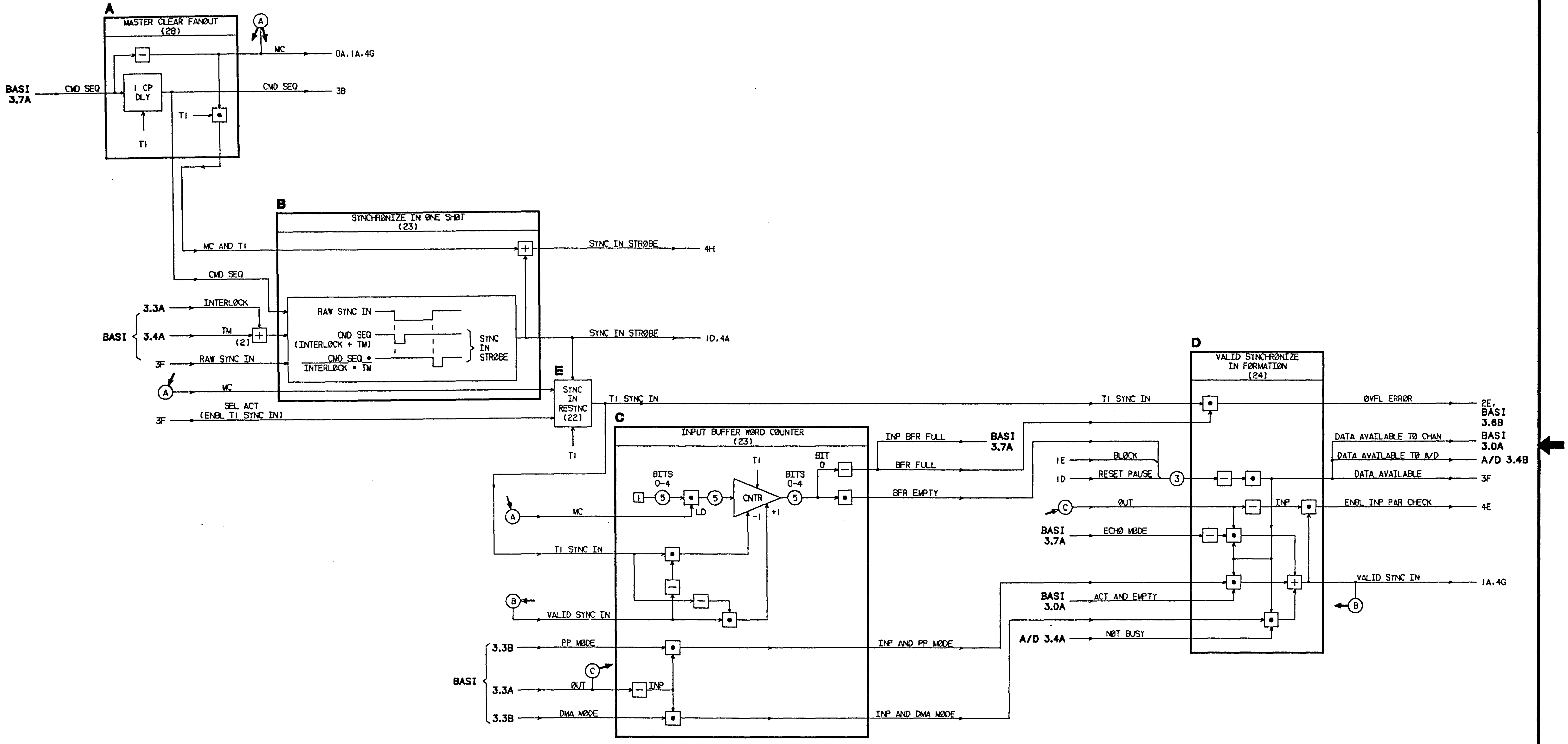
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JZ)
PORTS A,B TRANSMITTERS
AND RECEIVERS, CONTROL
SIGNAL INPUT MUX

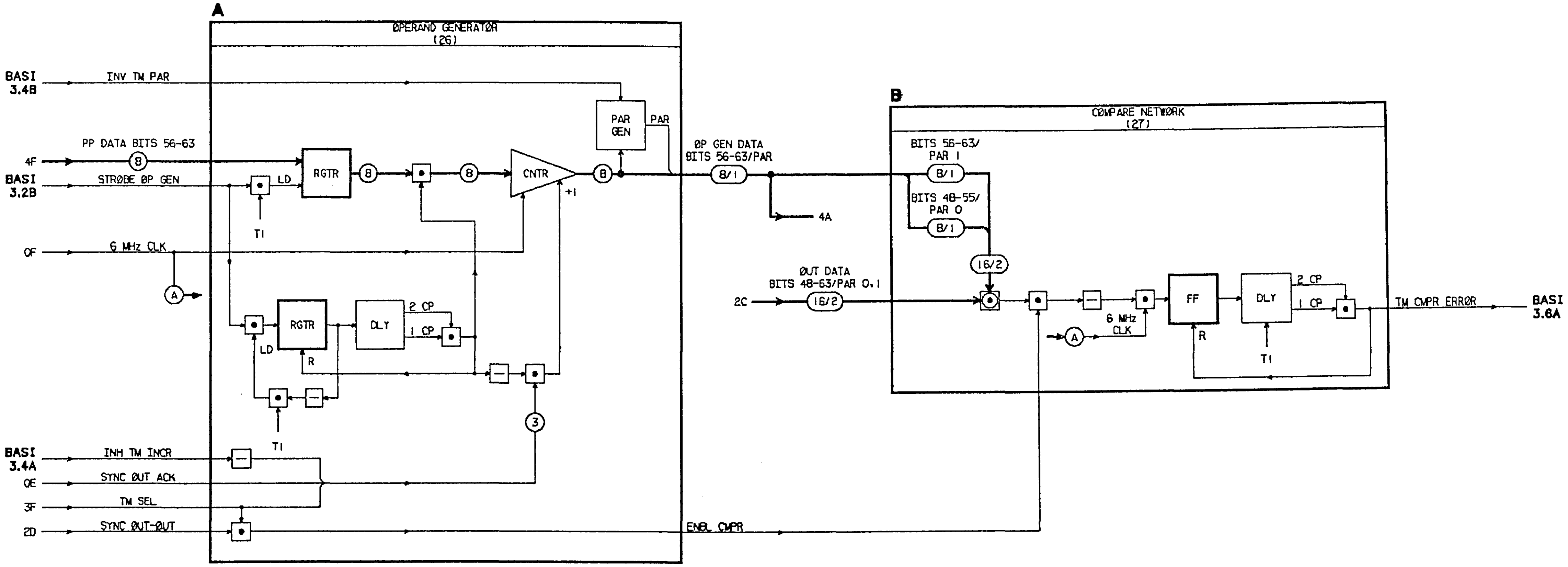
CODE IDENT	DWG NO	REV
	60463540	C
SHEET	EXTI-ISI 3.3	PAGE



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JZ)
DATA INPUT BUFFER.
PP INPUT DATA MUX
60463540
A
EXTI-ISI 3.4



CONTROL DATA	LEVEL 3 DIAGRAM (JZ) INPUT BUFFER WORD COUNTER, SYNCHRONIZER	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION		SHEET EXTI-ISI 3.5	PAGE	



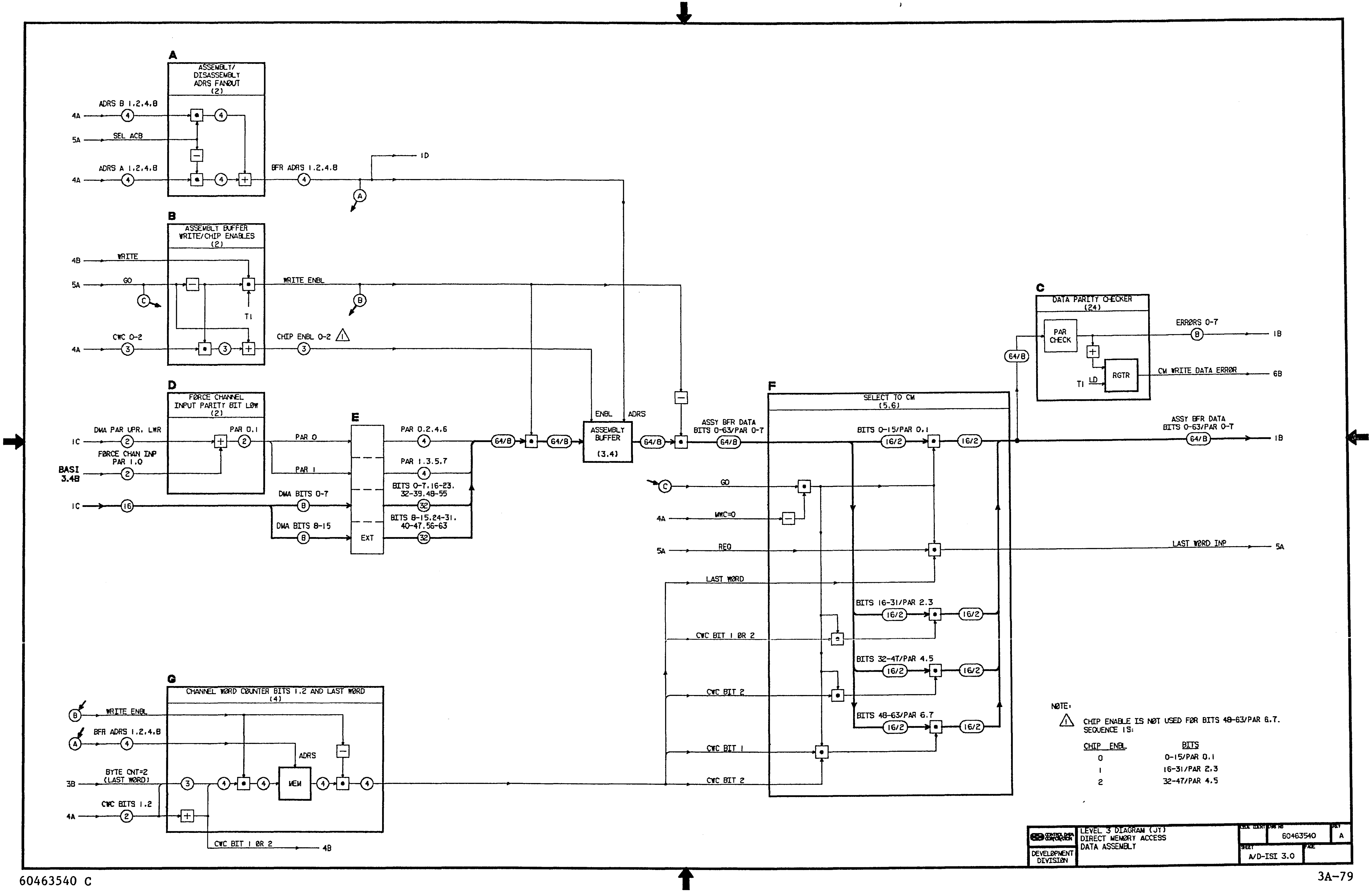
CONTROL DATA CORPORATION

DEVELØPMENT
DIVISIØN

LEVEL 3 DIAGRAM (JZ)
ØPERAND GENERATØR.
CØMPARE NETWØRK

CODE IDENT DWG NO 60463540 REV A

SHEET EXTI-ISI 3.6 PAGE

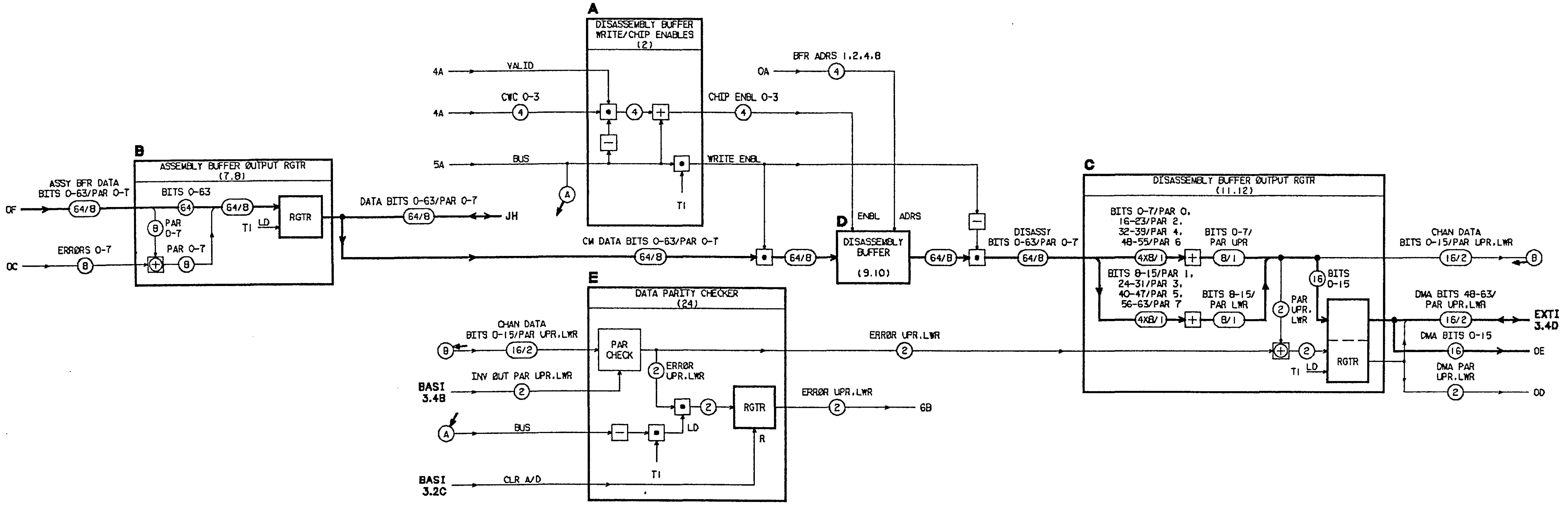


NOTE:

⚠ CHIP ENABLE IS NOT USED FOR BITS 48-63/PAR 6,7.
SEQUENCE IS:

CHIP ENBL	BITS
0	0-15/PAR 0,1
1	16-31/PAR 2,3
2	32-47/PAR 4,5

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JY)
DIRECT MEMORY ACCESS
DATA ASSEMBLY
DWG NO 60463540
REV A
SHEET A/D-ISI 3.0

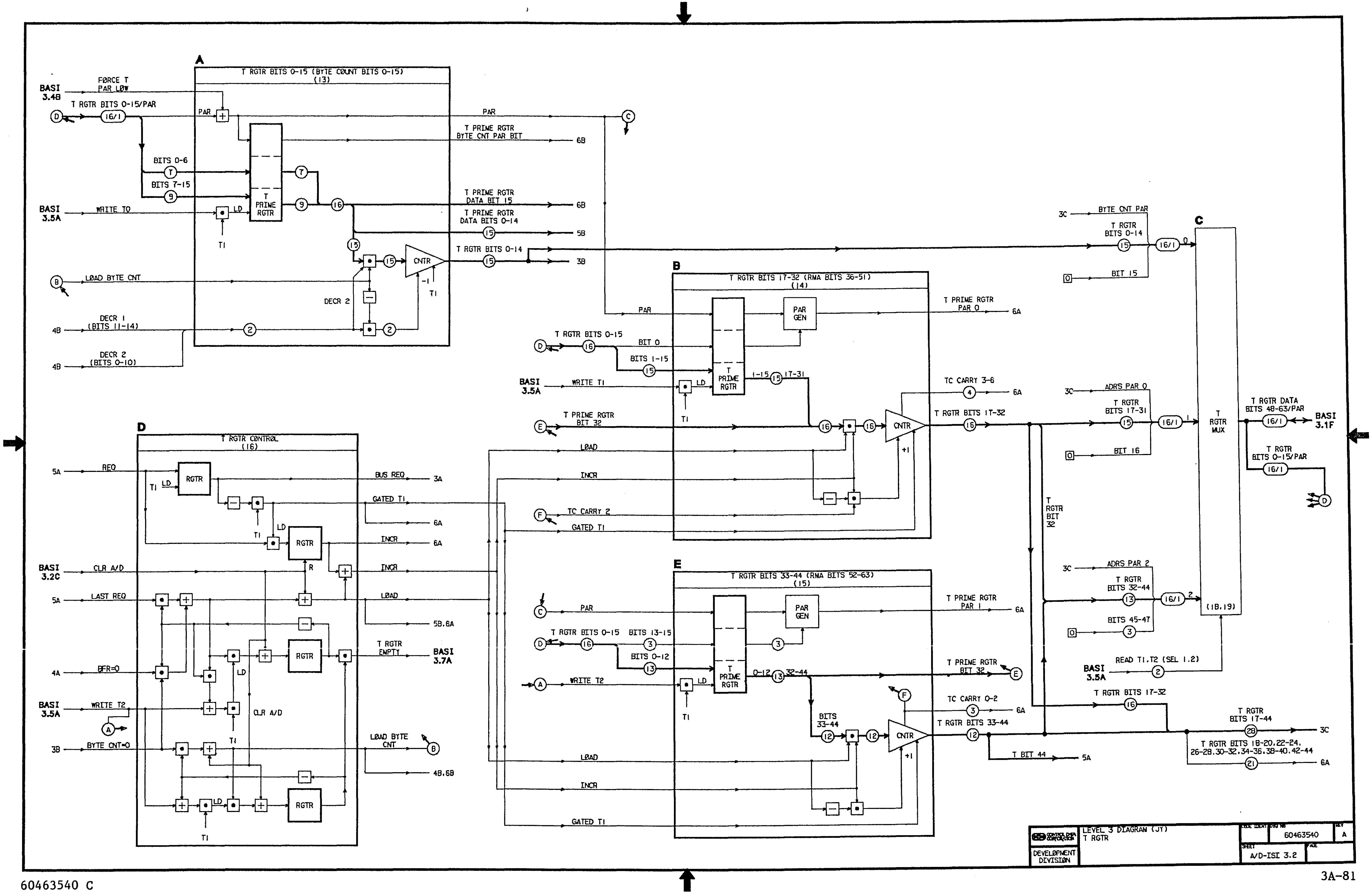


NØTE:

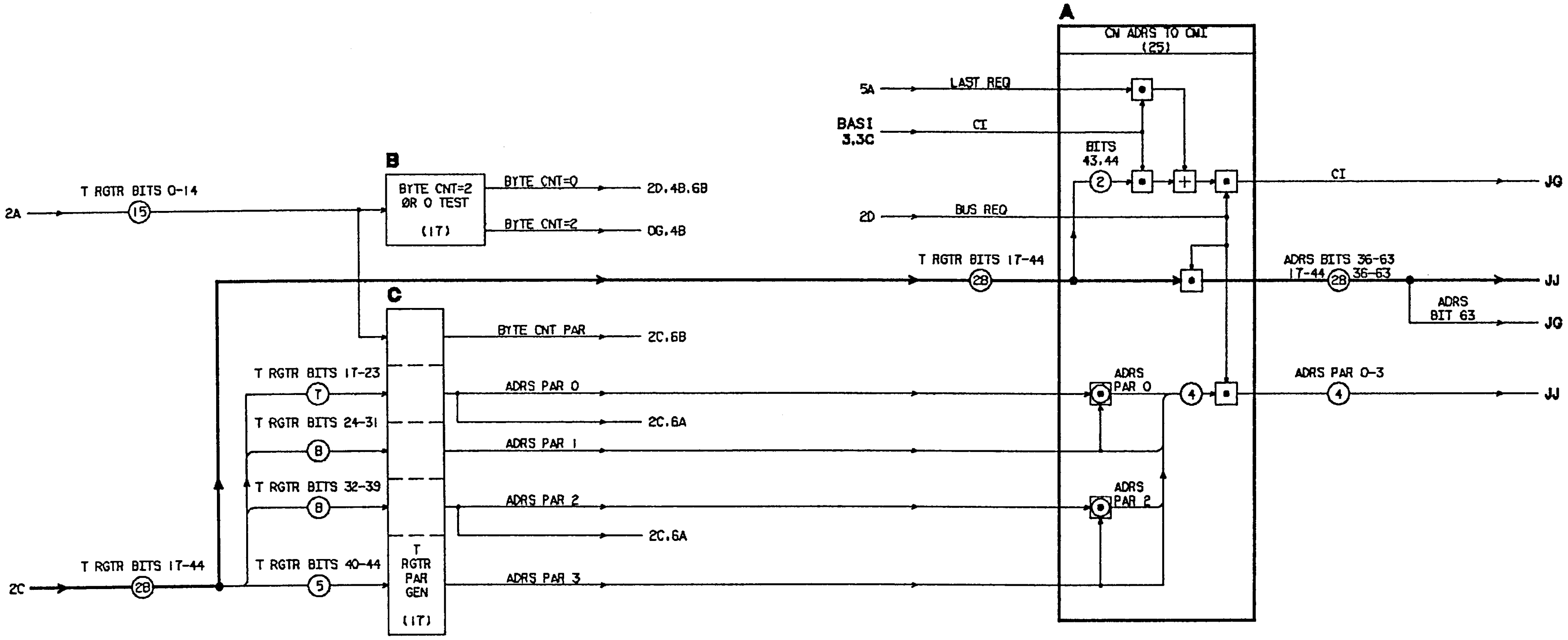
⚠ CHIP ENABLE SEQUENCE IS:

CHIP ENBL	BITS
0	0-15/PAR 0.1
1	16-31/PAR 2.3
2	32-47/PAR 4.5
3	48-63/PAR 6.7

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 3 DIAGRAM (JY)
CM DATA DISASSEMBLY
CODE IDENT
DWG NO 60463540
REV A
SHEET A/D-ISI 3.1
PAGE



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JT)
T RGTR
60463540
A
A/D-ISI 3.2



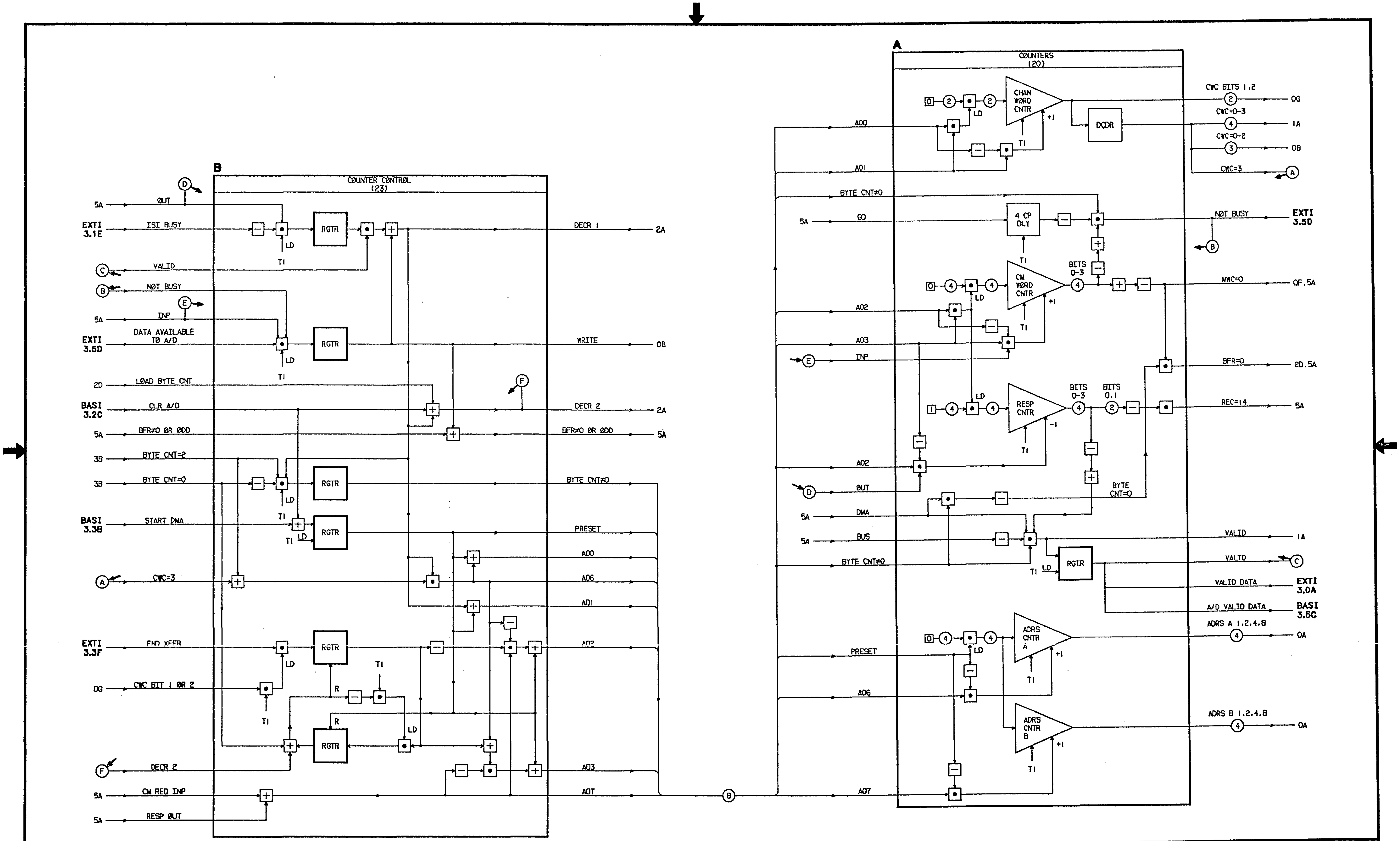
CONTROL DATA CORPORATION

DEVELØPMENT DIVISIØN

LEVEL 3 DIAGRAM (JY)
CM ADRS TØ CMI

60463540 A

SHEET A/D-ISI 3.3



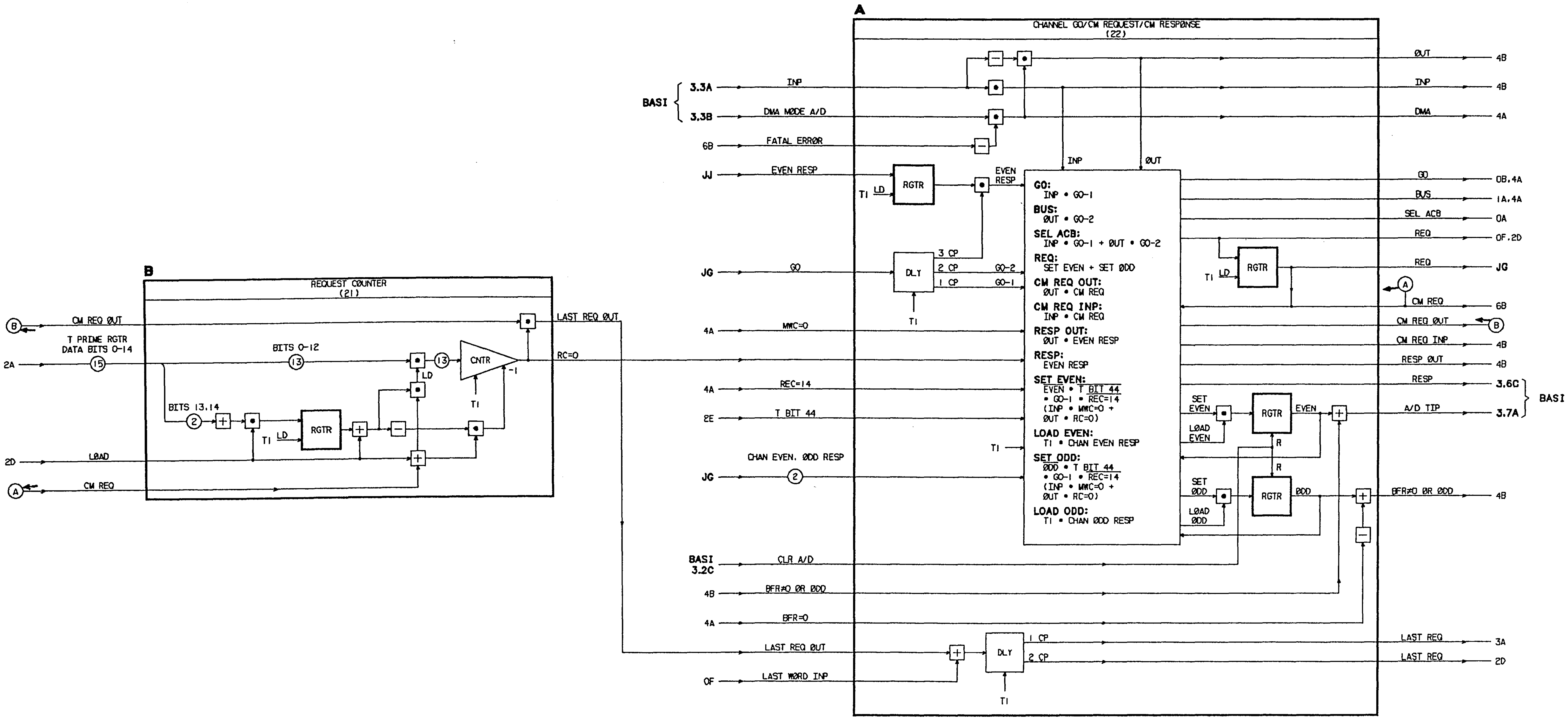
CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
CHANNEL WORD, CW WORD,
RESPONSE, AND
ADRS COUNTERS

CODE IDENT | DWG NO 60463540 | REV A

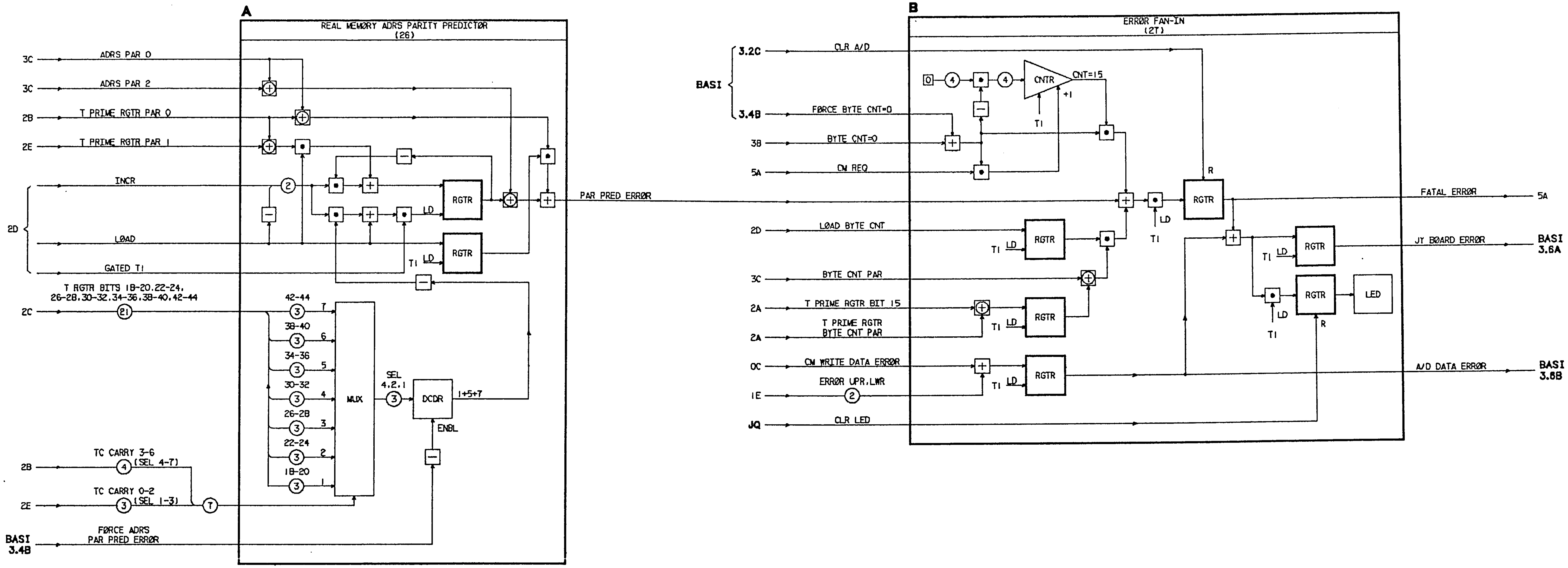
SHEET A/D-ISI 3.4 | PAGE



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
ASSEMBLY/DISASSEMBLY
CONTROL

60463540 | F
A/D-ISI 3.5



CONTROL DATA CORPORATION

DEVELØPMENT DIVISIØN

LEVEL 3 DIAGRAM (JY)
ERRØR DETECTØR

CODE IDENT	DWG NO	REV
	60463540	A

SHEET	PAGE
A/D-ISI 3.6	

DMA ENHANCED C170 CHANNEL ADAPTER (DMA-170 0.0)

ADAPTER OVERVIEW

The DMA-Enhanced CYBER 170 Channel Adapter (170 adapter) can be installed in any of ten channel locations in the CIO cabinet. This option provides an interface between a CIO PP and a standard 170 channel. In addition to the standard 170 protocol, this adapter supports the fast-transfer capabilities of the Extended Semiconductor Memory (ESM) II low-speed port. A PP controls the adapter by issuing functions and sending data using standard PP I/O instructions.

The adapter enables the PP to transfer data between the external device and PPM using standard I/O instructions. In addition, the adapter may transfer data between the external device and CM. This data flow is called DMA. The PP operates concurrently with the adapter during DMA data transfers. This allows the PP more time to process I/O requests from the CPU. The primary purpose of the adapter is to allow DMA transfers between a buffer residing in scattered pages of CM and an external device.

An I/O request consists of a list of commands. This list contains control information for the external device and data transfer length/address pairs for the adapter. These length/address pairs define the RMA (word boundary) and length (bytes) in the CM buffer. Due to the physical sectoring of some external devices, the PP separates single length/address pairs into multiple pairs. This forces a transfer to end on a physical boundary. For disk I/O devices, the PP adds control words to the beginning of each sector.

FUNCTION REGISTER AND DECODE PROMs

The adapter monitors the most significant bit of the 16-bit function word from the PP. If bit 48 is a one, the function word is an adapter function. If zero, the lower 12 bits of the function word go to the external device. The adapter translates the function word to determine the specified operation. Adapter function codes are in the following listing and described in the following paragraphs.

Code (Hex)†	Function
8000	Master Clear
8200	Clear T
84XX	Start DMA Input
86XX	Start DMA Output
8800	Clear DMA Mode
8C00	Disable Test Mode
8E00	Enable Test Mode
9000	Read Control Register
9200	Write Control Register
9400	Read Error Status Register
9800	Read Operational Status Register
9C00	Read T
9E00	Write T Prime (T´)

---

†XX specifies PP word count.

Function codes 8AXX, 96XX, and 9AXX are not used. If these codes are received, the adapter remains active and full. The adapter responds with an inactive status only when a used function is received.

MASTER CLEAR (8000)

This function clears the Control, Error Status, and T Registers. The adapter goes inactive and empty with the channel and error flags cleared. Also, DMA mode clears and a 1-microsecond master clear pulse goes to the external device.

CLEAR T (8200)

This function clears the T Registers, DMA mode, and all DMA buffers and holding registers. An inactive out signal is not sent to the external device when DMA mode clears.

START DMA INPUT/OUTPUT (84XX/86XX)

These functions initiate DMA transfers. The start DMA input function transfers data from the external device to CM. The start DMA output function transfers data from CM to the external device. Bit 55 of the function word (set) enables the transfer between CM and ESM-II in fast transfer mode. Bits 56 through 63 specify the number of words the PP may transfer before going into DMA mode. After receiving these functions, the adapter performs the following tasks.

1. Sends an active out signal to the external device.
2. Clears DMA mode (if previously set).
3. Loads bits 56 through 63 into the PP Word Counter.

The DMA transfer starts when the PP word count is zero and the T Register byte count is greater than zero.

CLEAR DMA MODE (8800)

This function terminates DMA mode. If a transfer is in progress, it stops and cannot be restarted. The adapter sends an inactive out signal to the external device indicating the end of a transfer.

DISABLE TEST MODE (8C00)

This function clears test mode and DMA mode. The adapter returns to the normal state.

ENABLE TEST MODE (8E00)

This function enables three separate testing options.

1. If the adapter is not in DMA mode, PP output data feeds back through Adapter Output Register Rank I, Transmit Register, Deskew Register, Input Resynchronize Buffer, and Adapter Input Register Rank II where it is available to the PP.
2. If the adapter is in DMA input mode, PP output data is assembled and written into CM.
3. If the adapter is in DMA output mode, CM data is disassembled into Adapter Input Register Rank II where it is available to the PP.

READ CONTROL REGISTER (9000)

This function enables the PP to read the Control Register. After the PP sends this function and an activate, the adapter responds with an input register full and the contents of the Control Register.

WRITE CONTROL REGISTER (9200)

This function enables the PP to write to the Control Register. After the PP sends this function and an activate, the adapter accepts the following output data as Control Register write data.

READ ERROR STATUS REGISTER (9400)

This function enables the PP to read the Error Status Register. After the PP sends this function and an activate, the adapter responds with an input register full and the contents of the Error Status Register. This function clears the Error Status Register and the error flag.

READ OPERATIONAL STATUS REGISTER (9800)

This function enables the PP to read the Operational Status Register. After the PP sends this function and an activate, the adapter responds with an input register full and the contents of the Operational Status Register.

READ T (9C00)

This function enables the PP to read the T Register. After the PP sends this function and an activate, the adapter sends three 16-bit words which contain the current contents of the T Register in the following order.

1. Byte count bits 0 through 15
2. CM address bits 36 through 51
3. CM address bits 52 through 63

WRITE T PRIME (9E00)

This function enables the PP to write to the T Prime Register. After the PP sends this function and an activate, the adapter accepts the next three 16-bit words as T Prime Register write data in the following order.

1. Byte count bits 0 through 15
2. CM address bits 36 through 51
3. CM address bits 52 through 63

If the PP sends more than three words, the fourth word remains in Adapter Input Register Rank II and the full flag remains set.

CONTROL REGISTER

The Control Register selects the different operating modes for the adapter. The PP reads or writes this register using the 9000 or 9200 function, respectively. A master clear function (8000), power-on master clear, or channel master clear through the Input/Output Unit (IOU) Maintenance Access Control (MAC) clears this register.

Control register bit assignments and descriptions are as follows:

Bit	Description
48	Enable Cache Invalidate
49	Not Used
50	60-Bit Mode
51	Enable Test Clock
52	Disable External Clock
53	Block Full Out
54	Enable Overflow
55	Disable Error Register Clear
56	Enable Force Error Codes
57-58	Not Used
59-63	Force Error Codes

ENABLE CACHE INVALIDATE (BIT 48)

This bit enables a cache invalidate signal with every fourth and last word written to CM during a DMA transfer.

60-BIT MODE (BIT 50)

When set, this bit allows DMA data transfers between 12-bit channel words and 60-bit CM words. When clear, this bit allows transfers between 12-bit channel words and 64-bit CM words.

ENABLE TEST CLOCK (BIT 51)

This bit enables the generation of a 10-MHz clock which simulates the external clock from the ESM-II. This allows the testing of fast transfers. Setting or clearing this bit causes a clock fault in the Error Status Register.

DISABLE EXTERNAL CLOCK (BIT 52)

This bit disables the test clock or the external clock from the ESM-II. This bit allows testing of the adapter in a synchronous state when the external device is an ESM-II. Setting this bit causes a clock fault in the Error Status Register if an external clock is present.

BLOCK FULL OUT (BIT 53)

This bit prevents sending full out signals to the external device. If this bit is set during a DMA output transfer, output data backs up in the Disassembly Buffer. This allows checking the output data path.

ENABLE OVERFLOW (BIT 54)

When in test mode, this bit enables testing the Input Resynchronize Buffer overflow detection network. An overflow error occurs if the PP outputs more than 10 words.

DISABLE ERROR REGISTER CLEAR (BIT 55)

This bit disables clearing the Error Status Register during a PP test and clear channel c error flag set (SFM) or clear (CFM) instruction. After this bit is set, the Error Status Register is cleared only by a read error status register function, a master clear function, or a channel master clear through the IOU MAC.

ENABLE FORCE ERROR CODES (BIT 56)

This bit enables the decoding of Control Register bits 59 through 63.

FORCE ERROR CODES (BITS 59-63)

When bit 56 is set, these bits are decoded to enable testing of the parity networks. Hexadecimal codes 01, 02, 04 through 06, 10 through 13, and 20 through 26 are described in the following paragraphs.

Invert PROM Parity (01)

This code inverts the parity bit for the Function Decode PROMs. The KX error sets in the Error Status Register along with the KX board LED.

Invert Input Data Parity (02)

With this code and the adapter full, the KX error sets in the Error Status Register along with the KX board LED. If the PP inputs data, bad parity returns to the barrel and slot. This causes a conversion error on the JW board (bit 44 of fault status I). The JW board LED lights and an error bit sets in fault status I for the PP inputting the data.

Force Invalid Response (04)

This code causes an illegal translation of the CM response code during an actual CM reference. The invalid response bit sets in the Error Status Register.

Invert Response Code Parity (05)

This code inverts the parity bit of the CM response code at the parity checker during an actual CM reference. The KX error sets in the Error Status Register and the KX board LED lights.

Invert Control Register Parity (06)

This code inverts the parity bit of the Control Register at the parity checker. The KX error sets in the Error Status Register and the KX board LED lights.

Invert Shifter Parity (10)

This code inverts the parity bit of the 12/16 Conversion Shifter at the parity generator during a DMA input or output transfer. The 12/16 conversion error and KZ error set in the Error Status Register and the KZ board LED lights.

Invert Conversion Parity (11)

This code inverts the parity bit of the conversion data at the parity checker during a DMA input or output transfer. The 12/16 conversion error and KZ error set in the Error Status Register and the KZ board LED lights.

Invert Transmit Register Parity (12)

This code inverts the parity bit of the Transmit Register at the parity checker during a DMA output transfer. The KZ error sets in the Error Status Register and the KZ board LED lights. If not in test mode, bad parity goes to the external device. If in test mode, input data error sets in the Error Status Register.

Invert Input Parity (13)

This code inverts the parity bit of the input data at the parity checker during a DMA input transfer. The KZ error and input data error set in the Error Status Register and the KZ board LED lights.

Force Channel Input Parity 0,1 (20/21)

These codes force the parity bit low for bits 48 through 55 (parity 0) and bits 56 through 63 (parity 1) as DMA input data enters the Assembly Buffer. When the 64-bit CM word leaves the buffer, a parity error is detected. The JY error and assembly/disassembly data error set in the Error Status Register and the JY board LED lights.

Force T Parity Low (22)

This code forces the parity bit low for T Register data as it enters the T Prime Register. When T-prime data transfers to the T Register, a parity error is detected. The JY error sets in the Error Status Register and the JY board LED lights. This error inhibits CM requests until the adapter is master cleared or a clear T function is issued by the PP.

Invert Output Parity Upper/Lower (23/24)

These codes invert the parity bit for bits 48 through 55 (upper) and bits 56 through 63 (lower) as DMA output data leaves the Disassembly Buffer. The JY error, KZ error, and assembly/disassembly data error set in the Error Status Register and the JY and KZ board LEDs light.

Force Address Parity Prediction Error (25)

This code forces the RMA parity predictor to predict the parity bit will change state on every CM reference. A parity prediction error causes the JY error to set in the Error Status Register and the JY board LED lights. This error inhibits CM requests until the adapter is master cleared or a clear T function is issued by the PP.

Force Byte Count Equal to Zero (26)

This code forces the CM request counter to report an error after 16 CM requests are issued. This condition stimulates the constant CM request counter. The JY error sets in the Error Status Register and the JY board LED lights. This error inhibits CM requests until the adapter is master cleared or a clear T function is issued by the PP.

OPERATIONAL STATUS REGISTER

This read-only register provides information regarding the state of the adapter and 170 channel during DMA transfers. The PP reads this register using the 9800 function. This status allows the PP to control the operation of the adapter.

Operational status register bit assignments and descriptions are as follows:

Bit	Description
48-51	Zero
52	Output Buffer Full
53	Input Buffer Full
54	Data Available to Channel
55	Fast Transfer
56	External Clock Present
57	Test Mode
58	PP Word Count Equal to Zero
59	DMA Output
60	DMA Input
61	DMA Halted
62	T Register Empty
63	Transfer in Progress

OUTPUT BUFFER FULL (BIT 52)

This bit indicates the Output Resynchronize Buffer contains four 12-bit channel words.

INPUT BUFFER FULL (BIT 53)

This bit indicates the Input Resynchronize Buffer contains eight 12-bit channel words.

DATA AVAILABLE TO CHANNEL (BIT 54)

This bit indicates the Input Resynchronize Buffer contains at least one 12-bit channel word.

FAST TRANSFER (BIT 55)

This bit indicates the adapter is in DMA mode with fast transfers enabled.

EXTERNAL CLOCK PRESENT (BIT 56)

This bit indicates the adapter is receiving a clock from ESM-II. This clock must be present before fast transfers are executed.

TEST MODE (BIT 57)

This bit indicates the adapter is in test mode which allows checking all internal data paths and associated control circuits. The PP puts the adapter in test mode using the 8E00 function. The adapter remains in test mode until the PP issues a disable test mode function (8C00) or a master clear function (8000), or the IOU MAC sends a master clear.

PP WORD COUNT EQUAL TO ZERO (BIT 58)

This bit indicates the PP Word Counter has decremented to zero. The PP Word Counter is loaded from the least significant eight bits of the start DMA functions (84XX or 86XX) and is decremented by one for each word transferred.

DMA OUTPUT (BIT 59)

This bit indicates the adapter is attempting a DMA output transfer. The transfer occurs if the T Register byte count is nonzero and DMA halted (bit 61) is not present. This bit sets when a start DMA output function (86XX) is issued and the PP word count is zero. This bit clears when any of the following conditions occur.

- Master clear function (8000)
- Clear T function (8200)
- Start DMA input function (84XX)
- Clear DMA mode function (8800)
- Disable test mode function (8C00)
- Master clear from IOU MAC
- Power-on master clear

DMA INPUT (BIT 60)

This bit indicates the adapter is attempting a DMA input transfer. The transfer occurs if the T Register byte count is nonzero and DMA halted (bit 61) is not present. This bit sets when a start DMA input function (84XX) is issued and the PP word count is zero. This bit clears when any of the following conditions occur.

- Master clear function (8800)
- Clear T function (8200)
- Start DMA output function (86XX)
- Clear DMA mode function (8800)
- Disable test mode function (8C00)
- Master clear from IOU MAC
- Power-on master clear

DMA HALTED (BIT 61)

This bit indicates the external device sent an inactivate signal to the adapter during a DMA transfer.

If this condition occurs during a DMA output transfer, the data transfer to the external device is terminated. If the transfer is incomplete (byte count nonzero), the PP must issue a clear T function (8200) or a master clear function (8000) before starting a new transfer.

If this condition occurs during a DMA input transfer, the data transfer from the external device is terminated. All data in the Input Resynchronize Buffer is written into CM. If the transfer is incomplete (byte count nonzero), the PP must issue a clear T function (8200) or a master clear function (8000) before starting a new transfer.

T REGISTER EMPTY (BIT 62)

This bit indicates the T Prime Register is empty. The PP can now issue a write T function (9E00) which writes the T Prime Register.

TRANSFER IN PROGRESS (BIT 63)

This bit indicates the adapter issued a request to CM or the external device and has not received a response. In DMA mode, this bit is set during the entire transfer, provided the T Register is nonzero and all outstanding requests have not been honored.

ERROR STATUS REGISTER

This read-only register monitors the adapter's error checking circuits to determine if any hardware errors have occurred. The PP uses this error status for fault isolation and to determine the validity of a transfer. All error bits are ORed to form the adapter's error flag.

The Error Status Register and error flag are cleared differently in native 170 mode and enhanced mode. In native 170 mode with Control Register bit 55 clear, the Error Status Register and error flag are cleared when the PP executes a test and clear channel c error flag set (SFM) or clear (CFM) instruction. This allows the error flag to operate the same as for non-DMA 170 channels. In the enhanced mode with Control Register bit 55 set, the Error Status Register and error flag are not cleared by the SFM and CFM instructions. This allows the PP to use the SFM ad CFM instructions to determine if an error exists. Then the PP uses the read error status register function (9400) to determine the specific error and isolation information. In both modes, the Error Status Register and error flag are cleared by:

- Read error status register function (9400)
- Master clear function (8000)
- Master clear from IOU MAC

Error status register bit assignments and descriptions are as follows:

Bit	Description
48-49	Zero
50	Uncorrectable CM Error
51	CM Reject
52	Invalid Response
53	Any Response Code Parity Error
54	CMI Read Data Parity Error
55	Clock Fault
56	Overflow Error
57	Input Data Error
58	12/16 Conversion Error
59	A/D Data Error
60	BAS Parity Error
61	KZ Error
62	JY Error
63	KX Error

UNCORRECTABLE CM ERROR (BIT 50)

This bit indicates an uncorrectable error response was received from the Central Memory Interface (CMI).

CM REJECT (BIT 51)

This bit indicates a reject response was received from CMI.

INVALID RESPONSE (BIT 52)

This bit indicates the response code received from CMI decoded into an illegal value.

ANY RESPONSE CODE PARITY ERROR (BIT 53)

This bit indicates a parity error was detected on the CM response code. If KX error (bit 63) is set, the parity error was detected on the KX board; if not set, the error was detected in CMI.

CMI READ DATA PARITY ERROR (BIT 54)

This bit indicates the CMI detected a read data parity error during a DMA output transfer.

CLOCK FAULT (BIT 55)

This bit indicates a change was detected in the external clock. If this occurs during a DMA transfer, the adapter must be master cleared.

OVERFLOW ERROR (BIT 56)

This bit indicates data was received after the Input Resynchronize Buffer was full. The first word written into the buffer is overwritten by the last word received.

INPUT DATA ERROR (BIT 57)

This bit indicates a parity error was detected on the input data. The data is from the external device (normal DMA input transfer) or the Adapter Output Register Rank I (test mode).

12/16 CONVERSION ERROR (BIT 58)

This bit indicates a parity error was detected in the Conversion Network. The KZ error (bit 61) also sets.

A/D DATA ERROR (BIT 59)

This bit indicates a parity error was detected during assembly/disassembly of CM data. The JY error (bit 62) also sets.

BAS PARITY ERROR (BIT 60)

This bit indicates a parity error was detected in the output or function word received from the PP. The KX error (bit 63) also sets.

KZ ERROR (BIT 61)

This bit indicates the KZ board detected one of the following errors.

- Input data parity error
- Output data parity error
- 12/16 Conversion Shifter error
- Input Resynchronize Buffer overflow error

JY ERROR (BIT 62)

This bit indicates the JY board detected an error. If bit 59 is also set, the error was during assembly/disassembly and the transfer continues. If bit 59 is not set, one of the following errors occurred.

- RMA parity predictor error
- T Register byte count parity error
- Constant CM request error

These errors inhibit CM requests until the PP issues a clear T function or the adapter is master cleared.

KX ERROR (BIT 63)

This body indicates the KX board detected one of the following errors.

- Control Register parity error
- Adapter Output Register Rank I parity error
- Adapter Input Register Rank II parity error
- Function Decode PROM parity error
- KX response code parity error

MAC INTERFACE

Any PP can read certain registers in the adapter by doing a maintenance register read of the appropriate channel status register. For example, if the adapter is installed in CIO channel location 0, the PP does a maintenance register read on register B0. If installed in location 1, the read is on register B1. This continues through channel location 11 (octal) with the read on register B9. The format for the adapter's channel status is shown in the following listing.

Byte	Description
0	Error Status Register Bits 50-55

Bit	Description
0	Zero
1	Zero
2	Uncorrected CM Error
3	CM Reject
4	Invalid Response
5	Any Response Code Parity Error
6	CMI Read Data Parity Error
7	Clock Fault

1	Error Status Register Bits 56-63

Bit	Description
8	Overflow Error
9	Input Data Error
10	12/16 Conversion Error
11	A/D Data Error
12	BAS Parity Error
13	KZ Board Error
14	JY Board Error
15	KX Board Error

2	PP Word Counter Bits 56-63 (Bits 16-23)
3	Operational Status Register Bits 52-55

Bit	Description
24	Zero
25	Zero
26	Zero
27	Zero
28	Output Buffer Full
29	Input Buffer Full
30	Data Available to Channel
31	Fast Transfer

Byte	Description
4	Operational Status Register Bits 56-63

Bit	Description
32	External Clock Present
33	Test Mode
34	PP Word Count = 0
35	DMA Output
36	DMA Input
37	DMA Halted
38	T Register Empty
39	Transfer in Progress

5	Channel Flags

Bit	Description
40	Zero
41	Zero
42	Full I
43	Full II
44	Active
45	Full I or Full II
46	Error Flag
47	Channel Flag

6	Control Register Bits 48-55

Bit	Description
48	Enable Cache Invalidate
49	Zero
50	60-Bit Mode
51	Enable Test Clock
52	Disable External Clock
53	Block Full Out
54	Enable Overflow
55	Disable Error Register Clear

7	Control Register Bits 56-63

Bit	Description
56	Enable Force Error Codes
57	Zero
58	Zero
59	Force Error Code Bit 0
60	Force Error Code Bit 1
61	Force Error Code Bit 2
62	Force Error Code Bit 3
63	Force Error Code Bit 4

DMA TRANSFERS

The PP specifies a DMA transfer by sending the starting CM address and the byte count to the adapter. All DMA transfers start on a CM address and end on a 16-bit CM word parcel. If the transfer does not end on a CM word boundary, the word is filled with ones.

The adapter holds the address and byte count in the T and T Prime Registers. DMA transfers execute from the T Register. T Prime is a shadow register which maintains the I/O transfer rate across discontinuous pages in CM. If the byte count in T decrements to zero and T Prime is empty, the DMA transfer is suspended until a new T value is available or the PP issues a clear DMA mode function.

The PP initiates a DMA transfer by issuing a start DMA input or output function and ends the transfer with a clear DMA mode function. Before starting a DMA transfer, the PP prepares the external device. For example, the PP issues a read function to the external device before issuing a start DMA input function to the adapter. After receiving the start DMA function, the adapter sends an activate out signal to the external device to indicate the start of a transfer. After receiving the clear DMA mode function, the adapter sends an inactivate out signal to the external device to indicate the end of a transfer.

By specifying the number of words to be transferred in the PP word count field of a start DMA function, the PP writes or reads data on the front end of a transfer. Each word transferred decrements the PP word count. When the count reaches zero, the DMA transfer starts. Uses of this feature include supplying header information for disk systems and addresses for ESM-II.

FAST DMA TRANSFERS

The adapter supports the fast-transfer mode of the ESM-II low-speed port. Fast transfers are in DMA mode and have a transfer rate of one 12-bit word every 100 nanoseconds (120 million bits per second). An external clock from ESM-II enters the adapter to enable this fast transfer rate. Bit 55 of the start DMA input/output function enables fast transfers.

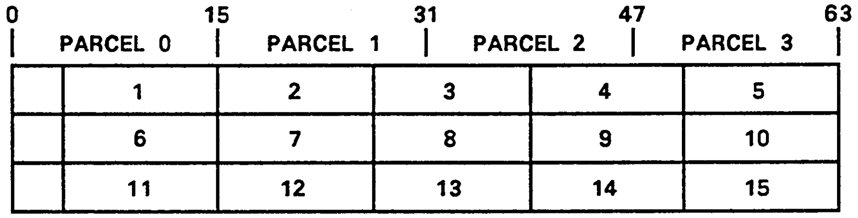
External interface signals are the same as standard 170 channels except active in, empty in, and empty out. Active in receives the asynchronous 10-MHz clock from ESM-II. All input/output transmissions are synchronized to this clock. A switch in the ESM-II low-speed port enables this clock. Empty out controls inputs from ESM-II. If the adapter issues an empty out, ESM-II inhibits the next full in. Empty in controls outputs from the adapter. If ESM-II issues an empty in, the adapter inhibits the next full out.

A typical sequence for executing a fast transfer is:

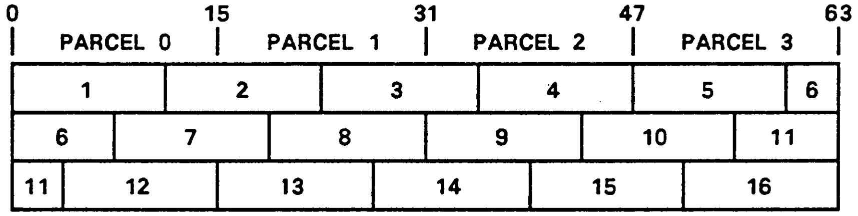
1. Master clear adapter.
2. Master clear ESM-II low-speed port.
3. Function adapter to read Operational Status Register. Check for external clock present.
4. Function adapter to write T Prime Register.
5. Function ESM-II low-speed port to enable fast transfers.
6. Function ESM-II low-speed port for a write operation.
7. Function adapter to start DMA output bit 55 set, and PP Word Count equals two.
8. Output two words from PP. This is the ESM-II address. DMA output transfer starts immediately after last word of address.
9. Function adapter to read Operational Status Register. Wait for transfer to complete.
10. Function adapter to clear DMA mode.
11. Function ESM-II low-speed port to read status.
12. Verify that transfer completed without errors.

CHANNEL/CM DATA MAPPING

For 60-bit CM, five 12-bit channel words map evenly into a CM word. The four most-significant bits (0 through 3) in the CM word are not used for reads and zeros for writes. Fifteen channel words map into parcels 0 through 3 at three CM locations as shown in the following figure.



For 64-bit CM, the 12-bit channel words do not map evenly into a CM word. Three CM locations are required for 16 channel words as shown in the following figure.



DATA PATHS

The following paragraphs describe the adapter data paths for each of the transfers.

PP TO T PRIME REGISTER

The PP writes three words into the T Prime Register through Adapter Output Register Rank I and T Register Data In and Out.

PP FROM T REGISTER

The PP reads three words from the T Register through Adapter Input Register Rank II.

PP TO FUNCTION REGISTER, CONTROL REGISTER, AND PP WORD COUNTER

The PP writes these registers and counter through Adapter Output Register Rank I.

PP FROM STATUS AND CONTROL REGISTERS

The PP reads these registers through Adapter Input Register Rank II.

INTER-PP TRANSFER

Data passes from one PP to another PP through Adapter Output Register Rank I and Adapter Input Register Rank II.

PP OUTPUT TRANSFER

Data passes from the PP to the external device through Adapter Output Register Rank I and the Transmit Register. The data also enters rank II but is not used. Data remains in the Transmit Register until the external device sends an empty signal.

PP INPUT TRANSFER

Data passes from the external device to the PP through the Deskew Register, Input Resynchronize Buffer, and Adapter Input Register Rank II. Up to eight words enter the buffer before input data stops. The adapter sends empty status to the external device until the buffer is full. When rank II accepts a word, the buffer accepts another word from the external device.

DMA OUTPUT TRANSFER

Data passes from CM to the external device as follows.

1. CM sends a 64-bit word to the Disassembly Buffer.
2. Disassembly Buffer separates the 64-bit word into four 16-bit parcels.
3. Conversion Network converts the 16-bit CM parcels to 12-bit channel words. Residue of the four bits from the first parcel is held until the second parcel arrives. Residue from the first parcel and eight bits from the second parcel form the second channel word. This process continues until all CM data is exhausted.
4. Conversion Network sends 12-bit channel words to the external device through the Output Resynchronize Buffer and Transmit Register.

DMA INPUT TRANSFER

Data passes from the external device to CM as follows.

1. External device sends 12-bit channel words to the Conversion Network through the Deskew Register and Input Resynchronize Buffer.
2. Conversion Network converts 12-bit channel words to 16-bit CM parcels. The first channel word is held until the second word arrives to form the first CM parcel. Residue of the eight bits from the second word is held until the third word arrives to form the second CM parcel. This process continues until all channel data is exhausted.
3. Conversion Network sends 16-bit CM parcels to the Assembly Buffer.
4. Assembly Buffer combines four 16-bit CM parcels into a 64-bit word and sends it to CM.

TEST MODE

The following paragraphs describe data paths and typical programming sequences for the adapter in test mode.

PP TRANSFERS

This test substitutes the PP for the external device during PP input and output transfers. Up to ten 12-bit words pass from the PP back to the PP through Adapter Output Register Rank I, Transmit Register, Deskew Register, Input Resynchronize Buffer, and Adapter Input Register Rank II. All ten words are held in the adapter before they return to the PP for compare testing. The eighth word in the Input Resynchronize Buffer is a duplicate of the Transmit Register contents. The programming sequence is:

1. Function adapter to set test mode.
2. Activate adapter.
3. Output up to ten 12-bit words.
4. Input data.
5. Check adapter for errors.
6. Compare data.
7. Repeat output/input until all patterns are checked.
8. Function adapter to clear test mode.

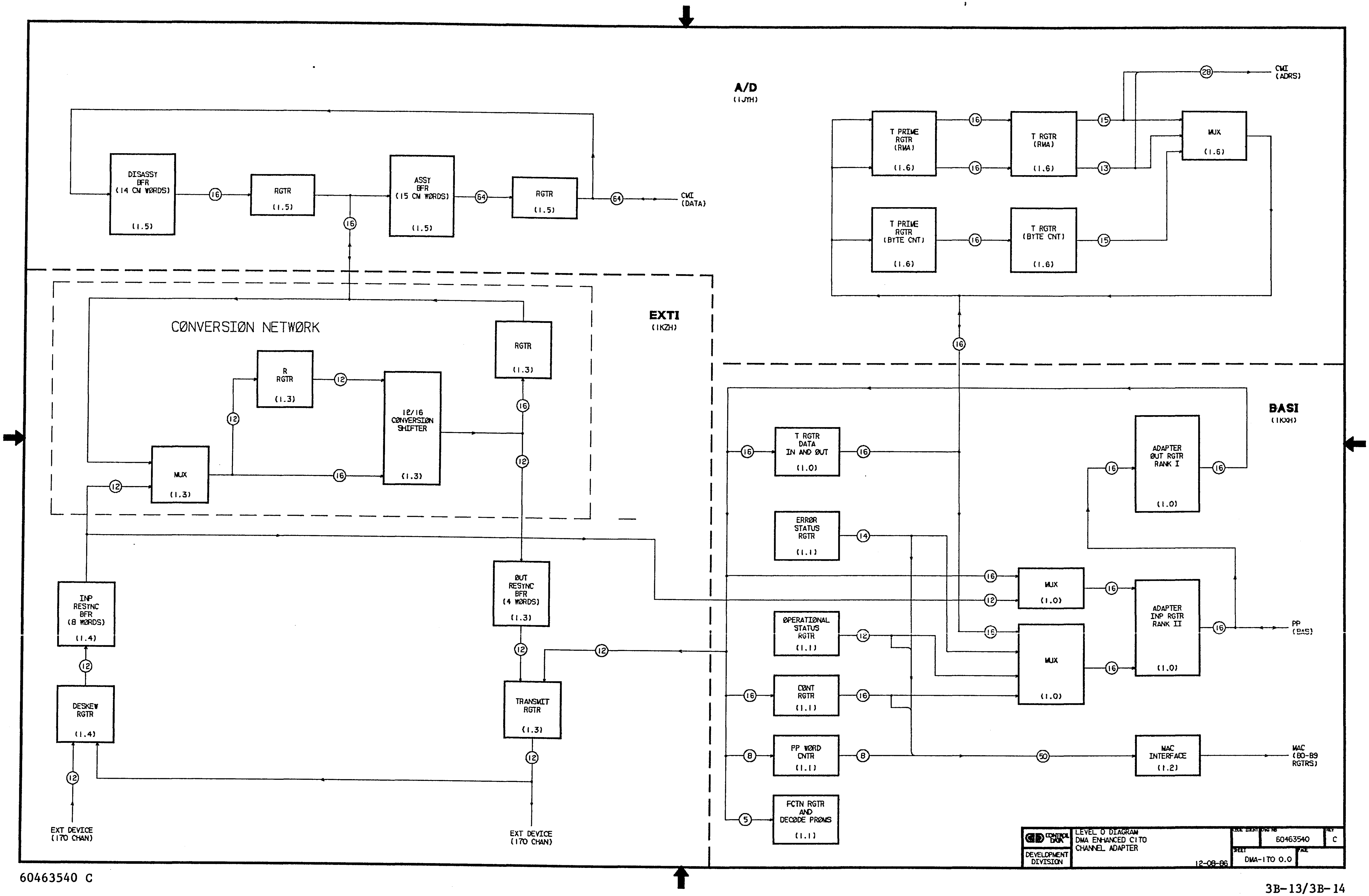
DMA TRANSFERS

This test substitutes the PP for the external device during the DMA input and output transfers. For DMA output transfers, data passes from CM to the PP through the Disassembly Buffer, Conversion Network, Output Resynchronize Buffer, Transmit Register, Deskew Register, Input Resynchronize Buffer, and Adapter Input Register Rank II. If fast transfer is enabled, data backs up in the buffers because the PP is slower than the fast transfer. For DMA input transfers, data passes from the PP to CM through Adapter Output Register Rank I, Transmit Register, Deskew Register, Input Resynchronize Buffer, Conversion Network, and Assembly Buffer. If fast transfer is enabled (Function Register bit 55 set), the enable test clock bit (Control Register bit 51) must be set. If the PP word count is zero, the programming sequence is:

1. Function adapter to set test mode.
2. Function adapter to write T Prime Register.
3. Activate adapter.
4. Output T values.
5. Deactivate adapter.
6. Function adapter to start DMA output or input.
7. Activate adapter.
8. Output or input test data.
9. Deactivate adapter.
10. Function adapter to clear DMA mode.
11. Function adapter to clear test mode.
12. Check Error Registers.
13. Check data.

If the PP word count is nonzero, the adapter goes into the outstanding DMA mode. Meanwhile, the PP simulates a PP input or output transfer of up to ten 12-bit words. When the PP transfer completes, the PP word count decrements to zero. The adapter goes into DMA mode and starts the DMA transfer. The programming sequence is:

1. Function adapter to set test mode.
2. Function adapter to write T Prime Register.
3. Activate adapter.
4. Output T values.
5. Deactivate adapter.
6. Function adapter to start DMA output or input. PP word count field contains quantity of 12-bit words to be echoed back to PP before DMA transfer starts.
7. Activate adapter.
8. Output up to ten 12-bit words.
9. Input words from step 8.
10. Check Error Register for PP transfers errors.
11. Repeat steps 8 through 10 until PP word count is zero.
12. Output or input test data.
13. Deactivate adapter.
14. Function adapter to clear DMA mode.
15. Function adapter to clear test mode.
16. Check Error Register for DMA transfer errors.
17. Check data.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 0 DIAGRAM
DMA ENHANCED CITO
CHANNEL ADAPTER

12-08-86

CODE IDENT	DWG NO	REV
	60463540	C
SHEET	PAGE	
DMA-ITO 0.0		

This diagram shows the data paths between the adapter and the PP. Data from the PP enters Adapter Output Register Rank I. Data to the PP leaves from Adapter 1. This diagram also shows microcode control and adapter flags.

ADAPTER OUTPUT REGISTER RANK I

All data from the PP to the adapter enters this register. Output data from this register goes to:

- Function Register (1.1G)
- Control Register (1.1A)
- PP Word Counter (1.1C)
- T Prime Register (1.6B)
- Transmit Register (1.3F)
- Adapter Input Register Rank II

This register also sends Function to the Transmit Register which sends Full Out (if data is being sent) or Function Out (if function is being sent) to the external device.

ADAPTER OUTPUT PARITY CHECKER

This circuit checks parity on data received from the PP. BAS Parity Error indicates the error was detected when data was entering Adapter Output Register Rank I. Rank I Parity Error indicates the error was detected after the register was loaded. After the parity is checked, this circuit regenerates parity for 12-bit channel words and 16-bit internal words.

T REGISTER DATA IN AND OUT

This circuit sends the address and byte count to the T Prime Register. If T Register Read/Write Control (1.1J) sends both Clear T and Read T, this circuit sends zeros (parity is a one) to the T Prime Register.

EXTERNAL INPUT DATA MUX

This multiplexer selects input data from the external device or output data from Adapter Output Register Rank I for input to the PP. Enable KZ Data signifies that data is available from the external device. If this signal is absent, output data from rank II is selected.

REGISTER SELECT MUX

This multiplexer selects the Control (1.1A), Error Status (1.2C), Operational Status (1.1F), or T Register (1.6B) contents for input to the PP. Selection of these internal functions is based on Function Register Bits 52 and 53.

ADAPTER INPUT REGISTER RANK II

This register sends data to the PP from the External Input Data Mux or the Register Select Mux.

ADAPTER INPUT PARITY CHECKER

This circuit checks parity on data in Adapter Input Register Rank II when the register is full. After the parity is checked, this circuit regenerates parity for the 16-bit words sent to the PP.

MICROCODE DECODE

This circuit decodes Microcode Bits 73 through 75 to determine which input/output instruction is being executed by the PP. Microcode Bit 85 sets the Channel Flag. PPMC Channel Select enables the decode.

Decode	Instruction
0	Function
1	Activate
2	Output
3	Input
4	Inactivate
5	Clear Error Flag
6	Clear Channel Flag
7	Not Used

Various adapter control signals enable the decodes. The rank designators associated with the output signals relate to PP slot times. Rank designators 0 and 4 do not relate to ranks I and II which are for the adapter´s output and input registers.

CHANNEL FLAG AND ACTIVE FLAG

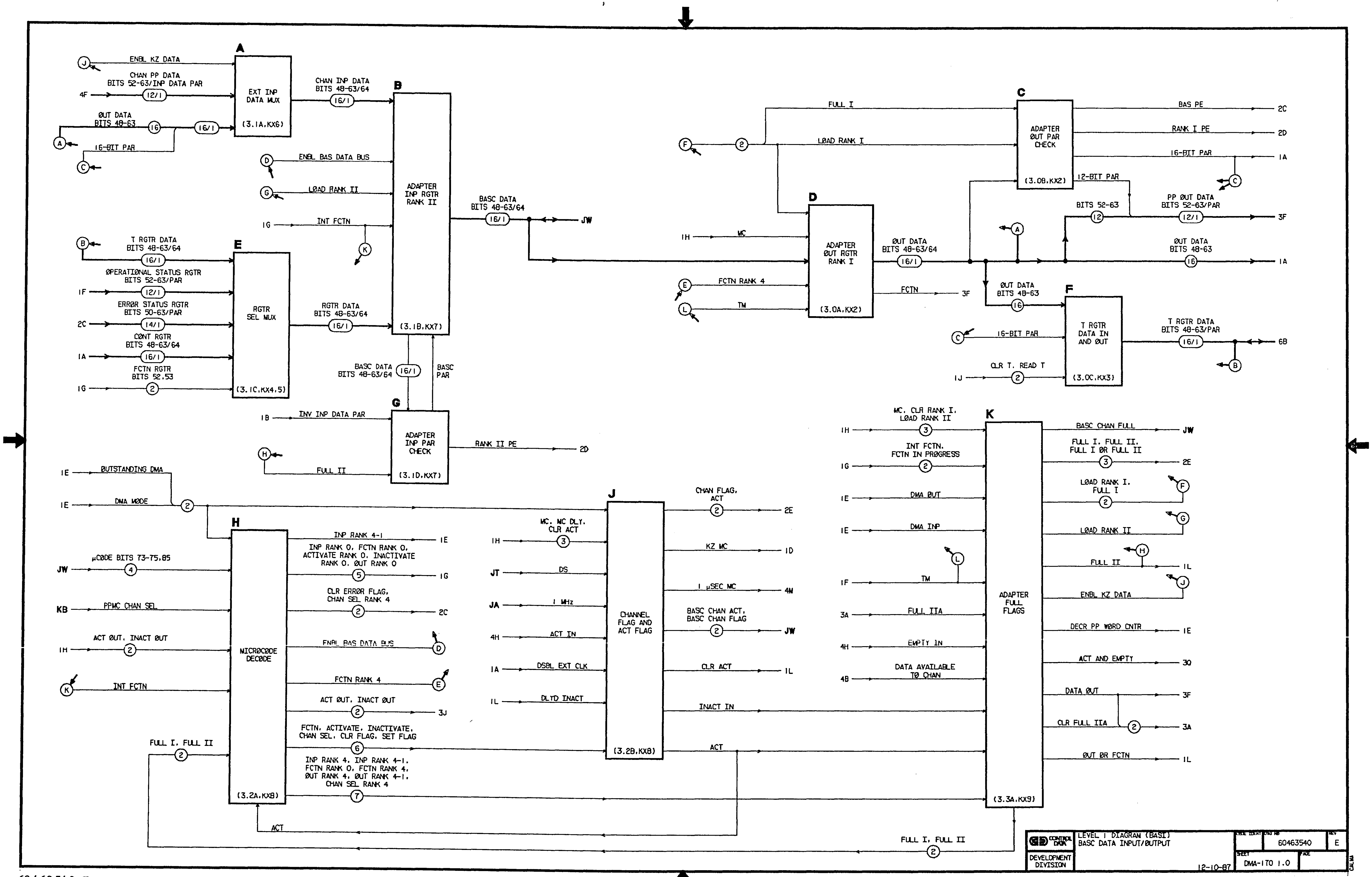
The Channel Flag is a programmable flag used by the operating system.

The Active Flag sets when the PP issues Activate or Function or the external device sends Active In during a PP transfer. This Flag clears when the PP issues Inactivate or the external device sends Inactive In during a PP transfer.

ADAPTER FULL FLAGS

This circuit controls data flow within the BASI. The following text describes the output signals.

- Load Rank I - Enables data into Adapter Output Register Rank I.
- Full I - Data is in Adapter Output Register Rank I.
- Load Rank II - Enables data into Adapter Input Register Rank II.
- Full II - Data is in Adapter Input Register Rank II.
- Data Out - Data for a PP output transfer is in rank I.
- Active and Empty - Rank II can accept data for a PP input transfer.
- Enable KZ Data - Enables data from external device into rank II during PP input transfer.
- Decrement PP Word Counter - External device has accepted word transmitted by adapter.
- Clear Full IIA - PP inputted data from rank II or master clear occurred.
- BASC Channel Full - Status to PP indicates rank I and/or rank II are full.
- Full I or Full II - Occurs during branch instruction and if ranks I and II are both full.



CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (BASI)
BASC DATA INPUT/ØUTPUT

12-10-87

60463540

E

DMA-1TO 1.0

This diagram shows the data path from Adapter Output Register Rank I (1.0D) to the Function Register, PP Word Counter, and Control Register. The Operational Status Network is also shown.

FUNCTION REGISTER

In addition to the Function Register, this circuit contains two FFs which are used for internal functions. Output Data Bit 48 indicates the PP issued an internal function. Internal Function remains set for the entire function. Function In Progress sets when Internal Function sets, but clears when the function should terminate. For example, on a write T function, this FF clears after the third word is written. If a fourth word is input, the cleared FF disables writing into T.

The Function Register holds seven bits of the Function Decode PROM Address. Function in Progress is the eighth bit. Each PP instruction causes a change to the address. The relationship between control signals and address bits is:

Bit	Signal
0	Function in Progress
1	Output Data Bit 51
2	Output Data Bit 52
3	Output Data Bit 53
4	Output Data Bit 54
5	Function Rank 0
6	Output Rank 0
7	Activate Rank 0 or Input Rank 0

FUNCTION DECODE PROMS A THROUGH E

These 4-bit, 256-location PROMs produce the control signals needed to execute the adapter´s functions. Each function changes the 8-bit address and, therefore, changes the state of the control signals.

POWER ON MASTER CLEAR

When power is applied to the adapter, the Function Register clears. This causes Function Decode PROM E to generate a Master Clear.

T REGISTER READ/WRITE CONTROL

This circuit controls the reading, writing, and clearing of the T Register (1.6). A 2-bit counter presets to 3 when the function is issued, and then increments to 0, 1, and 2. Count = 2 indicates the last word has been read or written.

DMA CONTROL FF´S

A start DMA input or output function sets the corresponding outstanding DMA input or output FF. If the PP word count is zero, the DMA input- or output-mode FF sets and the outstanding DMA FF clears. If the count is nonzero, the PP Word Counter decrements for every word taken from the channel until the count is zero. The DMA input- or output-mode FF clears when the transfer ends.

Output Data Bit 55 indicates a fast DMA transfer is occurring. Fast Transfer Mode sets when the PP Word Counter is loaded.

PP WORD COUNTER

This counter decrements during DMA functions when the PP transfers a number of words before the DMA transfer begins. Output Data Bits 56 through 63 specify the number of words. The counter decrements every time a word transfers.

OPERATIONAL STATUS NETWORK

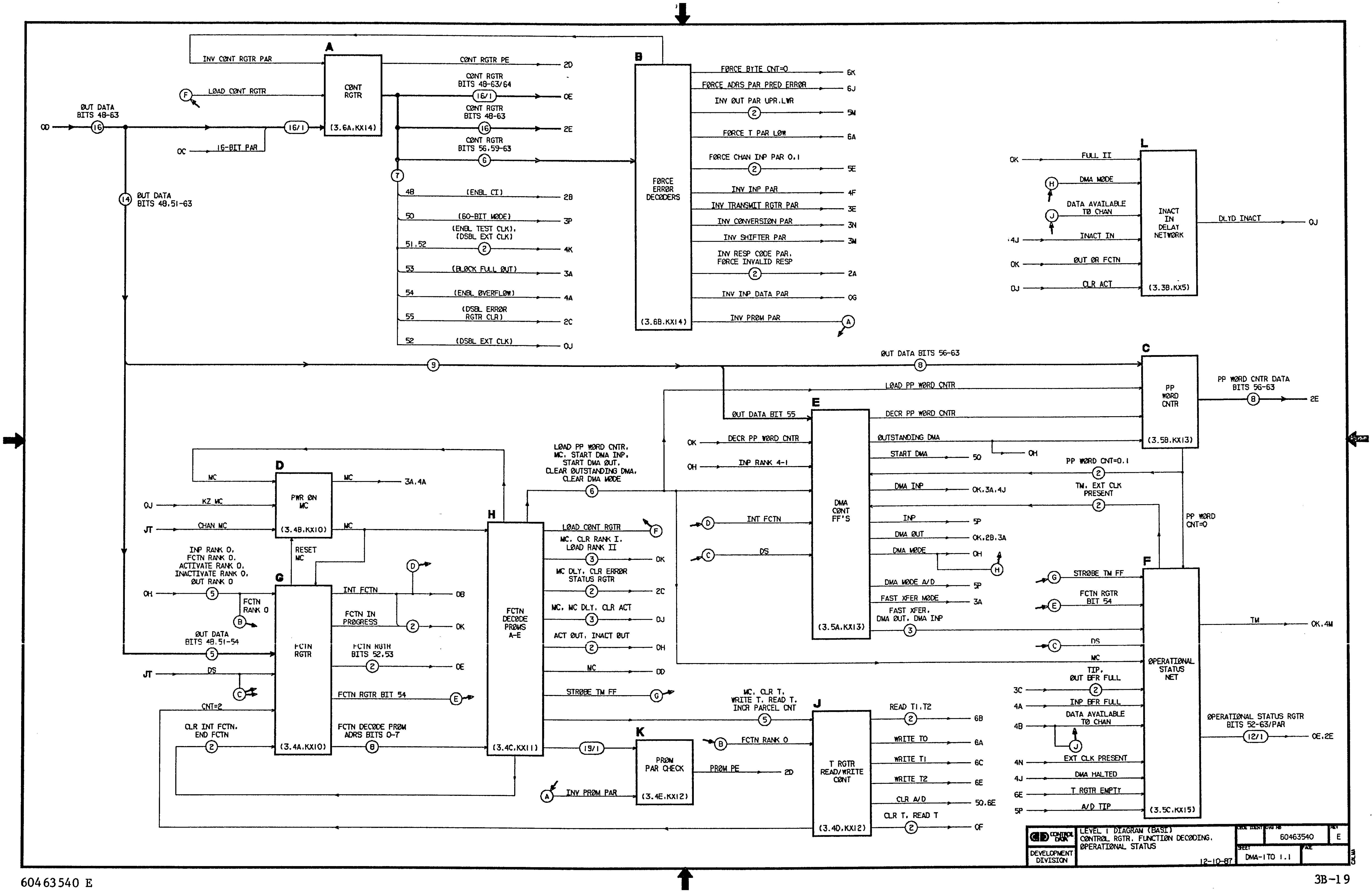
This register provides information regarding the state of the adapter during DMA transfers. All status bits are latched by Deadstart and unlatched by Master Clear.

CONTROL REGISTER

This register selects the different operating modes for the adapter. Output Data Bits 48 through 63 specify the operating modes.

FORCE ERROR DECODERS

When Output Data Bit 56 is set, Bits 59 through 63 are decoded to enable testing the parity networks.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (BASI)
CØNTRØL RGTR, FUNCTIØN DECØDING,
ØPERATIØNAL STATUS

12-10-87

CODE IDENT
DWG NO 60463540
REV E
SHEET DMA-1TO 1.1
PAGE

CALMA

This diagram shows error summing for the adapter and the interface to MAC.

CM RESPONSE CODE TRANSLATOR

This translator checks the response code from CM for errors. If any errors occurred, the appropriate signals go to the Error Status Register.

CM FUNCTION CODE

This circuit generates a function code for CM during DMA transfers. Only two functions are possible. They are CM read (DMA output) and CM write (DMA input).

ERROR STATUS NETWORK

This network monitors the parity checkers in BASI for errors. If an error occurs, an LED lights and the KX Error goes to the Error Status Register. This network also monitors EXTI (KZ board) and A/D (JY board) for errors. Any adapter error sets the appropriate Channel Error in the FS2 Register in MRB.

ERROR STATUS REGISTER

This register monitors the adapter´s error checking circuits. The PP uses this error status for fault isolation. Error Flag sets when one or more errors occur. This is the last register cleared by a master clear.

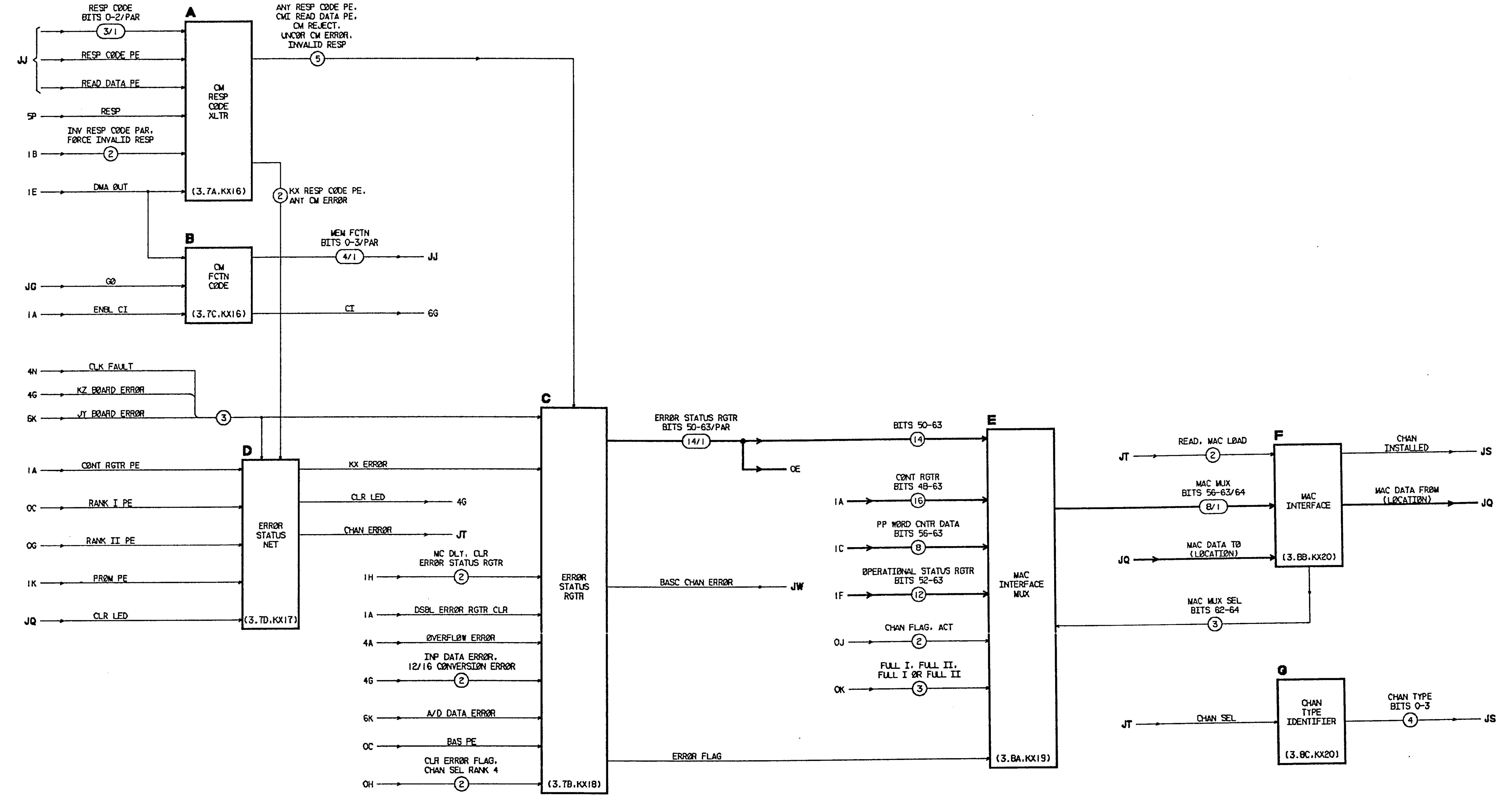
MAC INTERFACE MUX, MAC INTERFACE

MAC reads the adapter´s status through the MAC Interface Mux and a shift register in the MAC Interface as follows.

1. MAC sends 5-bit serial string to MAC Interface on MAC Data To line.
2. Shift register in MAC Interface shifts 5-bit string into bit positions 60 through 64. (Bits 60 and 61 are not used.)
3. MAC Interface sends MAC Mux Select Bits 62 through 64 from shift register to MAC Interface Mux.
4. MAC Interface Mux sends selected 8-bit status byte to MAC Interface.
5. MAC Load from MRB loads entire status byte into shift register.
6. Read from MRB enables serial status byte (shifted through shift register) to MAC on MAC Data From line.

CHANNEL TYPE IDENTIFIER

This circuit identifies what type of channel is installed. The channel type goes to the options installed register in MRA.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (BASI)
ERROR STATUS.
MAC INTERFACE

11-06-86

CODE IDENT | DWG NO 60463540 | REV C
SHEET DMA-1TO 1.2 | PAGE

This diagram shows the output control and data paths to the external device. The 12/16 conversion network is shown here but is used for both DMA input and output transfers.

OUTPUT CONTROL LOGIC

This circuit controls the data flow from the adapter to the external device. The following text describe the output signals.

- Busy - Controls data flow between the A/D and EXTI.
- Send Data - Enables data from the Disassembly Buffer (1.5J) to the Output Resynchronize Buffer.
- Full IIA - Indicates Transmit Register is full during PP output transfer.
- Transmit - Sets when Transmit Register receives data and clears when the data goes to the external device. This pulse is triggered by an empty in from the external device. In fast transfer mode, this signal remains set until ESM-II sends an empty in to terminate the transfer.

OUTPUT BUFFER ADDRESS COUNTERS

These counters provide write and read addresses for the 4-word Output Resynchronize Buffer. The write address decrements when a word enters the buffer. The read address decrements when a word leaves the buffer.

OUTPUT RESYNCHRONIZE NETWORK

This network determines whether the Output Resynchronize Buffer contains valid data. Each buffer location has a buffer full register located in this network. If the write address points to a location that is already full, Output Buffer Full disables Send Data which disables writing the buffer. If the read address points to a location that is not full, the absence of Stage Full disables Transmit which disables the Transmit Register. If full, the Transmit Register sends the word to the external device and the buffer full register clears. Each buffer full register has a delayed output which is used for resynchronization.

OUTPUT RESYNCHRONIZE BUFFER

This 4-word RAM receives 12-bit Conversion Data from the 12/16 Conversion Shifter. This buffer sends the data to the external device through the Transmit Register.

TRANSMIT REGISTER

This register is a pass on for DMA output transfers. For PP output transfers, Data Out loads data from Adapter Output Register Rank I (1.0D) into the Transmit Register.

TRANSMIT ENABLES

This circuit provides the proper pulse width for data transmission.

EMPTY, ACTIVE, INACTIVE OUTPUT NETWORKS

If the adapter is in fast transfer mode, this network sends Empty Out to the external device when the input buffer is half full. When not in fast transfer mode, this network sends Empty Out when the external device sends Full In and the input buffer is not full. Active Out and Inactive Out pass through a resynchronization network before being sent to the external device.

12/16 CONVERTER INPUT

This circuit selects DMA Output Data or Input Data for conversion. The R Register holds the remainder (or residue) from a word until the next word arrives. A parity generator produces a parity bit for each 4-bit parcel in the R Register.

12/16 CONVERSION SHIFTER

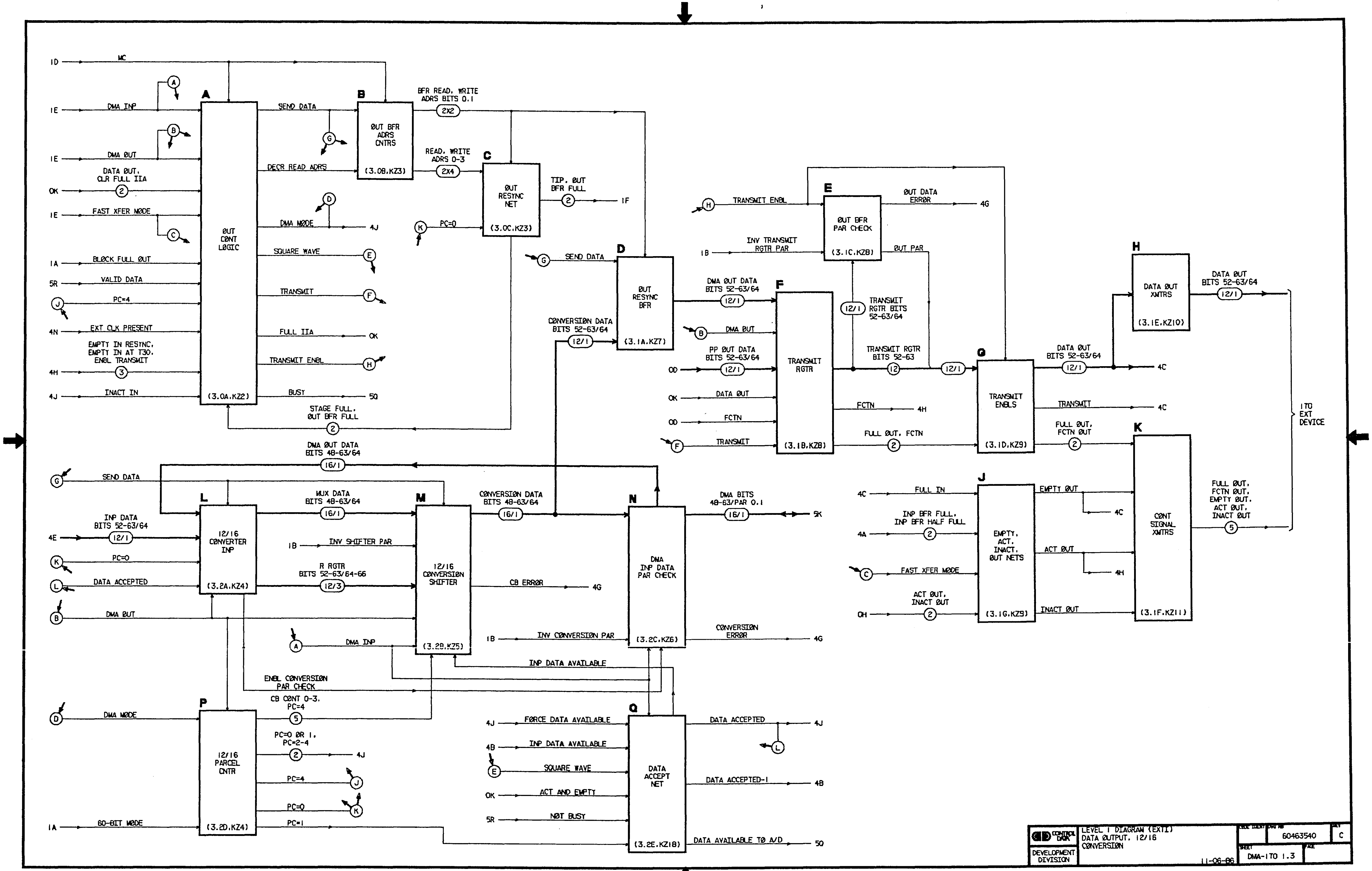
This macrocell converts 12-bit channel words to 16-bit CM parcels (DMA input) or 16-bit parcels to 12-bit words (DMA output). DMA input data goes to the Assembly Buffer (1.5C). DMA output data goes to the Output Resynchronize Buffer.

12/16 PARCEL COUNTER

This counter controls the 12/16 Conversion Shifter by counting 4-bit parcels. It counts from 0 through 4 (60-bit mode) or 1 through 4 (64-bit mode). This determines where the conversion is in its cycle.

DATA ACCEPT NETWORK

This network controls input data flow from the external device. It determines when a valid channel word is in the Input Resynchronize Buffer.



CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (EXTI)
DATA ØUTPUT, 12/16
CØNVERSIØN

11-06-86

60463540

C

DMA-ITO 1.3

DATA INPUT, ERROR SUMMING, CLOCK FORMATION (DMA-170 1.4)

This diagram shows the input control and data paths from the external device. The error summing, end transfer, and clock formation networks are also shown.

INPUT BUFFER WRITE, READ CONTROL

These circuits contain the write and read address counters for the 8-word Input Resynchronize Buffer. When data goes into the buffer, the write address counter decrements. When data goes out of the buffer, the read address counter decrements. The read address follows the write address but cannot overrun it. Master clear initially sets the counters to 7. The counters then decrement circularly from 7 to 0.

Input Buffer Write Control contains a full register for each buffer location. This register determines whether the associated location contains valid data. If the write address points to a location that is already full, an Overflow Error occurs. When a word is read from the buffer, the corresponding buffer full register is cleared. Each buffer full register has a delayed output which is used for resynchronization.

INPUT RECEIVERS AND DESKEW REGISTER

This circuit selects one of two paths for the Input Resynchronize Buffer. The normal path is Data In from the external device. In test mode, the Data Out path from the Transmit Register (1.3F) is selected. The Deskew Register lines up the bits.

INPUT RESYNCHRONIZE BUFFER

This 8-word PROM receives data from the external device or from the Transmit Register during test mode. The buffer sends the 12-bit data to the 12/16 Converter Input (1.3L) or the External Input Data Mux (1.0A).

INPUT BUFFER DATA MERGE

This circuits ORs the two macrocells that comprise the Input Resynchronize Buffer.

ERROR SUMMING NETWORK

This network monitors the error checking circuits in EXTI. If an error occurs, an LED lights and the KZ Board Error goes to the Error Status Network (1.2D) and the Error Status Register (1.2C).

CONTROL IN RESYNCHRONIZER

This circuit resynchronizes signals from the external device with the internal clock.

END TRANSFER NETWORK

Inactive In from the external device terminates a DMA input transfer. This network delays Inactive In until all input data is converted to 16-bit CM parcels and sent to the Assembly Buffer (1.5C). If the final parcel contains less than 16 bits, Force Data Available causes the parcel to be ones-filled. The Assembly Buffer ones-fills the remainder of the 64-bit word before sending it to CM.

EXTERNAL CLOCK TUNING NETWORK

This network selects the 10-MHz External Clock (on the Active In line) from ESM-II or the internally-generated 10-MHz Fake External Clock. This network contains four tuning switches which select verious delays for the External Clock.

EXTERNAL CLOCK T1/T2 FORMATION

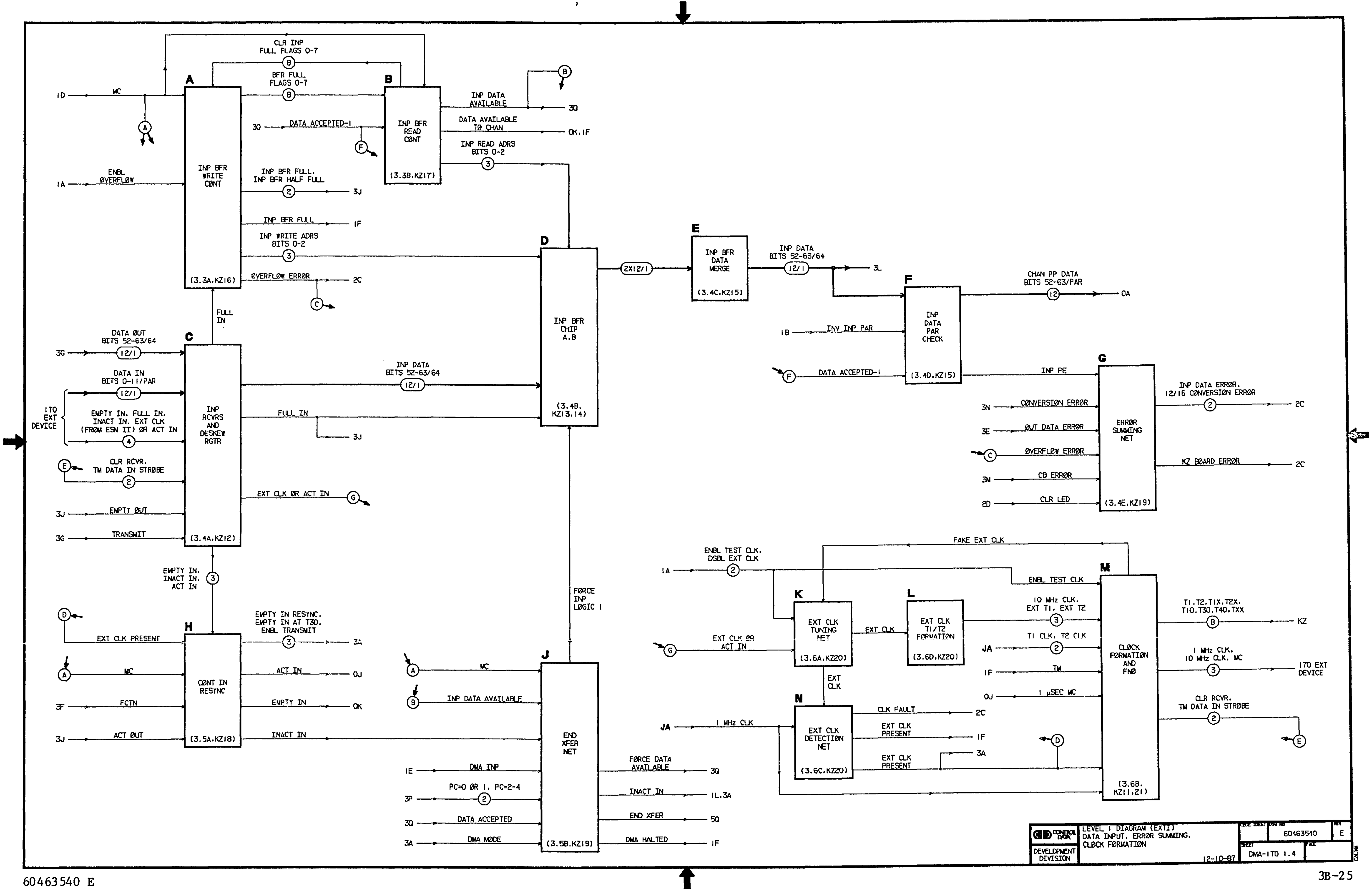
This circuit further delays External Clock and produces three clock signals which are sent to the Clock Formation and Fanout network.

EXTERNAL CLOCK DETECTION NETWORK

This network determines the presence or absence of the External Clock. It does this by counting the number of External Clock pulses received. If eight pulses are received every microsecond, the External Clock is present. If not, the clock is absent. A clock fault detector generates Clock Fault whenever the External Clock goes on or off. The External Clock can be initialized only at deadstart time.

CLOCK FORMATION AND FANOUT

This circuit generates the EXTI (KZ board) clocks. T1 and T2 are constant. T1X, T2X, T10, T30, T40, and TXX are different for normal and fast transfers. Refer to EXTI-170 3.6B for timing information.



CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM (EXTI)
DATA INPUT, ERROR SUMMING,
CLOCK FORMATION
12-10-87
CODE IDENT
DWG NO 60463540
REV E
SHEET DMA-1TO 1.4
PAGE
CALMA

This diagram shows the data paths from EXTI to CM through the Assembly Buffer and from CM to EXTI through the Disassembly Buffer.

ASSEMBLY

The adapter assembles 12-bit channel words into 60- or 64-bit CM words during DMA input transfers as follows.

1. External device sends channel words to input buffer (1.4D).
2. Conversion shifter (1.3L,M) converts 12-bit channel words to 16-bit CM word parcels. Residue from 12-bit channel word is saved until next channel word arrives. T register byte count (1.6A) decrements by two for every 16-bit CM word parcel.
3. Assembly Buffer assembles four 16-bit parcels into a 64-bit CM word.
4. Assembly Buffer Output Register sends 64-bit word to CM.
5. T register RMA (1.6C,F) increments by eight to set up next CM address.
6. DMA input transfer terminates when T register byte count equals zero or if the external device sends an inactive in (1.4C). If T equals zero, any residue from 12/16 conversion is saved for next transfer. If inactive is received, residue is assembled with ones fill and sent to CM.

DISASSEMBLY

The adapter disassembles 60- or 64-bit CM words into 12-bit channel words during DMA output transfers as follows.

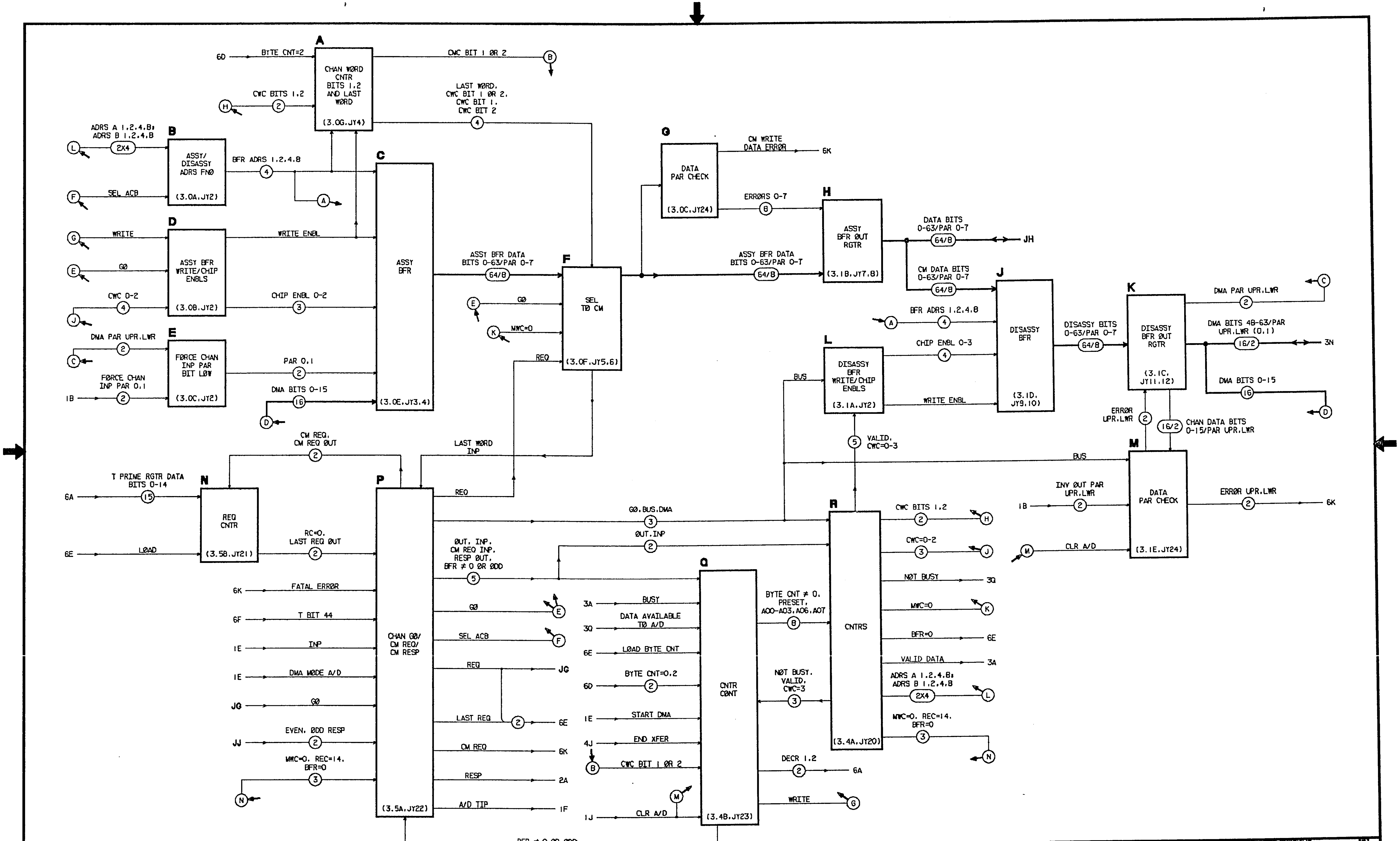
1. CM sends word to Disassembly Buffer.
2. T register RMA (1.6C,F) increments by eight to set up next CM address.
3. Disassembly Buffer Output Register sends disassembled 16-bit word parcels to conversion shifter (1.3L,M,N).
4. Conversion shifter converts 16-bit CM word parcels to 12-bit channel words. Residue from 16-bit parcels is saved for next 12-bit channel word. T register byte count (1.6A) decrements by two for every 16-bit word parcel.
5. Output buffer (1.3D) sends channel words to external device.
6. DMA output transfer terminates when T register byte count equals zero or if the external device sends an inactive in (1.4C). If T equals zero, any residue from 12/16 conversion is saved for next transfer.

COUNTERS

The Counters keep track of the number of 16-bit words that are being processed by the assembly/disassembly circuits.

CHANNEL GO/CM REQUEST/CM RESPONSE

These circuits coordinate the DMA assembly/disassembly operations with the CM requests and responses.



CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (A/D)
ASSEMBLY, DISASSEMBLY,
CONTROL COUNTERS

11-06-86

CODE IDENT

DWG NO 60463540

REV C

SHEET DMA-1TO 1.5

PAGE

This diagram shows the CM address path for DMA transfers and an Error Fan-In which detects JY board errors.

T REGISTER

The T Register receives the 16-bit byte count and the 32-bit real-memory address (RMA) from the T Prime Register. The least significant bit of the byte count, the most significant bit of RMA, and the three least significant bits of RMA are not used. These unused bits are always zero. The PP must load the T Register through the T Prime Register before a DMA transfer may proceed.

The 15-bit byte count decrements by two as every 16-bit word enters the Assembly Buffer (DMA input) or leaves the Disassembly Buffer (DMA output). The 28-bit RMA increments by eight after every CM reference.

The PP may read the 48-bit T register by issuing a read T function, activating the adapter, inputting three 16-bit words, and deactivating the adapter.

T PRIME REGISTER

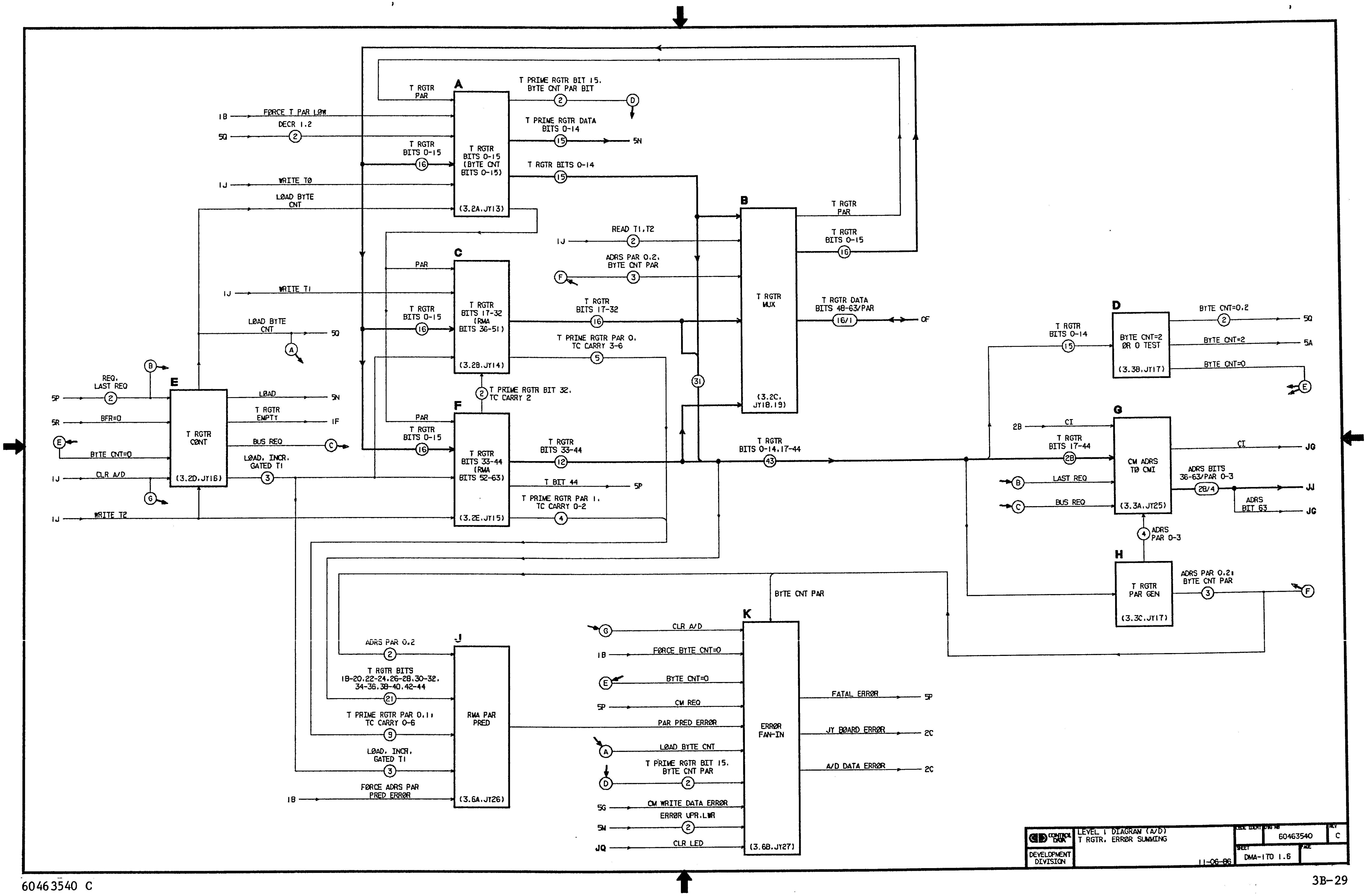
The T Prime Register receives the 16-bit byte count and the 32-bit RMA from the PP. When the T Register is empty (status bit 62), the PP may write the 48-bit T Prime Register by issuing a write T function, activating the adapter, outputting three 16-bit words, and deactivating the adapter. All three words must be written. The PP cannot read this register.

When the T Prime Register is full, the contents transfer to the T Register as follows.

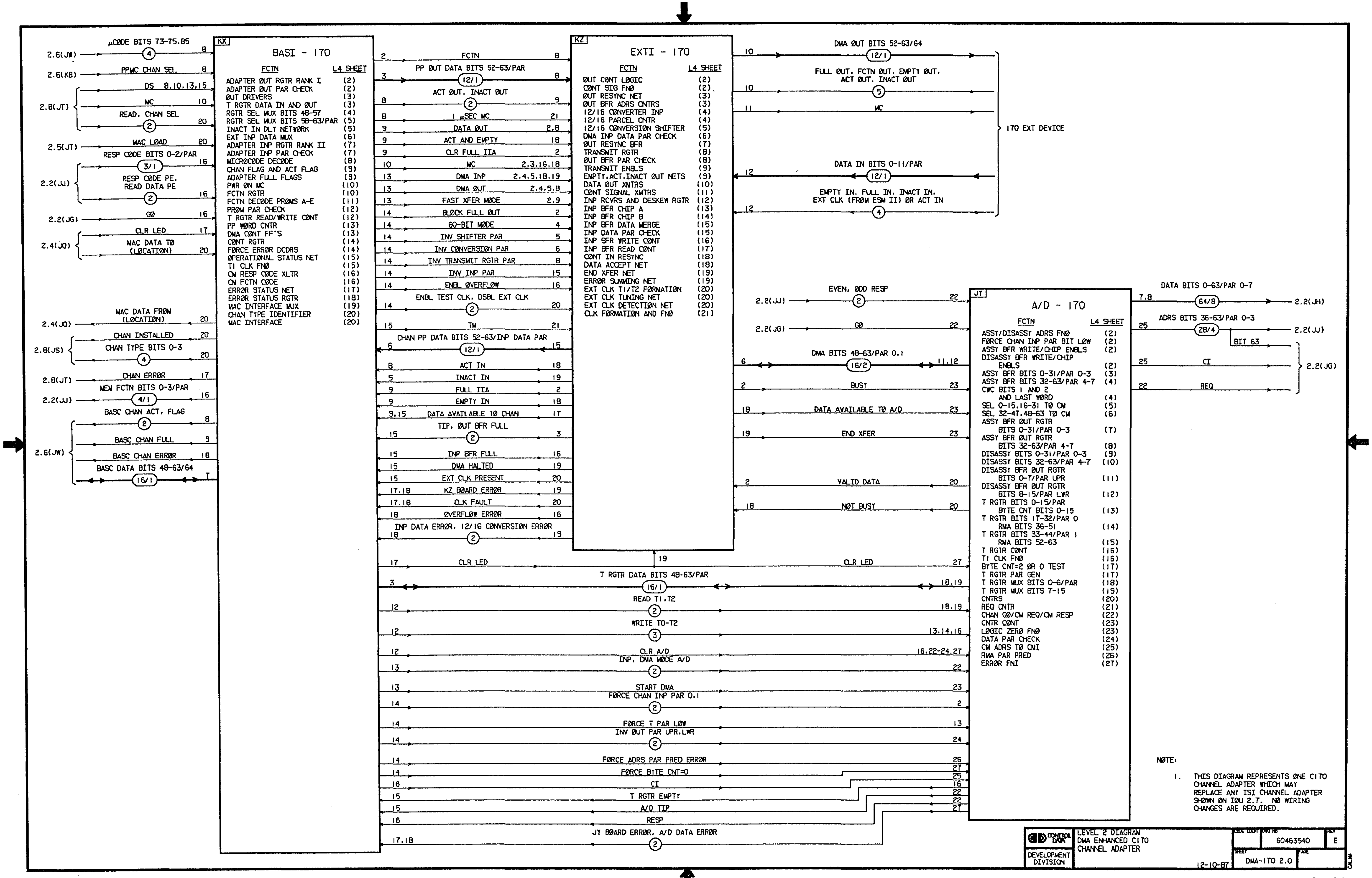
- If DMA transfer not in progress, T Register byte count equals zero, and assembly/disassembly buffers empty, all 48 bits transfer and status bit 62 sets.
- If DMA transfer in progress and T Register byte count equals zero, the 16-bit byte count transfers. During DMA output transfers, status bit 62 sets.
- If DMA transfer in progress and last CM reference occurs, the 32-bit RMA transfers. During DMA input transfers, status bit 62 sets.

CM ADDRESS TO CMI

This circuit sends the RMA from the T Register to CMI during a DMA transfer. The circuit also sends Cache Invalidate on every fourth and last CM write if bit 48 is set in the Control Register (1.1A).



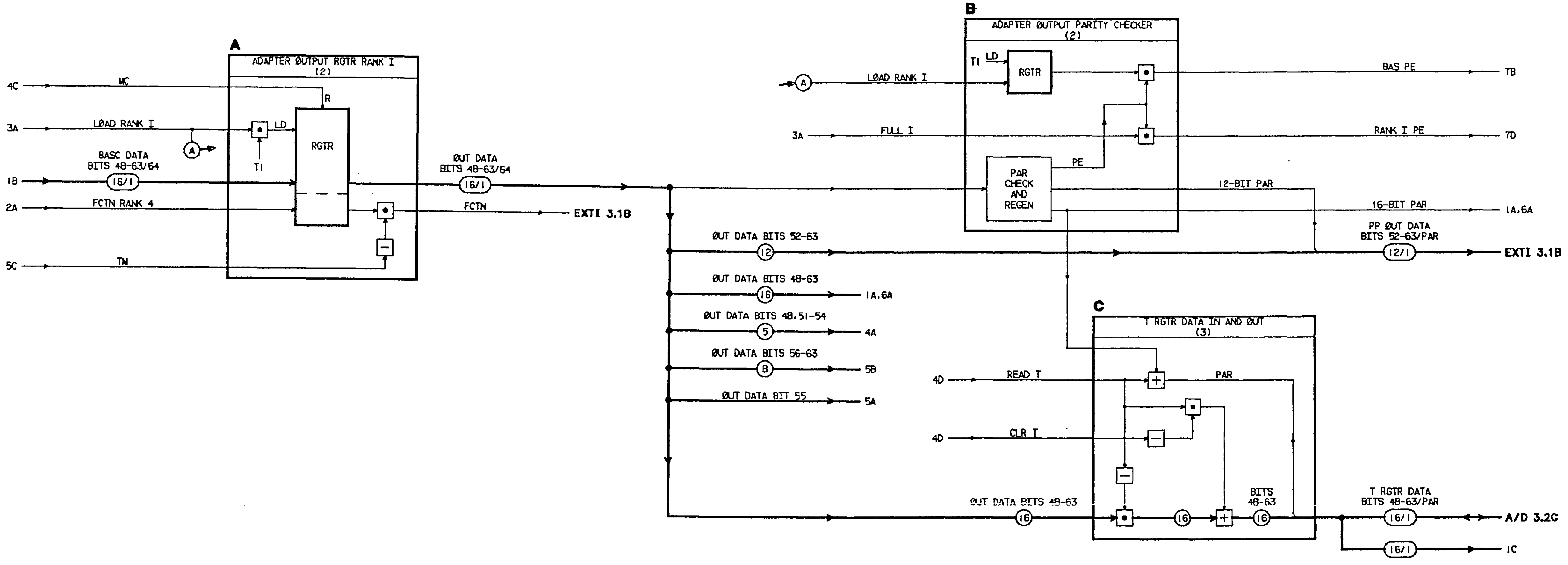
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM (A/D)
T RGTR. ERRØR SUMMING
11-06-86
CODE IDENT
DWG NO 60463540
REV C
SHEET DMA-1TO 1.6
PAGE



NOTE:

1. THIS DIAGRAM REPRESENTS ONE CITO CHANNEL ADAPTER WHICH MAY REPLACE ANY ISI CHANNEL ADAPTER SHOWN ON IOU 2.7. NO WIRING CHANGES ARE REQUIRED.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
DMA ENHANCED CITO
CHANNEL ADAPTER
DWG NO 60463540
REV E
SHEET DMA-1TO 2.0
12-10-87

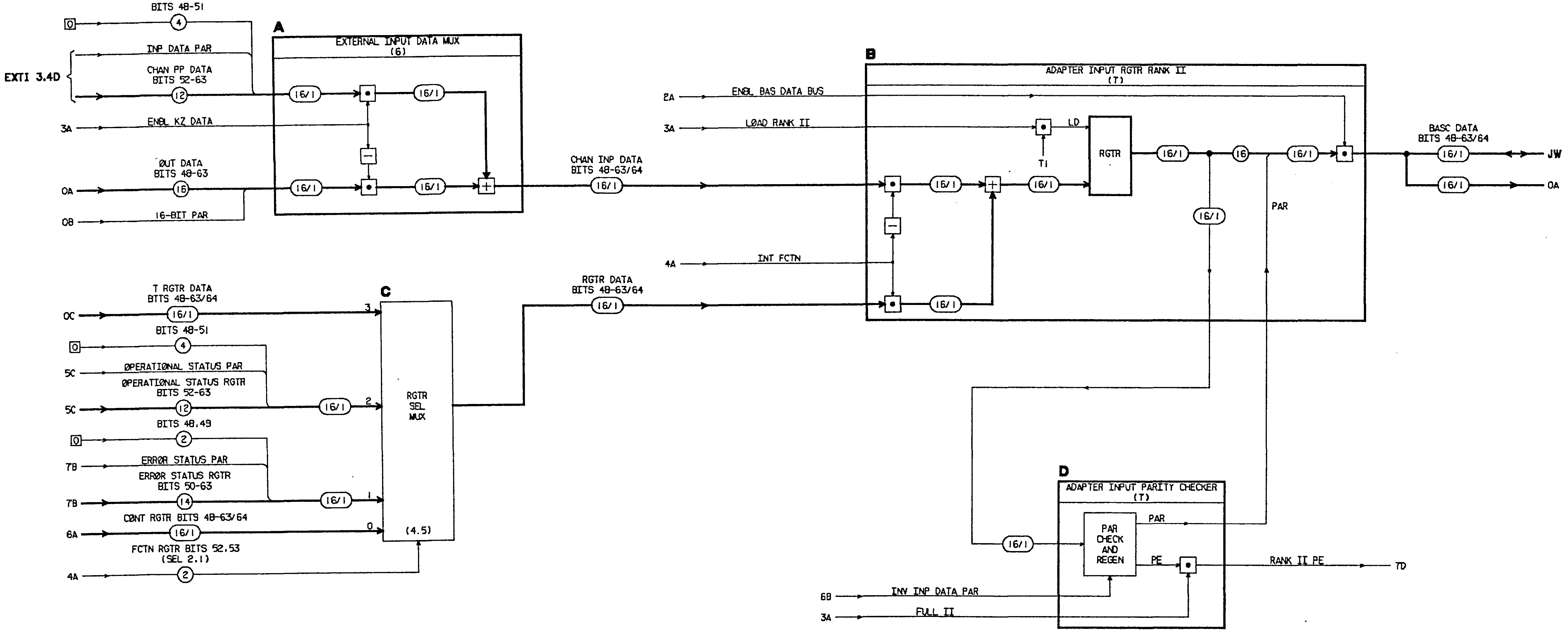


CONTROL DATA
DEVELOPMENT DIVISION

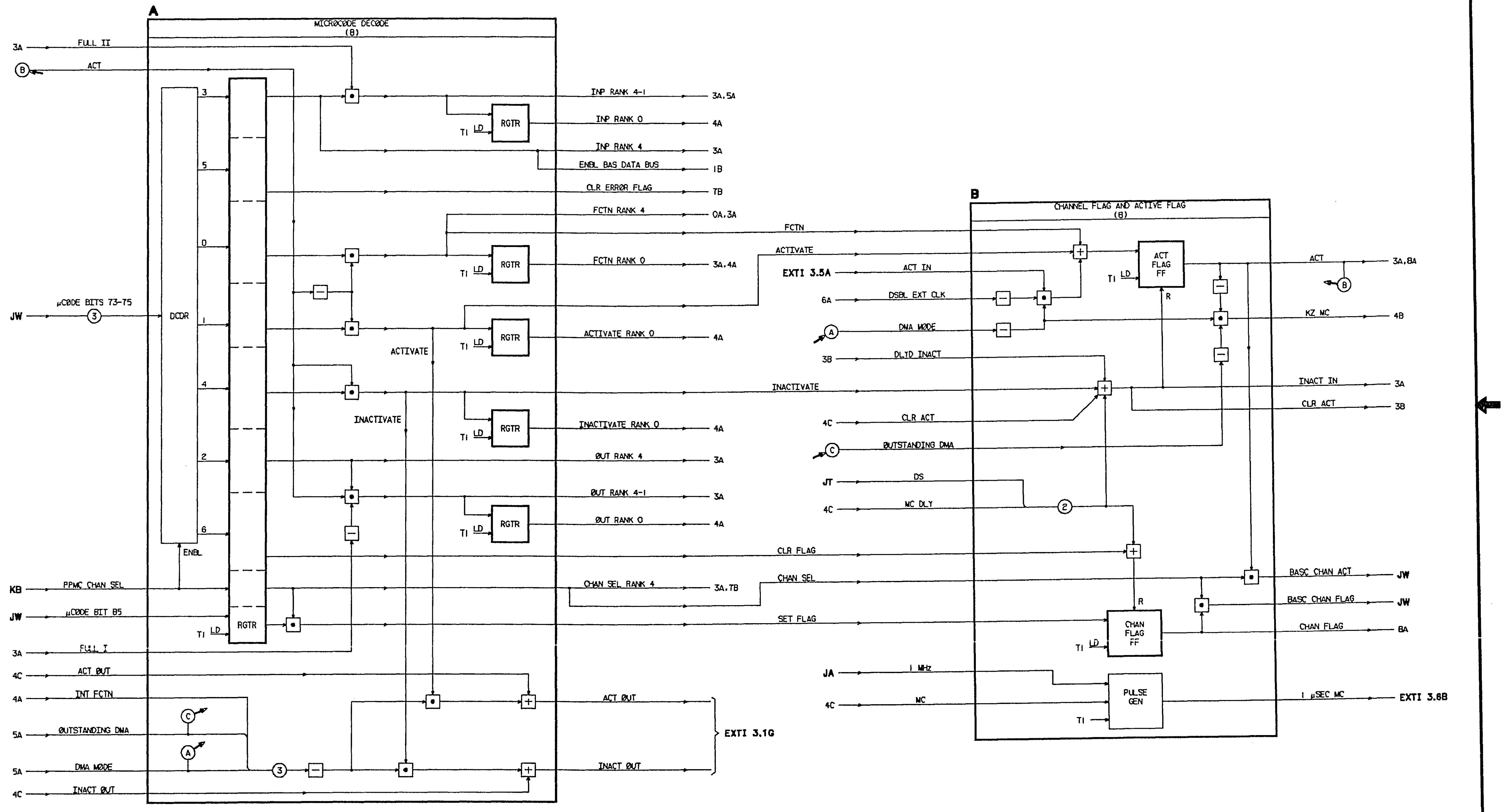
LEVEL 3 DIAGRAM (KX)
ADAPTER ØUTPUT RGTR.
T RGTR INPUT/ØUTPUT

11-06-86

CODE IDENT
DWG NO 60463540
REV C
SHEET BASI-170 3.0
PAGE



CONTROL DATA	LEVEL 3 DIAGRAM (KX) EXTERNAL INPUT DATA MUX. RGTR SELECT MUX. ADAPTER INPUT RGTR	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	11-06-86	SHEET BASI-170 3.1	PAGE	



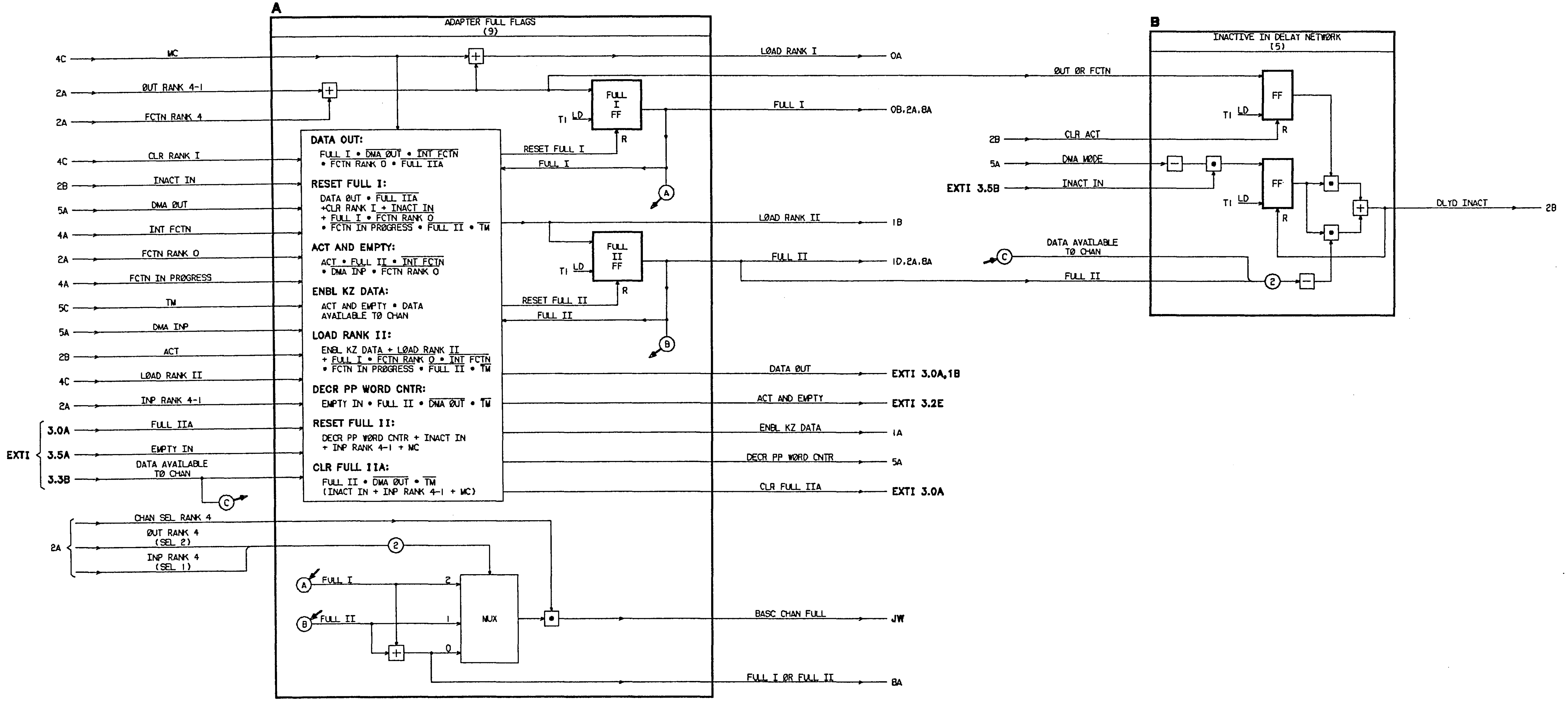
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (KX)
MICROCODE DECODE.
CHANNEL FLAG, ACTIVE FLAG
12-10-87

CODE IDENT	DWG NO	REV
	60463540	E

SHEET	PAGE
BASI-170 3.2	

CALMA



CONTROL DATA

DEVELOPMENT
DIVISION

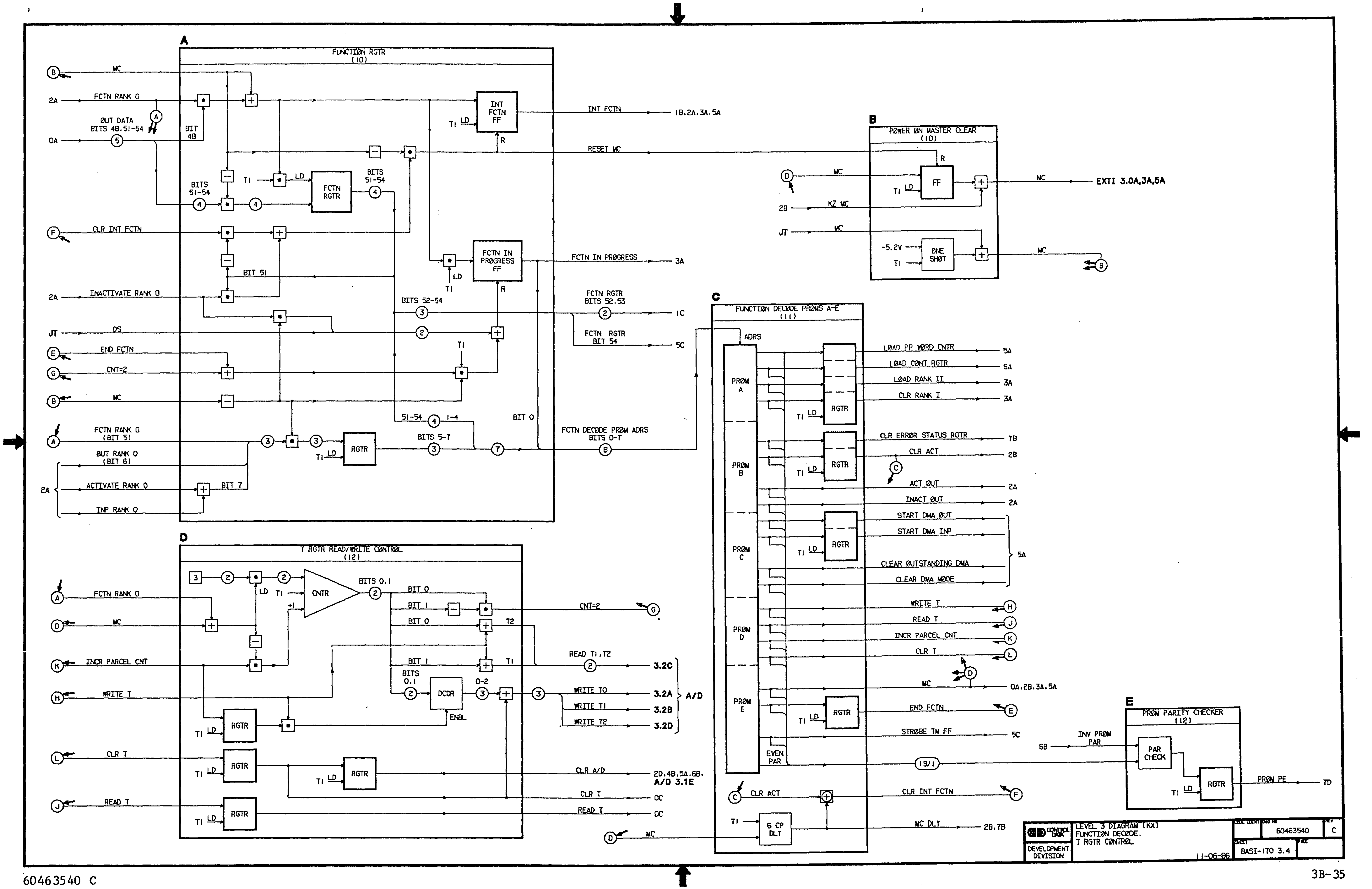
LEVEL 3 DIAGRAM (KX)
ADAPTER FULL FLAGS

12-10-87

CODE IDENT	DWG NO	REV
	60463540	E

SHEET	PAGE
BASI-170 3.3	

CALMA



CONTROL DATA

DEVELOPMENT DIVISION

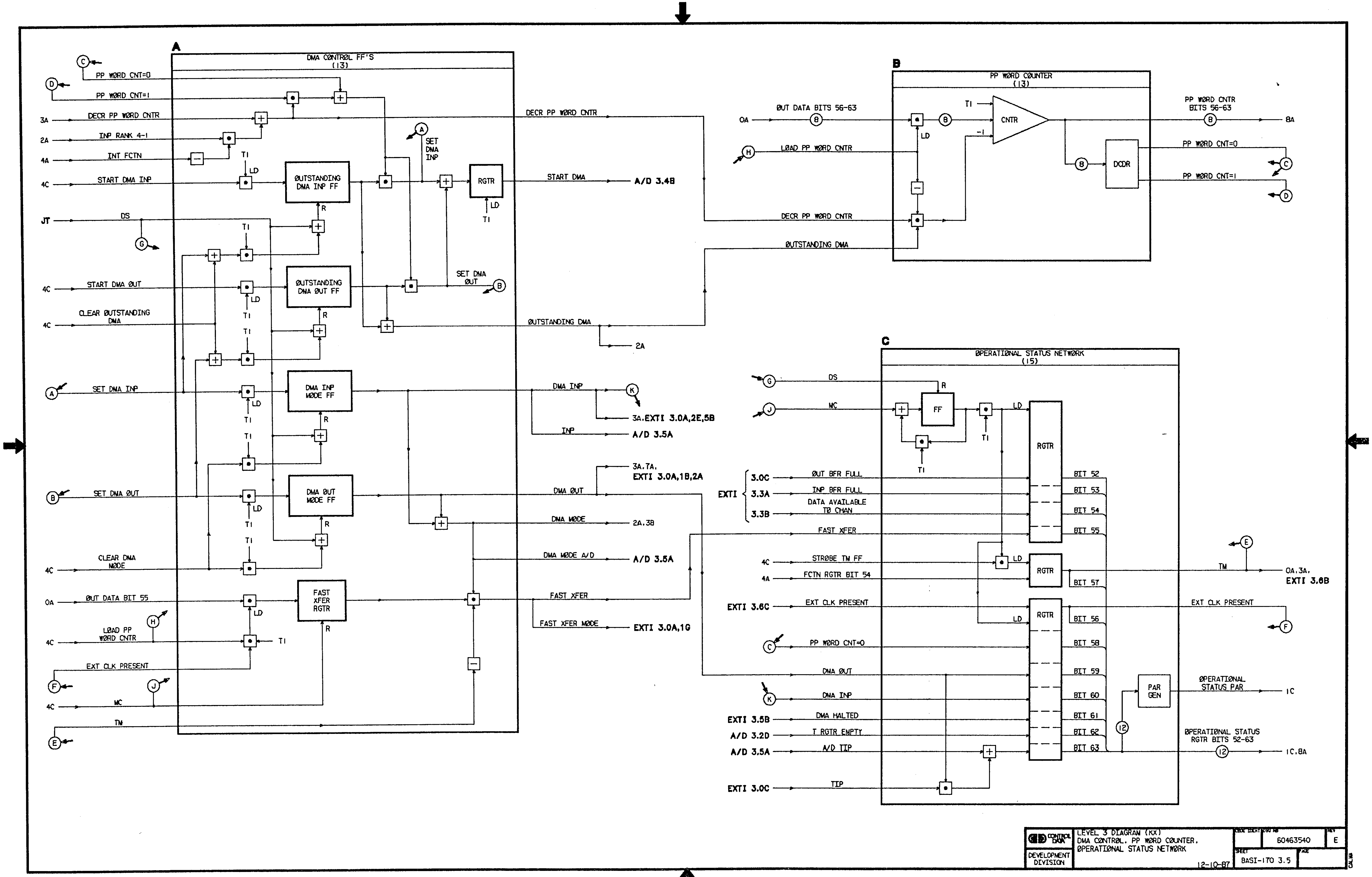
LEVEL 3 DIAGRAM (KX)
FUNCTION DECODE,
T RGTR CONTROL

11-06-86

60463540

C

BASI-170 3.4



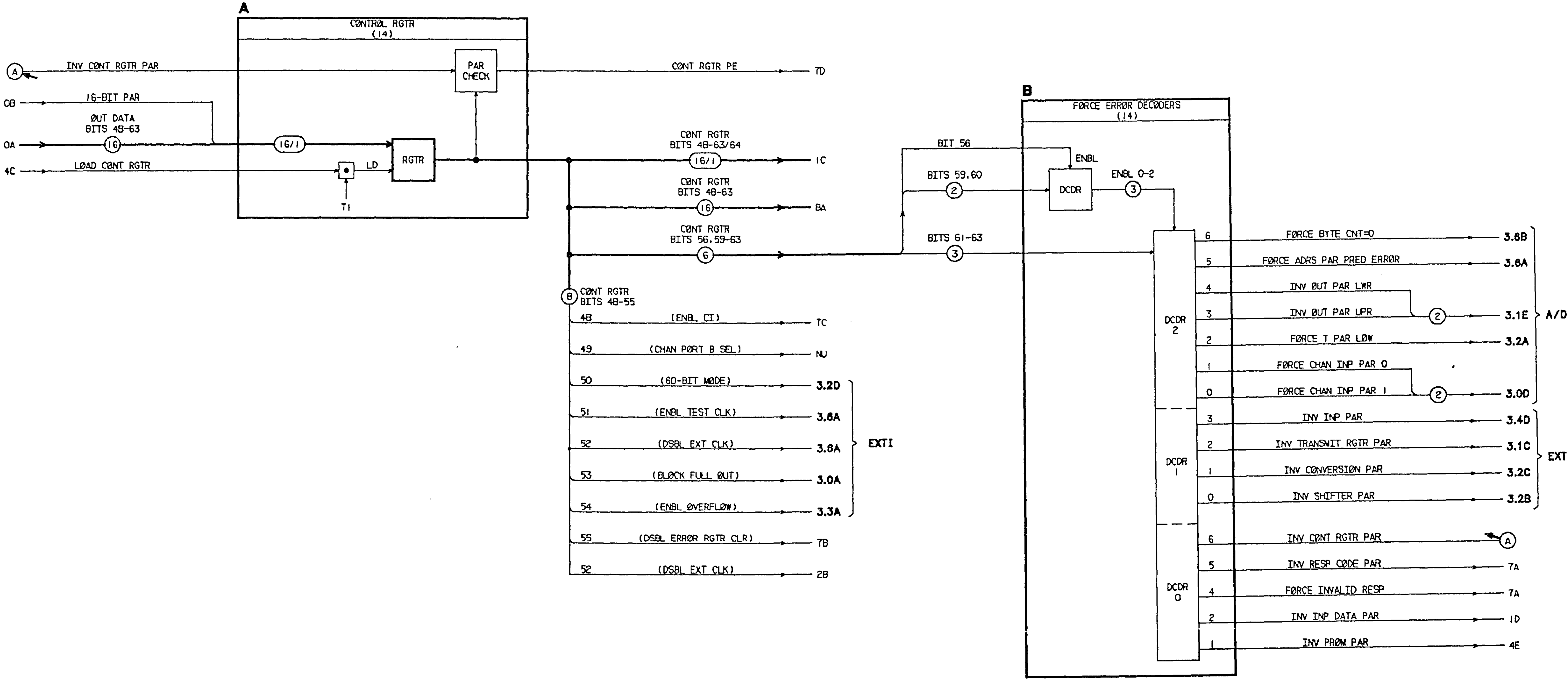
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (KX)
DMA CONTROL. PP WORD COUNTER.
OPERATIONAL STATUS NETWORK

12-10-87

CODE IDENT | DWG NO 60463540 | REV E

SHEET BASI-170 3.5 | PAGE



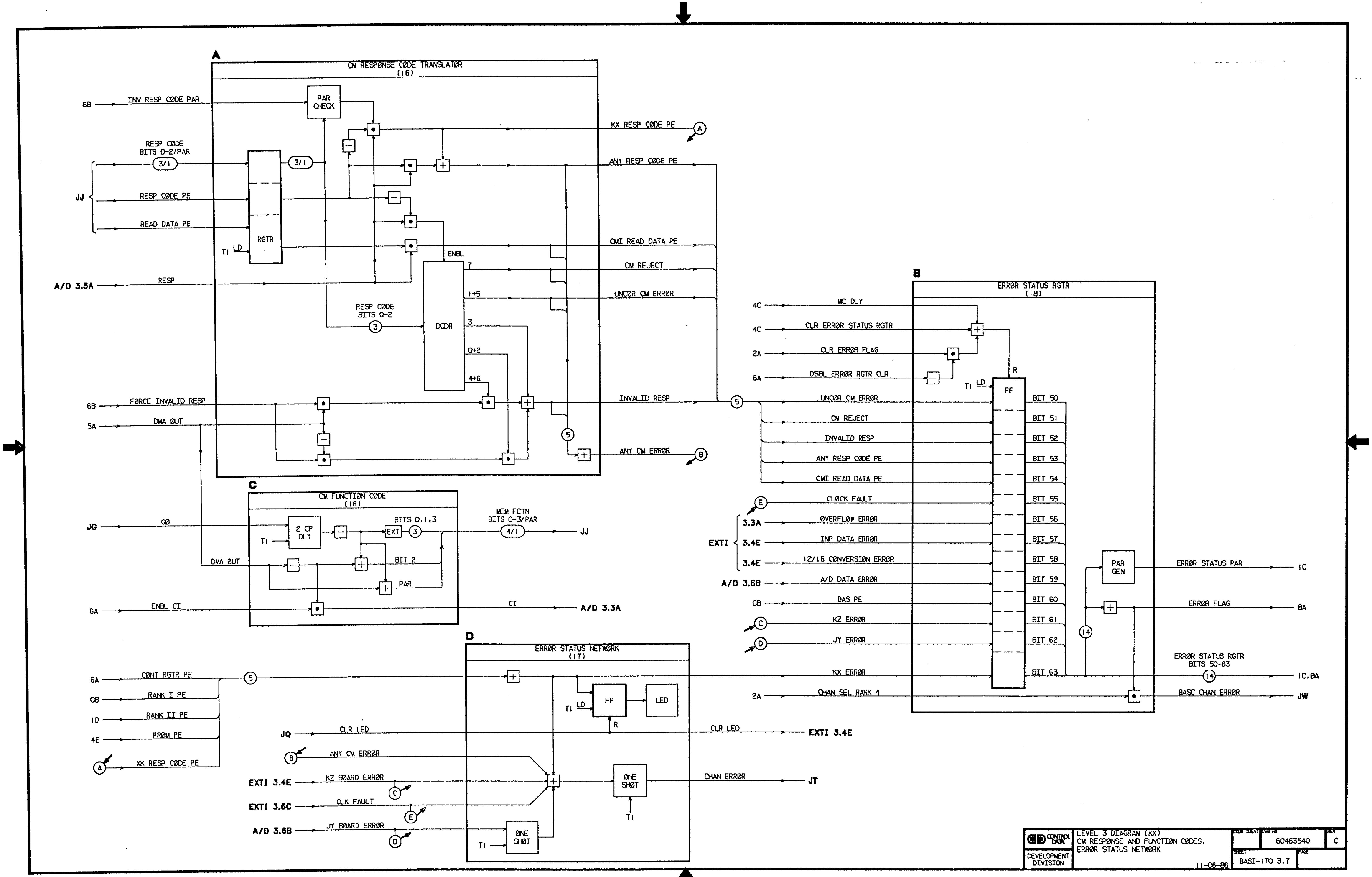
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (KX)
CONTROL RGTR.
FORCE ERROR DECODERS

11-06-86

CODE IDENT	DWG NO	REV
	60463540	C

SHEET	PAGE
BASI-170 3.6	



CONTROL DATA

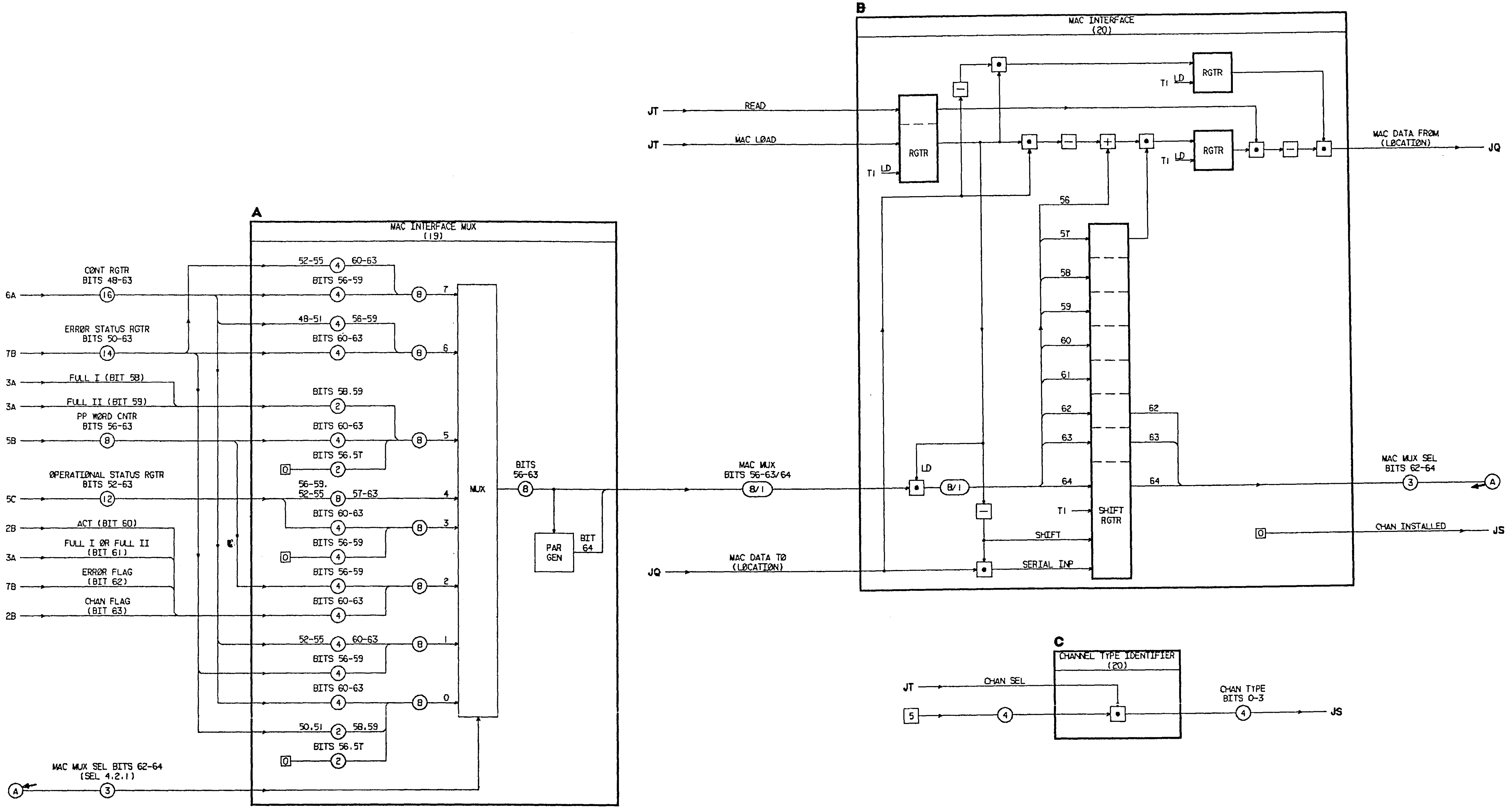
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (KX)
CM RESPONSE AND FUNCTION CODES.
ERROR STATUS NETWORK

11-06-86

CODE IDENT | DWG NO 60463540 | REV C

SHEET BASI-170 3.7 | PAGE

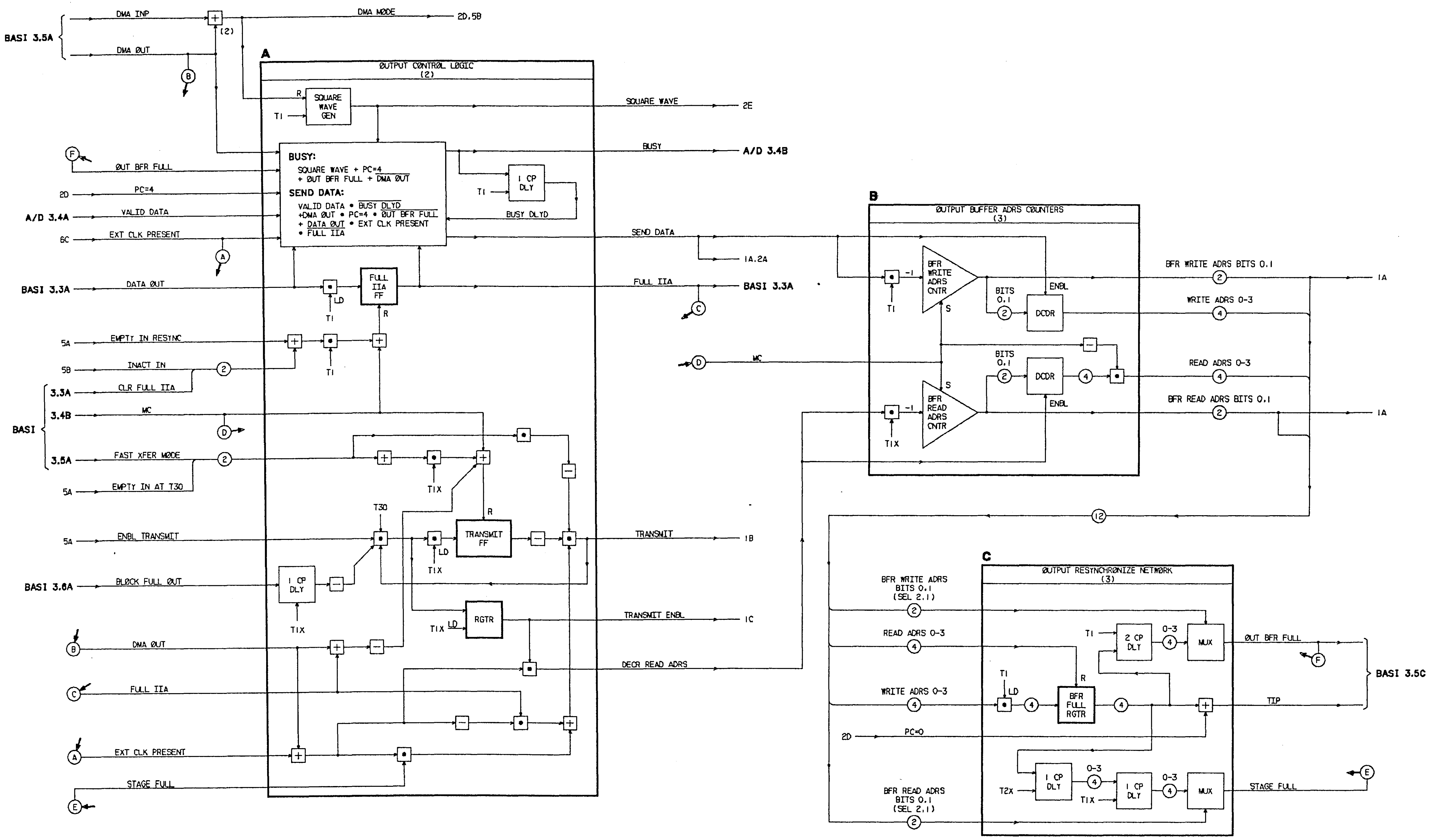


CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (KX)
MAC INTERFACE,
CHANNEL TYPE IDENTIFIER

11-06-86

60463540
C
BASI-1TO 3.8



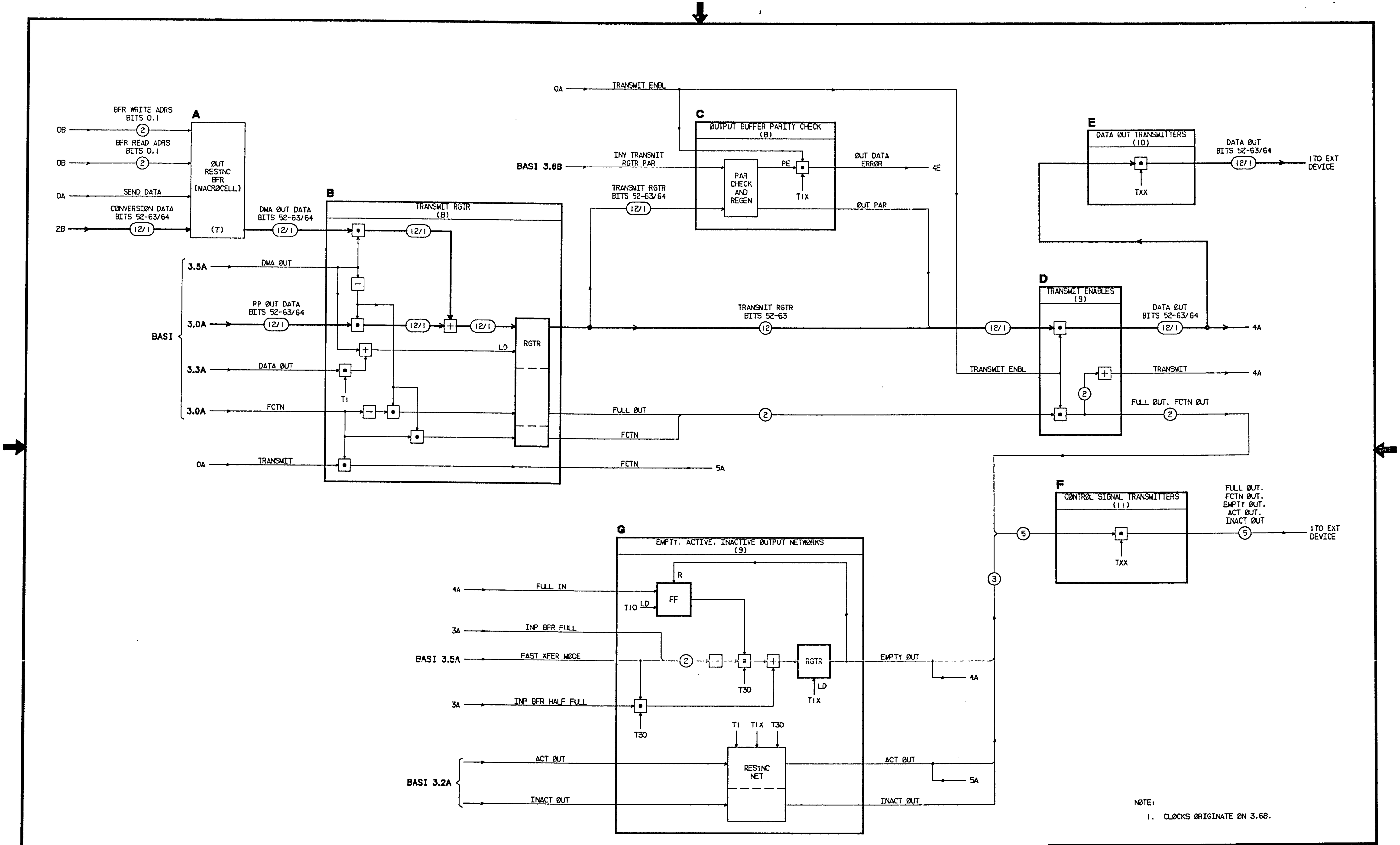
NOTE:

1. CLOCKS ORIGINATE ON 3.6B

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (KZ)
OUTPUT CONTROL, BUFFER ADRS
COUNTERS, RESYNCHRONIZE NETWORK
11-06-86

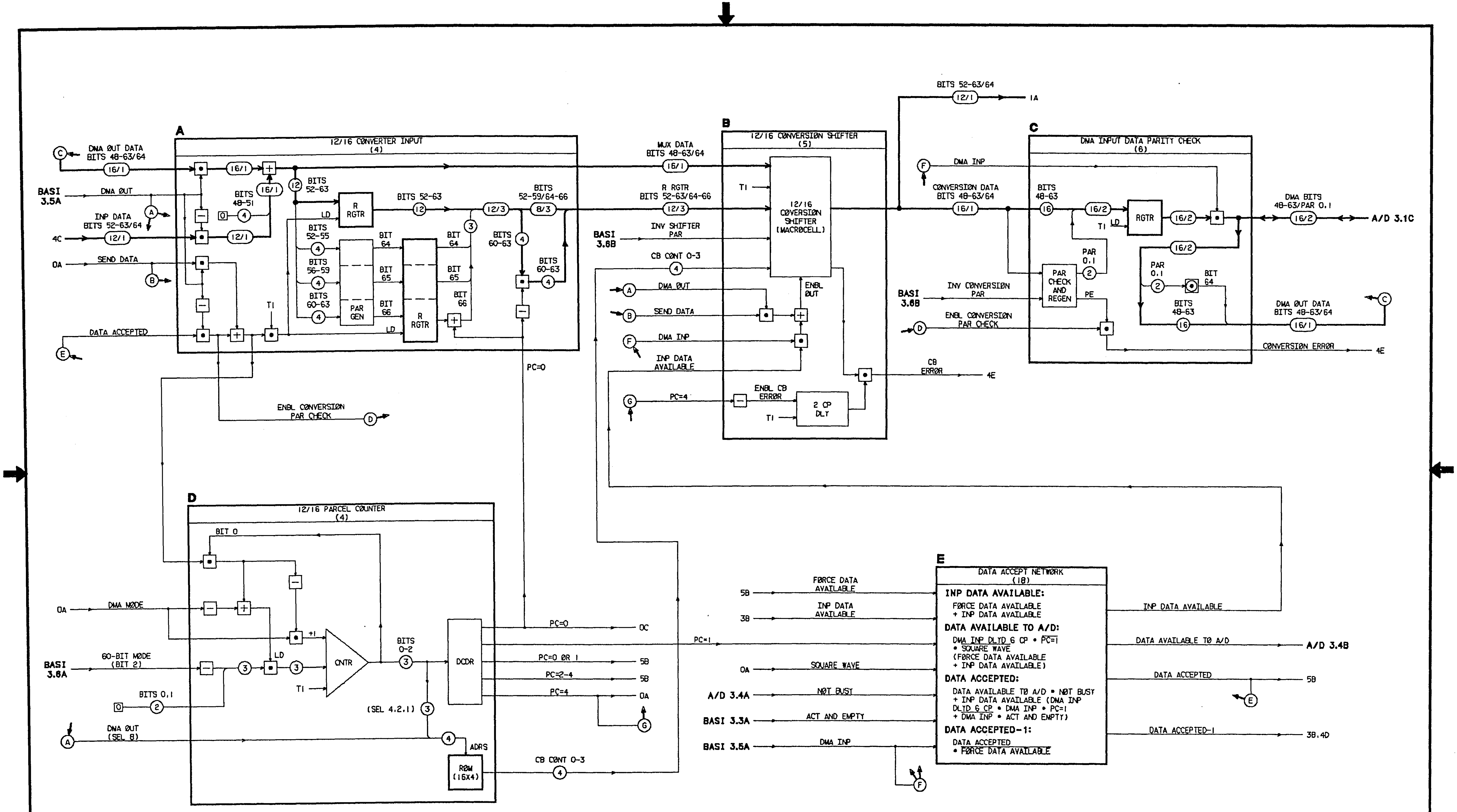
CODE IDENT | DWG NO 60463540 | REV C
SHEET EXTI-170 3.0 | PAGE



NOTE:

1. CLOCKS ORIGINATE ON 3.6B.

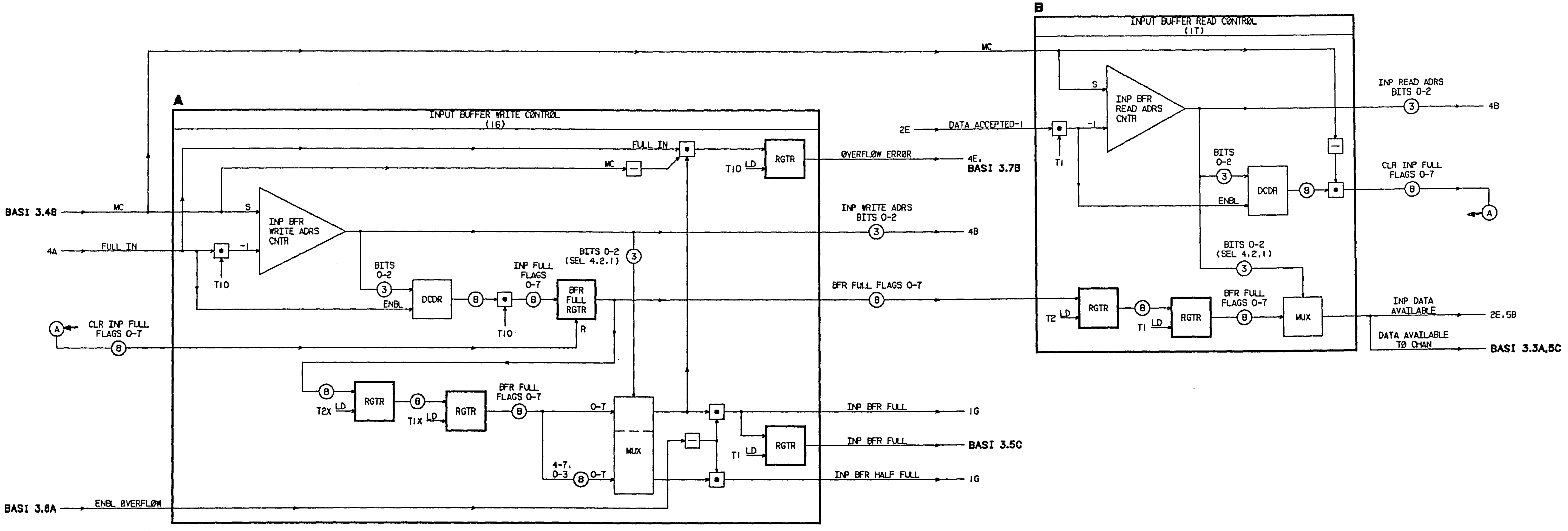
CD CONTROL DATA	LEVEL 3 DIAGRAM (KZ) OUTPUT DATA AND CONTROL	60463540	C
DEVELOPMENT DIVISION	11-06-86	EXTI-1TO 3.1	



NOTE:

1. CLOCKS ORIGINATE ON 3.6B.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (KZ)
INPUT DATA.
DATA ACCEPT NETWORK
12-10-87
CODE IDENT
DWG NO 60463540
REV E
SHEET EXTI-170 3.2
PAGE

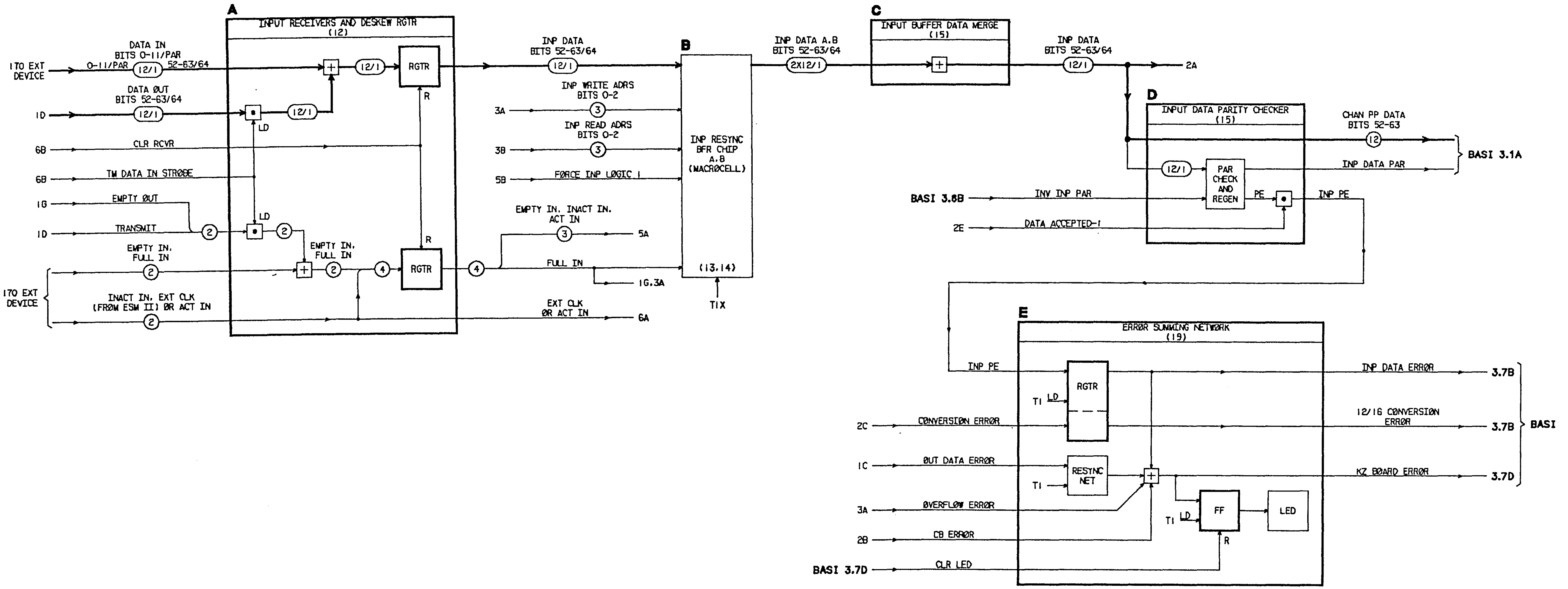


NOTE:

1. CLOCKS ORIGINATE ON 3.6B.

CONTROL DATA	LEVEL 3 DIAGRAM (KZ) INPUT BUFFER READ AND WRITE CONTROL	CODE IDENT	DWG NO 60463540	REV E
DEVELOPMENT DIVISION	12-10-87	SHEET EXTI-170 3.3	PAGE	

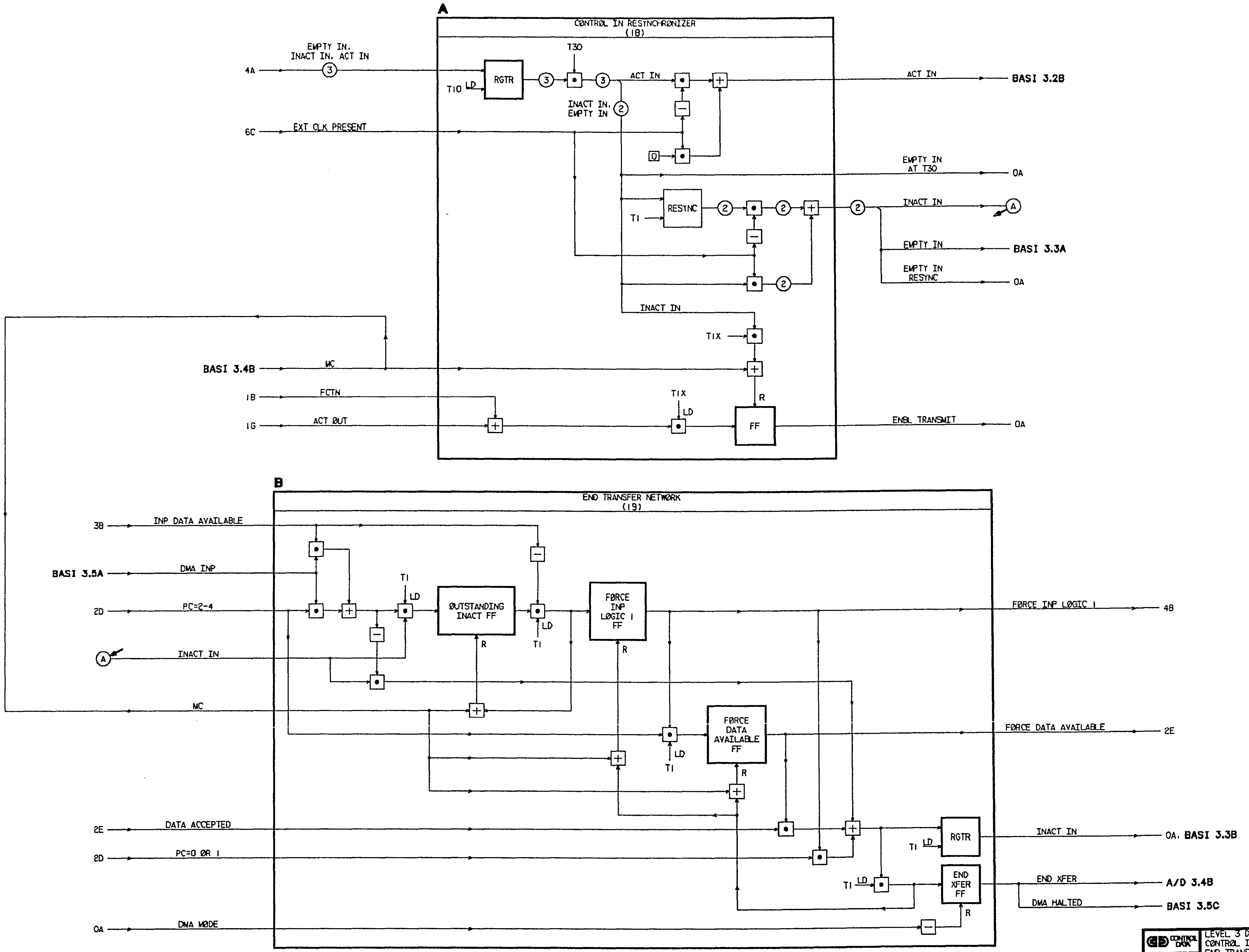
CALMA



NOTE:

1. CLOCKS ORIGINATE ON 3.6B.

CONTROL DATA	LEVEL 3 DIAGRAM (KZ) INPUT BUFFER. ERROR SUMMING NETWORK	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	11-06-86	SHEET EXTI-170 3.4	PAGE	



NOTE:

1. CLOCKS ORIGINATE ON 3.6B.

CONTROL DATA

DEVELOPMENT DIVISION

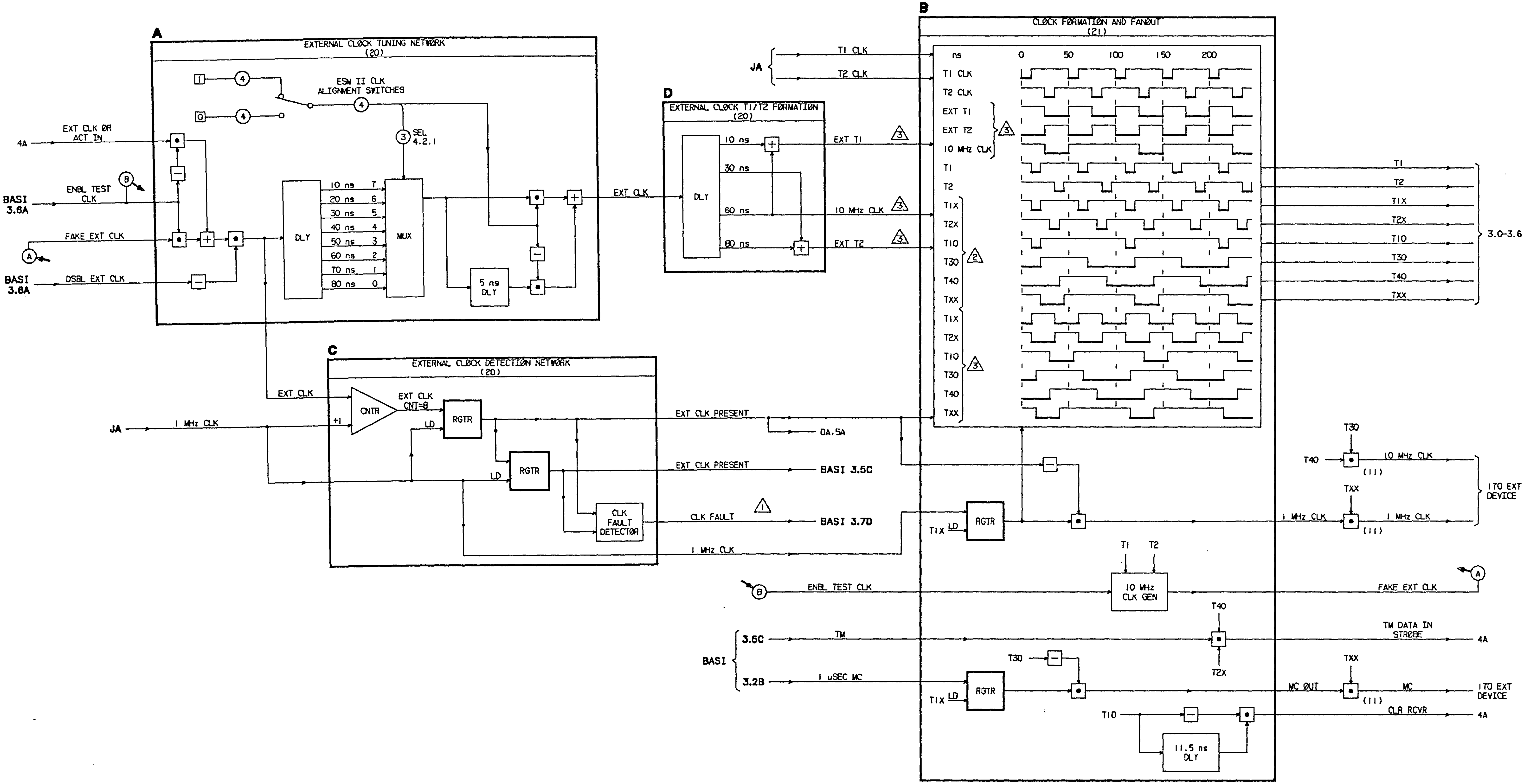
LEVEL 3 DIAGRAM (KZ)
CONTROL IN RESYNCHRONIZER.
END TRANSFER NETWORK

12-10-87

CODE IDENT | DWG NO 60463540 | REV E

SHEET EXTI-170 3.5 | PAGE

CALMA



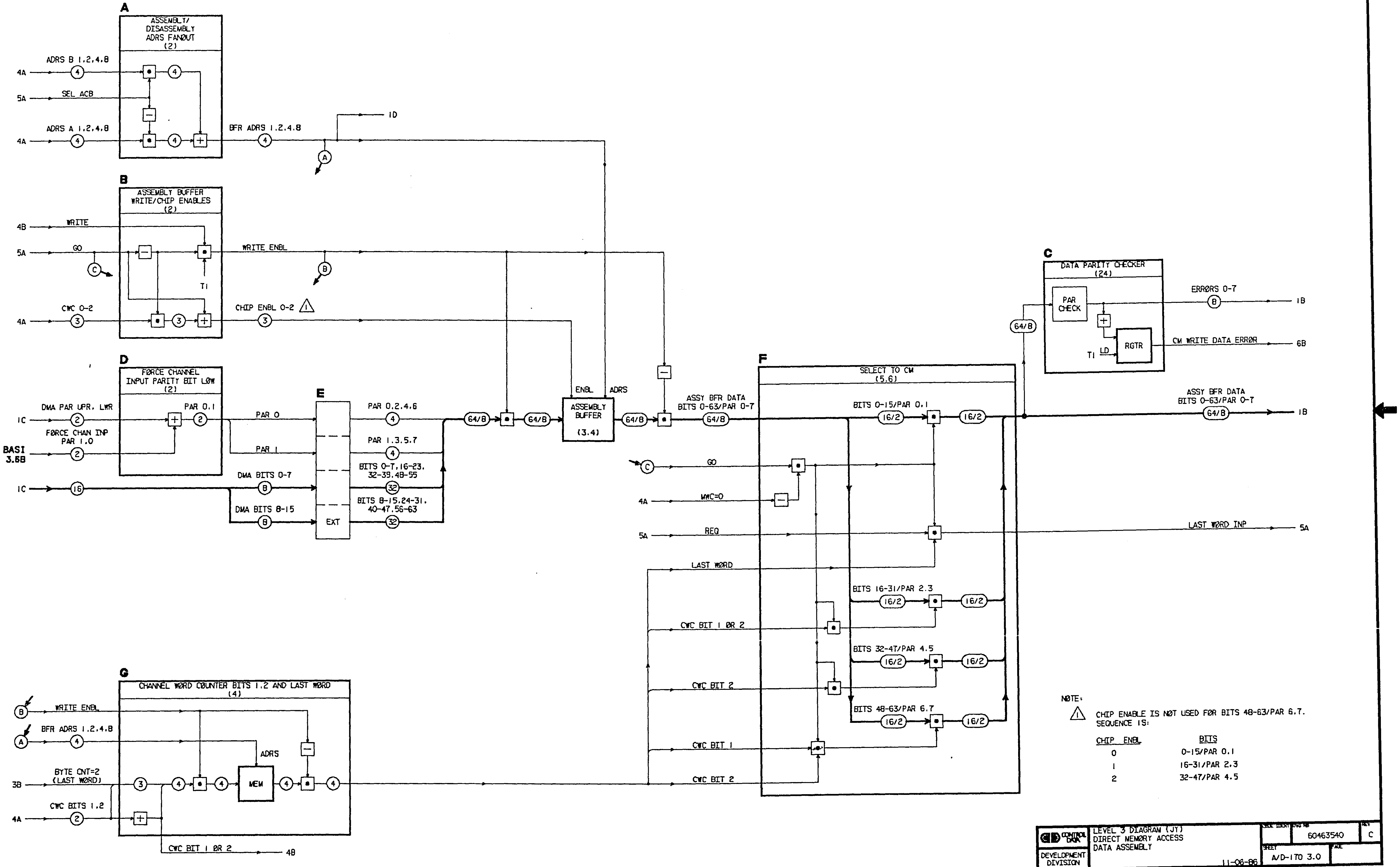
NOTES:

⚠1 CLOCK FAULT OCCURS WHEN EXTERNAL CLOCK GOES ON OR OFF DURING OPERATION. EXTERNAL CLOCK MAY BE INITIALIZED ONLY AT DEADSTART.

⚠2 THESE SIGNALS ARE PRESENT ONLY WHEN EXTERNAL CLOCK IS NOT PRESENT.

⚠3 THESE SIGNALS ARE PRESENT ONLY WHEN EXTERNAL CLOCK IS PRESENT. EXTERNAL CLOCK ENTERS ASYNCHRONOUSLY.

CONTROL DATA	LEVEL 3 DIAGRAM (KZ) CLOCK FORMATION	CODE IDENT	DWG NO 60463540	REV C
DEVELOPMENT DIVISION	11-06-86	SHEET EXTI-170 3.6	PAGE	

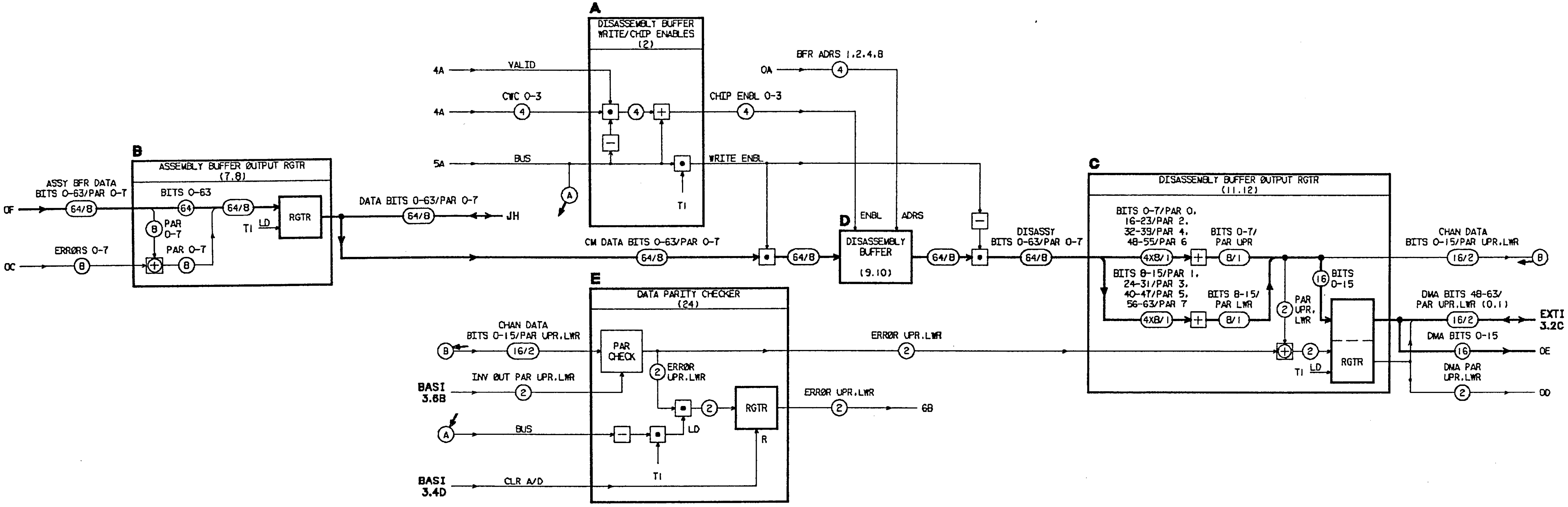


NØTE:

⚠1 CHIP ENABLE IS NØT USED FØR BITS 48-63/PAR 6.7. SEQUENCE IS:

CHIP ENBL	BITS
0	0-15/PAR 0.1
1	16-31/PAR 2.3
2	32-47/PAR 4.5

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JY)
DIRECT MEMØRY ACCESS
DATA ASSEMBLY
11-06-86
DWG NO 60463540
REV C
SHEET A/D-1TO 3.0



NØTE:

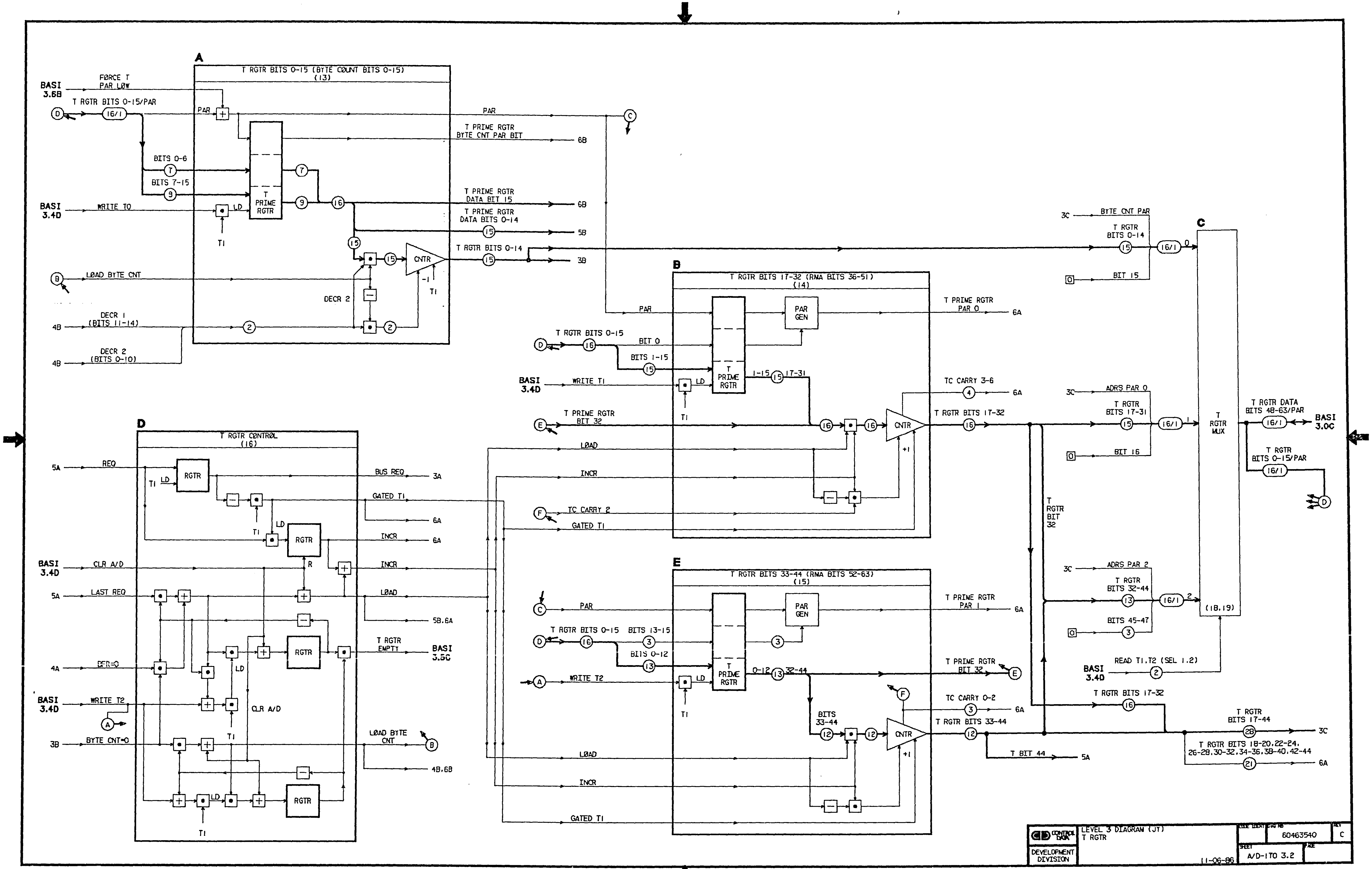
⚠ CHIP ENABLE SEQUENCE IS:

CHIP ENBL	BITS
0	0-15/PAR 0.1
1	16-31/PAR 2.3
2	32-47/PAR 4.5
3	48-63/PAR 6.7

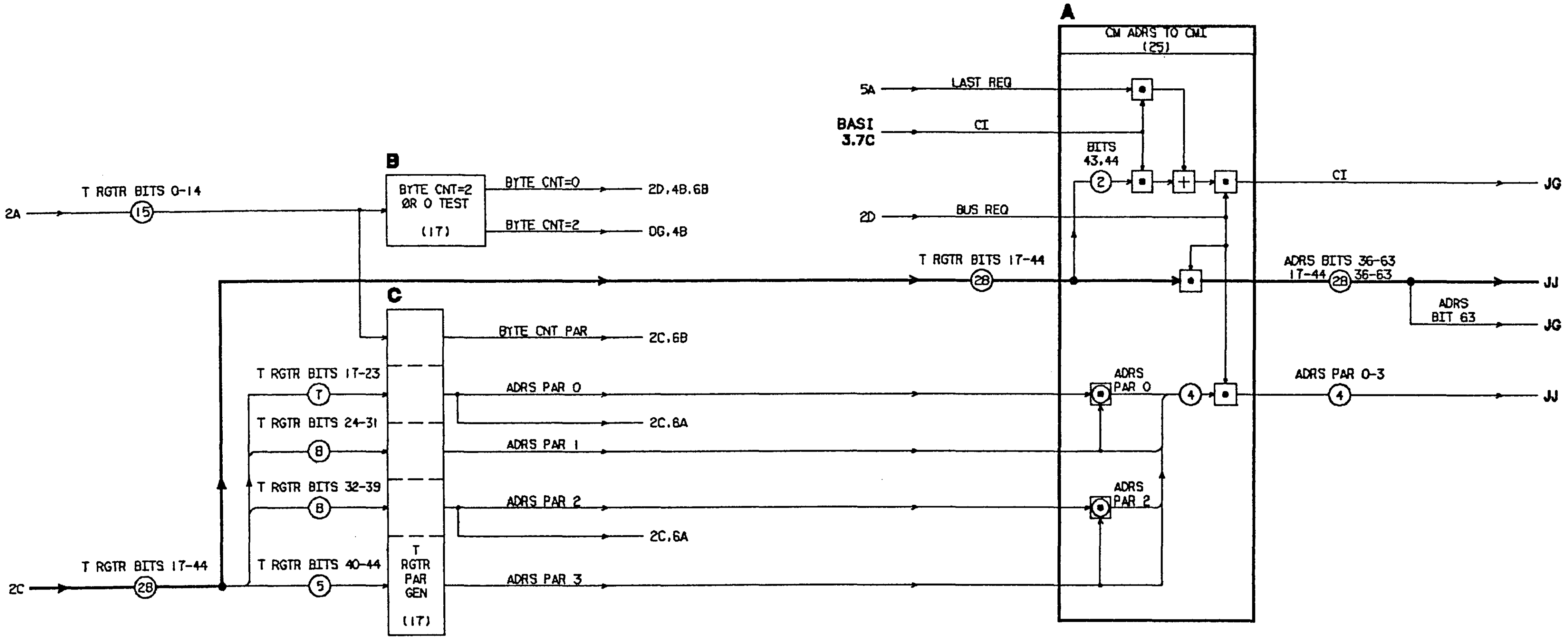
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
CM DATA DISASSEMBLY
11-06-86

CODE IDENT
DWG NO 60463540
REV C
SHEET A/D-1TO 3.1
PAGE



CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (JT)
T RGTR
60463540
C
A/D-1TO 3.2
11-06-86



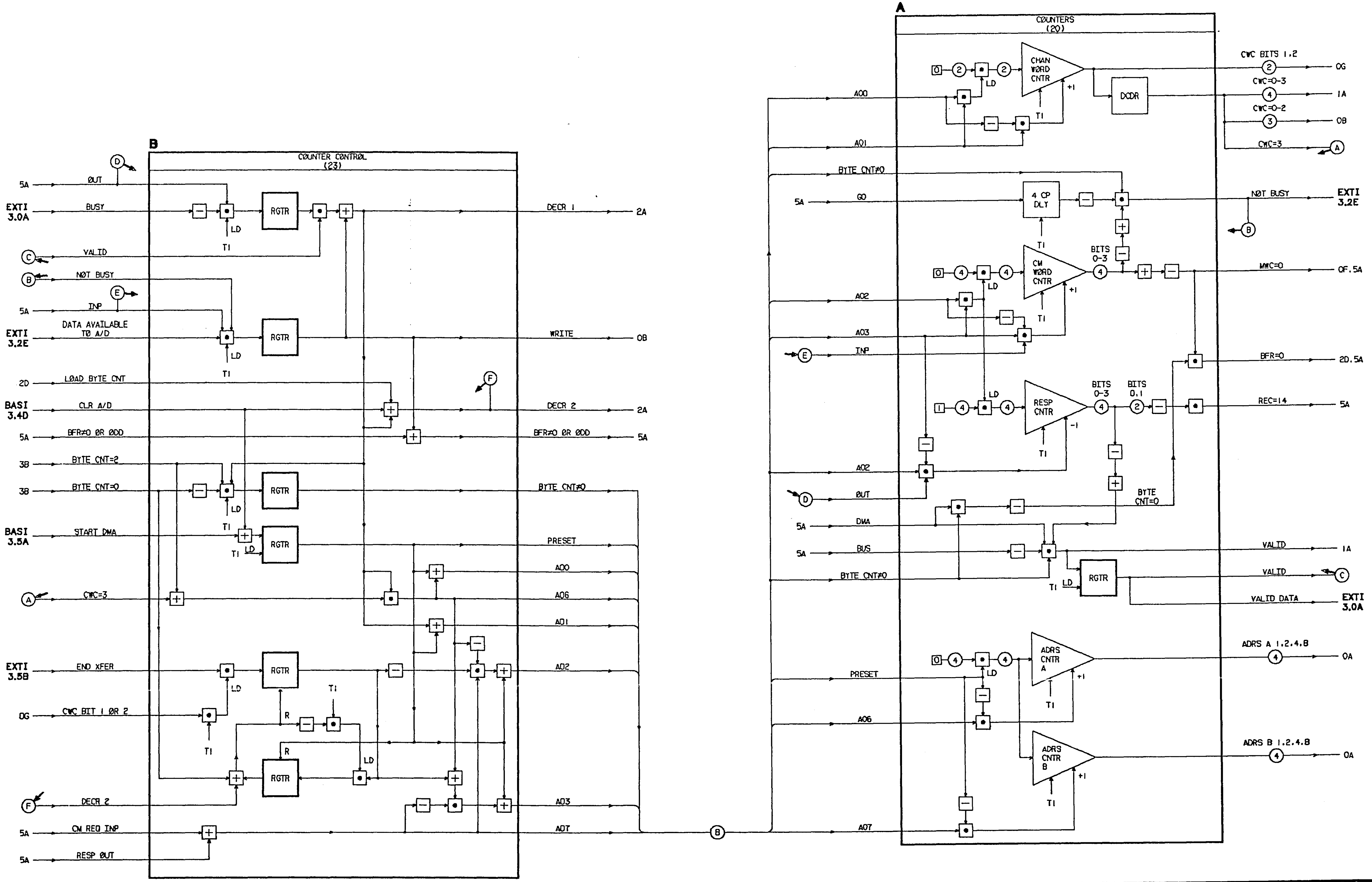
CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
CM ADRS T0 CMI

11-06-86

CODE IDENT | DWG NO 60463540 | REV C

SHEET A/D-1TO 3.3 | PAGE



CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
CHANNEL WORD, CM WORD,
RESPONSE, AND
ADRS COUNTERS

11-06-86

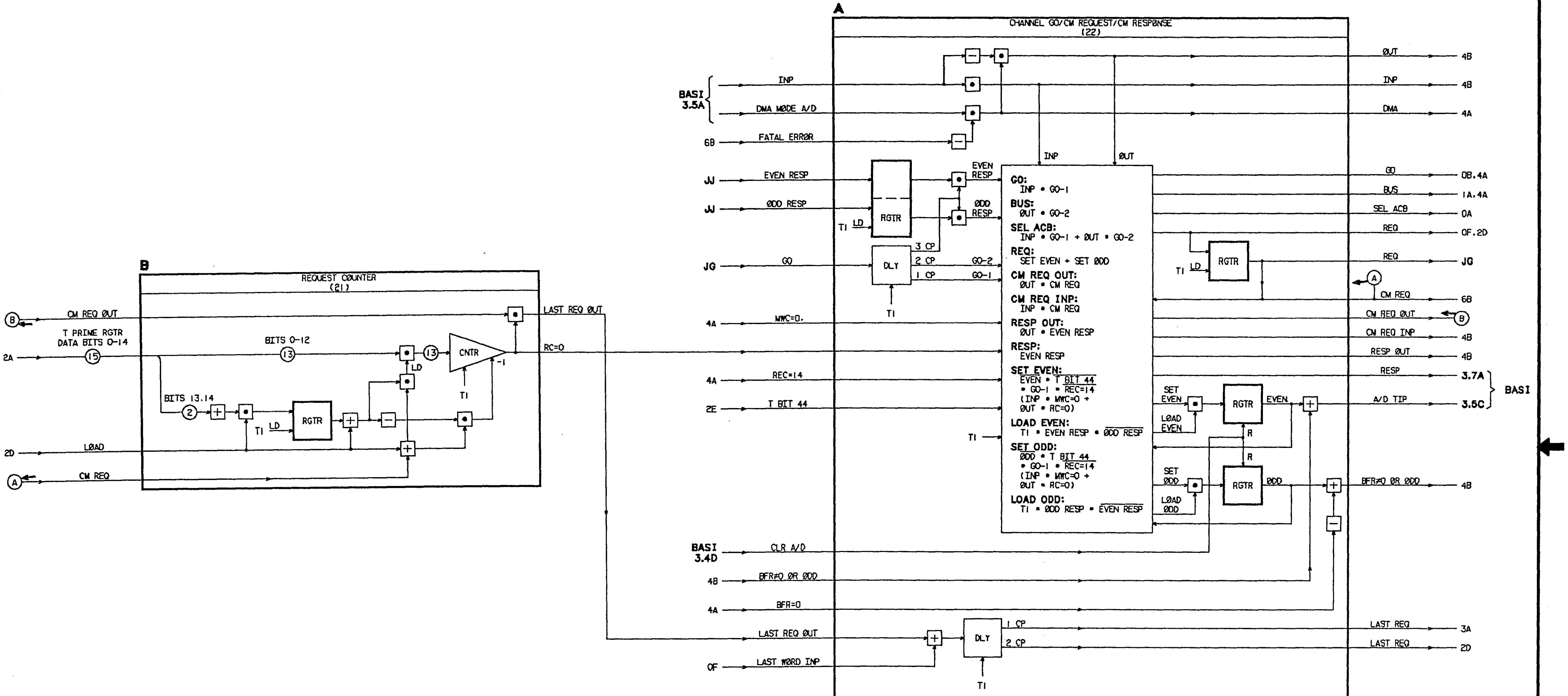
CODE IDENT

DWG NO 60463540

REV C

SHEET A/D-1 TO 3.4

PAGE



CONTROL DATA

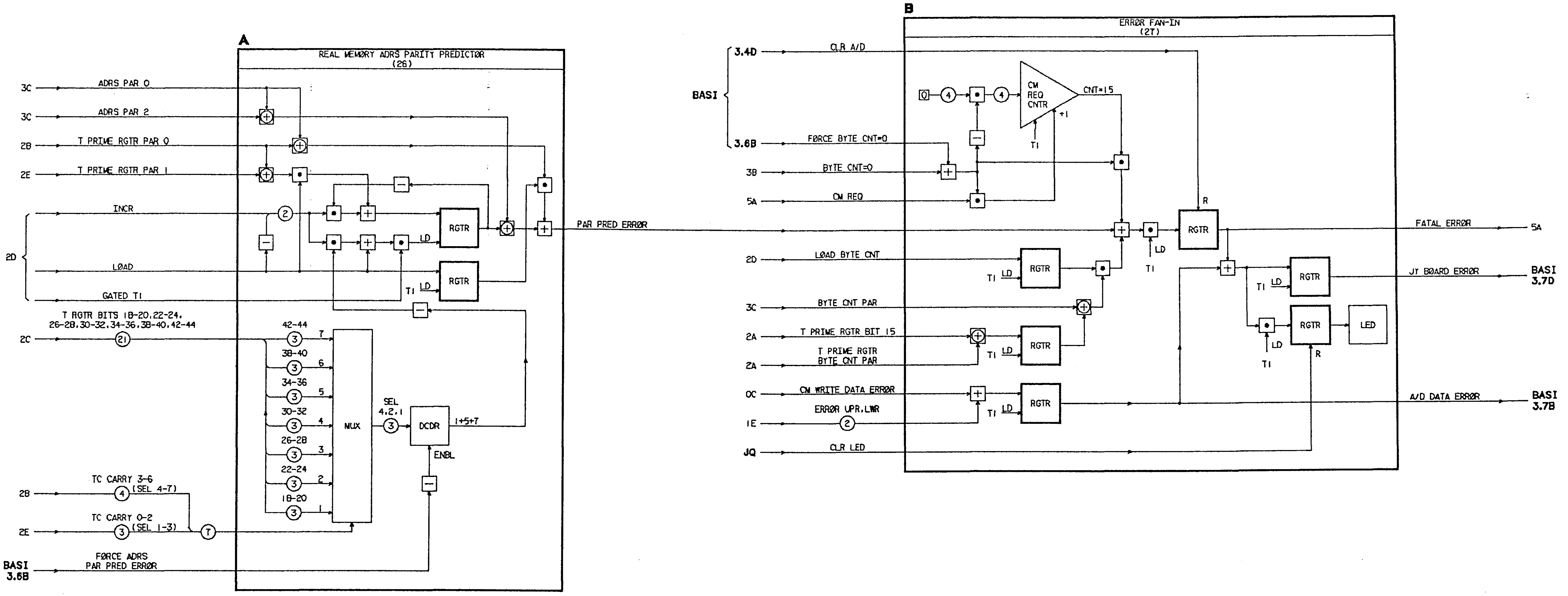
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
ASSEMBLY/DISASSEMBLY
CONTROL

11-06-86

DWG NO	REV
60463540	C

SHEET A/D-1 TO 3.5



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
ERRØR DETECTØR

11-06-86

CODE IDENT	DWG NO	REV
	60463540	C

SHEET	PAGE
A/D-1TO 3.6	

ADAPTER OVERVIEW

The Direct Memory Access (DMA) Enhanced Intelligent Peripheral Interface (IPI) Channel Adapter (adapter) consists of three logic boards and a cable drop. The adapter is installed in any of 10 external channel locations in the Concurrent Input/Output (CIO) cabinet. This option provides an interface between a CIO Peripheral Processor (PP) and an IPI channel. A PP controls the adapter by issuing functions and sending data using standard PP input/output (I/O) instructions.

The adapter enables the PP to transfer data between the external device and PP memory using standard I/O instructions. In addition, the adapter may transfer data between the external device and Central Memory (CM). This data flow is called DMA. The PP operates concurrently with the adapter during DMA data transfers. This allows the PP more time to process I/O requests from the CPU. The primary purpose of the adapter is to allow DMA transfers between a buffer residing in scattered pages of CM and an external device.

An I/O request consists of a list of commands. This list contains control information for the external device and data transfer length/address pairs for the adapter. These length/address pairs define the real memory address (word boundary) and length (bytes) in the CM buffer. Due to the physical sectoring of some external devices, the PP separates single length/address pairs into multiple pairs. This forces a transfer to end on a physical boundary.

BARREL AND SLOT INTERFACE (BASI)

The BASI (1LXH board) transfers data and control information between the Barrel and Slot (BAS) and the 1JYH and 1LZH boards as follows.

- Length/address pairs from Barrel and Slot (BAS) to T Prime Register (1JYH board).
- Length/address pairs from T Register (1JYH board) to BAS.
- Functions and control information from BAS to registers in DMA Array (1LZH board).
- Error status, operational status, and control information from registers in DMA Array (1LZH board) to BAS.
- Data from BAS to external device through 1LZH board.
- Data from external device to BAS through 1LZH board.

Data from one PP to another also passes through the BASI.

Maintenance Access Control (MAC) serially reads a 64-bit status word from the 1LZH board through the BASI into one of registers B0 through B9. Each channel location in the CIO cabinet is assigned to a B register.

EXTERNAL INTERFACE (EXTI)

The EXTI (1LZH board) transfers data between the external device and the Central Memory Interface (CMI) through the 1JYH board. The EXTI consists mainly of two 6000-gate arrays which control the data transfers. The IPI Array contains:

- Data Buffer (16 words)
- Status Register
- Error Register

The DMA Array contains:

- Function Decoder
- Control Register
- Operational Status Register
- Error Status Register

EXTI also contains a Random Data Generator which emulates the external device when the adapter is in test mode.

ASSEMBLY/DISASSEMBLY (A/D)

The A/D (1JYH board) transfers data between CMI and the 1LZH board. For input transfers, A/D assembles 16-bit channel words into 64-bit CM words. For output transfers, A/D disassembles 64-bit CM words into 16-bit channel words.

The 1JYH board also contains the T and T Prime Registers which hold the length/address pairs.

FUNCTION CODES

The DMA Array determines the adapter´s specified operation by decoding the function word from the PP. The adapter responds with an inactive status only when a legal function is decoded. The adapter uses functions which control internal operations, IPI channel, and IPI bus.

INTERNAL FUNCTIONS

Internal function codes are listed below.

Code (Hex)	Function
0000	Master Clear
0004	Read Random Data Generator
0014	Write Random Data Generator
0022	Clear IPI Error
0X22	Force Error
XX42	Set Sync Period
0X62	External Clock/Port Select
0100	Clear Error
0200	Read Control Register
0300	Write Control Register
0400	Select PP from DMA
0500	Select PP to DMA
0600	Read Error Status Register
0700	Read Operational Status Register
0800	DMA Terminate
0900	Illegal Function
0A00	Read T Register
0B00	Write T Prime Register
0C00	Select IPI to DMA
0D00	Select DMA to IPI
0E00	Clear T Registers
XF00	Illegal Function

BUS CONTROL FUNCTIONS

These functions establish the bus configuration for subsequent information transfers. Except for condition code 0, these functions are followed by one word from the external device on bus B which contains one byte of status and one byte of data. The conditions and signals defined by these functions remain unchanged until the next function arrives. The bus control functions are listed below.

Bits	Function
48-55	Bus A Output
56-59	Condition Code
60	Select Out
61	Master Out
62	Sync Out
63	One

The status and data from IPI channel bus B are listed below.

Bit	Function
48	Error
49	Attention
50	Buffer Not Empty
51	Select Out
52	Slave In
53	Master Out
54	Sync In
55	Sync Out
56-63	Bus B Input (Data Source)

CHANNEL FUNCTIONS

Channel function codes are listed below.

Code (Hex)	Function
00A1	Master Terminate
00C1	Attention Present
00E1	Read IPI Status Register
00F1	Read IPI Error Register
0X81	Data Transfer Functions

IPI STATUS REGISTER

This read-only register (IPI Array) provides information regarding the state of the IPI channel during DMA transfers. Bit assignments are listed below.

Bit	Status
48	Error
49	Attention
50	Buffer Not Empty
51	Select Out
52	Slave In
53	Master Out
54	Sync In
55	Sync Out
56-63	Not Used

IPI ERROR REGISTER

This read-only register (IPI Array) monitors the IPI Array's error checking circuits during DMA transfers. Bit assignments are listed below.

Bit	Error
48	Buffer Count Parity Error
49	Not Used
50	Sync Count Parity Error
51	Period Count Parity Error
52	Function Upper Parity Error
53	Function Lower Parity Error
54, 55	Not Used
56	Lost Data
57	ICI Upper Data Parity Error
58	ICI Lower Data Parity Error
59	IPI Sequence Error
60	IPI Bus A Parity Error
61	IPI Bus B Parity Error
62	Illegal Operation
63	Not Used

DMA CONTROL REGISTER

The control register (DMA Array) selects the different operating modes for the adapter. The PP reads or writes this register using the 0200 or 0300 function, respectively. Power on master clear or a master clear function (0000) clears this register. Bit assignments are listed below.

Bit	Description
48	Enable Cache Invalidate
49, 50	Not Used
51	Enable Test Mode
52	Inhibit Test Mode Increment
53	Enable Transfer in Progress Flag
54	Enable T Prime Empty Flag
55	Not Used
56	Enable Force Error Codes
57, 58	Not Used
59-63	Force Error Codes

DMA OPERATIONAL STATUS REGISTER

This read-only register (DMA Array) provides information regarding the state of the adapter and IPI channel during DMA transfers. The PP reads this register using the 0700 function. This status allows the PP to control the operation of the adapter. Bit assignments are listed below.

Bit	Description
48	Function Register Parity Error
49	Control Register Parity Error
50	Data Register Input Parity Error
51	Data Register Output Parity Error
52	T Register Counter Parity Error
53	Deadman Timer Counter Parity Error
54, 55	Zero
56	DMA Transfer in Progress
57	IPI Transfer In Progress
58	Output Mode
59	Not Used
60	DMA/IPI Mode
61	PP/IPI Mode
62	T Prime Register Empty
63	Transfer In Progress

DMA ERROR STATUS REGISTER

This read-only register (DMA Array) monitors the adapter's error checking circuits to determine if any hardware errors have occurred. The PP reads this register using the 0600 function. The PP uses this error status for fault isolation and to determine the validity of a transfer. All error bits are ORed to form the adapter's error flag. This register is cleared by a master clear (0000) function or a clear error (0100) function. Bit assignments are listed below.

Bit	Description
48	Zero
49	Illegal Function or Sequence
50	Uncorrectable CM Error
51	CM Reject
52	Invalid Response
53	Response Code Parity Error
54	CMI Read Data Parity Error
55	IPI Error
56	DMA Register Parity Error
57	MAC Status Parity Error
58	Timeout
59	A/D Data Error
60	BAS Parity Error
61	LZ Error
62	JY Error
63	LX Error

DATA PATHS

The following paragraphs describe the adapter data paths for each of the transfers.

PP TO T PRIME REGISTER

The PP writes three words into the T Prime Register through the BAS Register and T Register Data Bus.

PP FROM T REGISTER

The PP reads three words from the T Register through the BAS Register and BAS Data Bus.

PP TO FUNCTION REGISTER AND CONTROL REGISTER

The PP writes these DMA Array registers through the BAS Register and the two channel Data Buses.

PP FROM ERROR STATUS, OPERATIONAL STATUS, AND CONTROL REGISTERS

The PP reads these DMA Array registers through the Channel Data Bus, BAS Register, and BAS Data Bus.

INTER-PP TRANSFER

Data passes from one PP to another through the BAS Register and BAS Data Bus.

PP OUTPUT TRANSFER

Data passes from the PP to the external device through the BAS Register, two Channel Data Buses, DMA Array, IPI Array, and IPI Ports A, B Transmitters.

PP INPUT TRANSFER

Data passes from the external device to the PP through the IPI Ports A, B Receivers, IPI Array, DMA Array, Channel Data Bus, BAS Register, and BAS Data Bus.

DMA OUTPUT TRANSFER

Data passes from CM to the external device through the Disassembly Buffer, DMA Data Bus, IPI Array, and IPI Ports A, B Transmitters.

DMA INPUT TRANSFER

Data passes from the external device to CM through the IPI Ports A, B Receivers, IPI Array, DMA Data Bus, and Assembly Buffer.

TEST MODE

Test mode allows testing the adapter´s internal data paths without an external device. The Random Data Generator supplies data for input transfers and produces a check sum for output transfers. In test mode, the adapter simulates maximum transfer rates.

The following paragraphs describe data paths and typical programming sequences for the adapter in test mode.

PP OUTPUT TRANSFER

Data passes from the PP, to the Random Data Generator, and back to the PP as follows.

1. PP sends a block of data words to Random Data Generator through BAS Register, two Channel Data Buses, DMA Array, and IPI Array.
2. Random Data Generator determines sum of words.
3. Random Data Generator sends result sum to PP through DMA Array, Channel Data Bus, BAS Register, and BAS Data Bus.
4. PP checks results.

PP INPUT TRANSFER

Data passes from the Random Data Generator to the PP as follows.

1. Random Data Generator produces a block of data words.
2. Random Data Generator sends block of data words to PP through IPI Ports A, B Transmitters/Receivers, IPI Array, DMA Array, Channel Data Bus, BAS Register, and BAS Data Bus.
3. PP checks block of data words.

DMA OUTPUT TRANSFER

Data passes from CM, to the Random Data Generator, and then to the PP as follows.

1. CM sends a block of data words to Random Data Generator through Disassembly Buffer, DMA Data Bus, and IPI Array.
2. Random Data Generator determines sum of words.
3. Random Data Generator sends result sum to PP through DMA Array, Channel Data Bus, BAS Register, and BAS Data Bus.
4. PP checks results.

A typical programming sequence for a DMA output transfer follows.

1. Issue master reset to external device to disable transmitters/receivers.
2. Function adapter to write Random Data Generator (internal function 0014).
3. Enable test mode (control register bit 51).
4. Function adapter to set select out (channel function 0009).
5. Function adapter for data transfer (channel function 0X81).
6. Function adapter for DMA write to IPI (internal function 0D00).
7. Function adapter to read Random Data Generator at end of transfer (internal function 0004).

DMA INPUT TRANSFER

Data passes from the Random Data Generator to CM as follows.

1. Random Data Generator produces a block of data words.
2. Random Data Generator sends block of data words to CM through IPI Ports A, B Transmitters/Receivers, IPI Array, DMA Data Bus, and Assembly Buffer.

A typical programming sequence for a DMA input transfer follows.

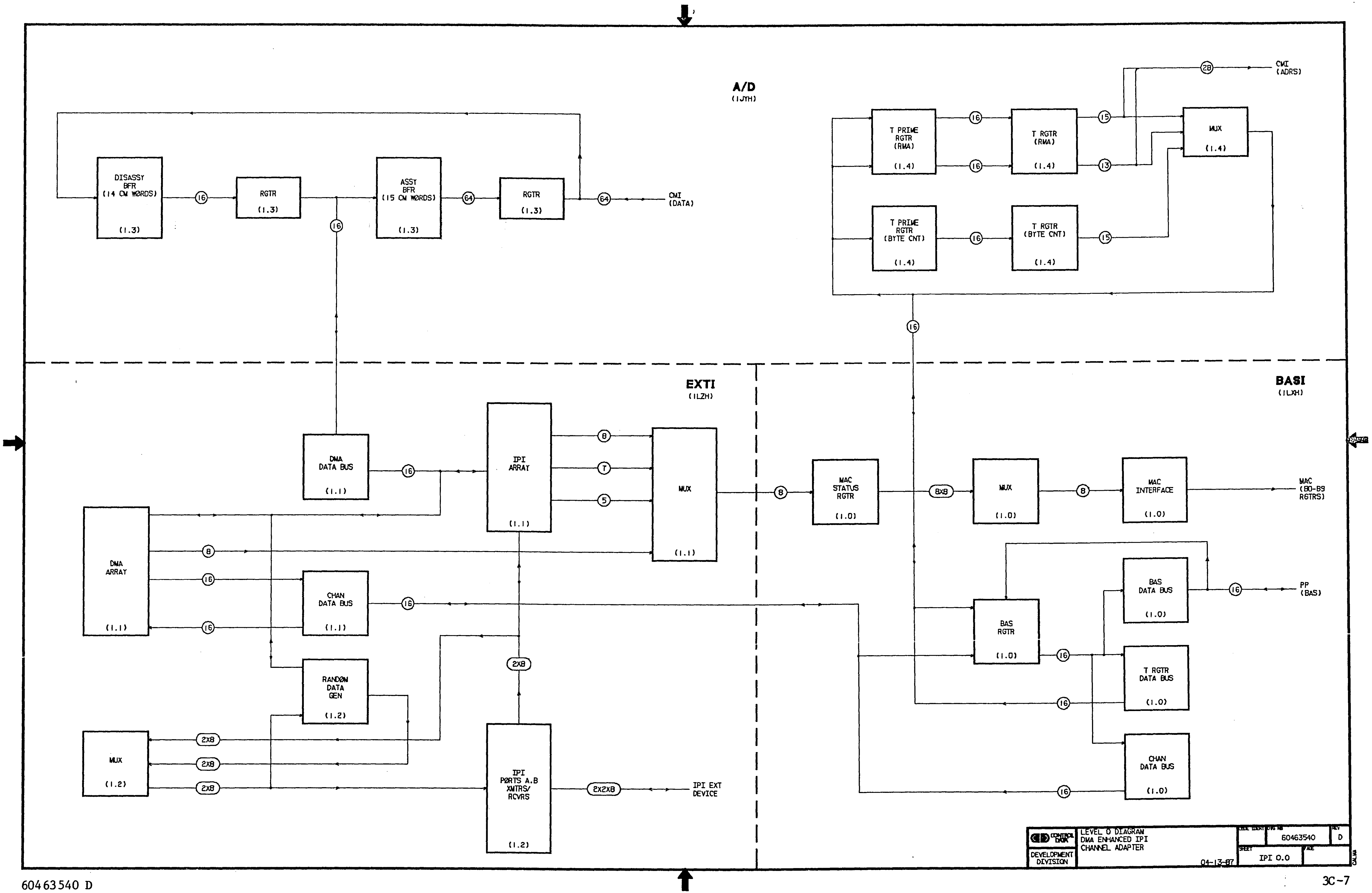
1. Issue master reset to external device to disable transmitters/receivers.
2. Function adapter to write Random Data Generator (internal function 0014).
3. Enable test mode (control register bit 51).
4. Function adapter to set select out (channel function 0009).
5. Function adapter for data transfer (channel function 0X81).
6. Function adapter for DMA read from IPI (internal function 0C00).

MAINTENANCE ACCESS CONTROL (MAC) INTERFACE

Any PP can read certain registers in the adapter by doing a maintenance register read of the appropriate channel status register. For example, if the adapter is installed in CIO channel location 0, the PP does a maintenance register read on register B0. If installed in location 1, the read is on register B1. This continues through channel location 11 (octal) with the read on register B9. The format for the adapter's channel status is shown below.

Byte	Description
0	DMA Error Status--Leftmost Byte (DMA Maintenance Bits 56-63) Bit 0 - Zero 1 - Illegal Function or Sequence 2 - Uncorrected CM Error 3 - CM Reject 4 - Invalid Response Code 5 - CM Response Code Parity Error 6 - CMI Read Data Parity Error 7 - IPI Error
1	DMA Error Status--Rightmost Byte (DMA Maintenance Bits 56-63) Bit 8 - DMA Register Parity Error 9 - MAC Status Parity Error 10 - Timeout 11 - A/D Data Error 12 - BAS Register Parity Error 13 - LZ Board Error 14 - JY Board Error 15 - LX Board Error
2	IPI Error Status--Leftmost Byte (IPI Error Byte 2 Bits 56-63) Bit 16 - Buffer Count Parity Error 17 - Zero 18 - Sync Count Parity Error 19 - Period Count Parity Error 20 - Function Upper Parity Error 21 - Function Lower Parity Error 22 - Zero 23 - Zero
3	IPI Error Status--Rightmost Byte (IPI Error Byte 3 Bits 56-63) Bit 24 - Lost Data 25 - ICI Upper Data Parity Error 26 - ICI Lower Data Parity Error 27 - IPI Sequence Error 28 - IPI Bus A Parity Error 29 - IPI Bus B Parity Error 30 - Illegal Operation 31 - Zero

Byte	Description
4	DMA Operational Status (DMA Maintenance Bits 56-63) Bit 32 - Zero 33 - Zero 34 - Output Mode 35 - Zero 36 - DMA/IPI Mode 37 - DMA/IPI Inactive 38 - T Prime Register Empty 39 - Transfer In Progress
5	Flag Status Bit 40 - Zero 41 - Zero 42 - Zero 43 - Zero 44 - Active 45 - Full 46 - Error 47 - Flag
6	DMA Control Register Status (DMA Maintenance Bits 56-63) Bit 48 - Enable Cache Invalidate 49 - Zero 50 - Disable Timeout 51 - Enable Test Mode 52 - Inhibit Test Mode Increment 53 - Enable Transfer In Progress Flag 54 - Enable T Prime Empty Flag 55 - Zero
7	IPI Status Register (IPI Operation Status Bits 56-63) Bit 56 - Error 57 - Attention 58 - Buffer Not Empty 59 - Select Out 60 - Slave In 61 - Master Out 62 - Sync In 63 - Sync Out


A/D
(1JYH)
DISASSY BFR (14 CM WORDS) (1.3)
16
RGTR (1.3)
16
ASSY BFR (15 CM WORDS) (1.3)
64
RGTR (1.3)
64
CMI (DATA)
T PRIME RGTR (RMA) (1.4)
16
16
T RGTR (RMA) (1.4)
15
13
MUX (1.4)
28
CMI (ADRS)
T PRIME RGTR (BYTE CNT) (1.4)
16
T RGTR (BYTE CNT) (1.4)
15
16
EXTI
(1LZH)
DMA DATA BUS (1.1)
16
IPI ARRAY (1.1)
8
7
5
MUX (1.1)
DMA ARRAY (1.1)
8
16
16
CHAN DATA BUS (1.1)
16
RANDOM DATA GEN (1.2)
2X8
MUX (1.2)
2X8
2X8
2X8
IPI PORTS A.B XMTRS/ RCVRS (1.2)
2X2X8
IPI EXT DEVICE
BASI
(1LXH)
8
MAC STATUS RGTR (1.0)
8X8
MUX (1.0)
8
MAC INTERFACE (1.0)
MAC (B0-B9 RGTRS)
BAS DATA BUS (1.0)
16
PP (BAS)
BAS RGTR (1.0)
16
T RGTR DATA BUS (1.0)
16
CHAN DATA BUS (1.0)
16
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 0 DIAGRAM
DMA ENHANCED IPI
CHANNEL ADAPTER
04-13-87
CODE IDENT
DWG NO
60463540
REV
D
SHEET
IPI 0.0
PAGE
CALMA

DATA PATHS

All data to/from a PP flows through the Barrel and Slot (BAS) Register. Depending on the operation, data also flows through the BAS Data Bus, Channel Data Bus, or T Register Data Bus.

BAS DATA BUS

A PP reads data through the BAS Register and the BAS Data Bus for the following operations.

- PP from T Register (shown on IPI 1.4B).
- PP from Error Status Register in DMA Array (1.1A).
- PP from Operational Status Register in DMA Array (1.1A).
- PP from Control Register in DMA Array (1.1A).
- Inter-PP transfer.
- PP input transfer from external device.

CHANNEL DATA BUS

A PP writes data through the BAS Register and the Channel Data Bus for the following operations.

- PP to Function Register in DMA Array (1.1A).
- PP to Control Register in DMA Array (1.1A).
- PP output transfer to external device.

T REGISTER DATA BUS

A PP writes data to the T Prime Register (1.4A,C,F) through the BAS Register and the T Register Data Bus.

CHANNEL FLAGS AND MICROCODE TRANSLATOR

Microcode Bit 85 sets the programmable Channel Flag that is used by the operating system. The other signals generated by this circuit control data flow within the adapter. The Microcode Translator decodes Microcode Bits 73 through 75 as follows to determine which input/output instruction is being executed by the PP.

Decode	Instruction
0	Function
1	Activate
2	Output
3	Input
4	Inactivate
5	Clear Error Flag
6	Clear Channel Flag
7	Not Used

CM FUNCTION CODE

This circuit generates a function code for CM during DMA transfers. Only two functions are possible. They are CM read (DMA output) and CM write (DMA input).

CM RESPONSE CODE

This circuit checks the response code from CM for errors. If any errors occurred, the appropriate signals go to the error status register in the DMA Array (1.1A).

ERROR STATUS

This circuit monitors the parity checkers in BASI for errors. If an error occurs, an LED lights and LX Error goes to the error status register in the DMA Array. BAS Parity Error indicates a parity checker in the BAS Register detected a Channel Parity Error on BAS, channel, or T register data. MAC Parity Error indicates a parity checker in the MAC Mux detected a status error.

MAC CONTROL

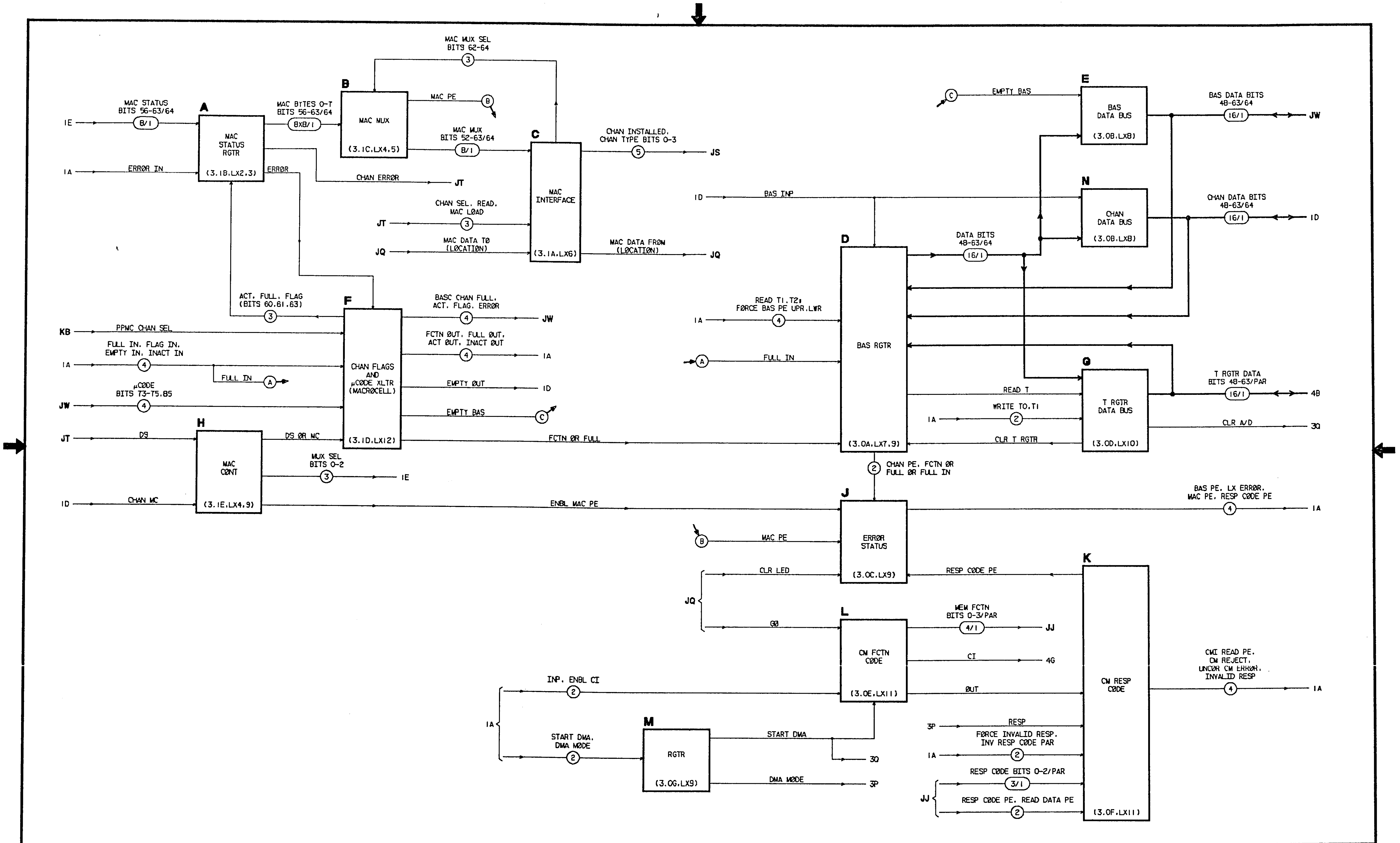
This circuit contains a free-running counter which controls the flow of status from the adapter to MAC.

MAC INTERFACE

MAC reads the adapter's status through the MAC Status Register, MAC Mux, and a shift register in the MAC Interface as follows.

1. MAC sends 5-bit serial string to MAC Interface on MAC Data To line.
2. Shift register in MAC Interface shifts 5-bit string into bit positions 60 through 64. (Bits 60 and 61 are not used.)
3. MAC Interface sends MAC Mux Select Bits 62 through 64 from shift register to MAC Mux.
4. MAC Mux sends selected 8-bit status byte to MAC Interface.
5. MAC Load from MRB loads entire status byte into shift register.
6. Read from MRB enables serial status byte (shifted through shift register) to MAC on MAC Data From line.

The MAC Interface also sends hard-wired Channel Installed and Channel Type information to the options installed register in MRA.



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (BASI)
BARREL AND SLOT
INTERFACE

CODE IDENT
DWG NO 60463540
REV F
SHEET IPI 1.0
PAGE

DATA PATHS

The following paragraphs describe data flow through the DMA Array, IPI Array, DMA Data Bus, and Channel Data Bus.

PP TO FUNCTION AND CONTROL REGISTERS

Channel output data from BASI (1.0N) goes to the DMA Array through the Channel Data Bus.

PP FROM ERROR STATUS, OPERATIONAL STATUS, AND CONTROL REGISTERS

Channel input data from the DMA Array goes to BASI through the Channel Data Bus.

PP OUTPUT TRANSFER

1. Channel output data from BASI goes to the DMA Array through the Channel Data Bus.
2. ICI-2 data from the DMA Array goes to the IPI Array.
3. IPI bus data goes from the IPI Array to the IPI Data Out Mux (1.2B).

PP INPUT TRANSFER

1. IPI bus data from the receivers (1.2A) goes to the IPI Array.
2. ICI-2 data from the IPI Array goes to the DMA Array.
3. Channel input data from the DMA Array goes to BASI through the Channel Data Bus.

DMA OUTPUT TRANSFER

1. DMA data from A/D (1.3K) goes to the IPI Array through the DMA Data Bus as ICI-2 data.
2. IPI bus data from the IPI Array goes to the IPI Data Out Mux (1.2B).

DMA INPUT TRANSFER

1. IPI bus data from the receivers (1.2A) goes to the IPI Array.
2. ICI-2 data from the IPI Array goes to A/D through the DMA Data Bus as DMA data.

TEST MODE DATA PATHS

The following paragraphs describe data flow when the adapter is in test mode.

PP OUTPUT TRANSFER

1. A block of words (channel output data) goes from BASI to the DMA Array through the Channel Data Bus.
2. ICI-2 data from the DMA array goes to the IPI Array.
3. IPI bus data from the IPI Array goes to the IPI Data Out Mux (1.2B).
4. Result sum from Random Data Generator-2 goes to the DMA Array as ICI-2 data.
5. Channel input data from the DMA Array goes to BASI through the Channel Data Bus.

PP INPUT TRANSFER

1. A block of random data words (IPI bus data) from the transmitters/receivers (1.2A) goes to the IPI Array.
2. ICI-2 data from the IPI Array goes to the DMA Array.
3. Channel input data from the DMA Array goes to BASI through the Channel Data Bus.

DMA OUTPUT TRANSFER

1. A block of words (DMA data) from A/D (1.3K) goes to the IPI Array through the DMA Data Bus as ICI-2 data.
2. IPI bus data from the IPI Array goes to the IPI Data Out Mux (1.2B).
3. Result sum from Random Data Generator-2 goes to the DMA Array as ICI-2 data.
4. Channel input data from the DMA Array goes to BASI through the Channel Data Bus.

DMA INPUT TRANSFER

1. A block of random data words (IPI bus data) goes from the receivers/transmitters to the IPI Array.
2. ICI-2 data from the IPI Array goes to A/D through the DMA Data Bus as DMA data.

POWER ON ONE SHOT

This circuit synchronizes the transmitters on the DMA and IPI Arrays. The power on master clear signal disables the transmitters. The power on clear in signal enables them. This allows all transmitters to come up in one state.

DEAD MAN TIMEOUT OSCILLATOR

This circuit limits data transfers through the DMA Array to one second.

LED

Any error detected on the 1LZH board lights this LED. It remains lit until the clear LED signal arrives from MAC.

DMA ARRAY

The DMA Array decodes the adapter´s function and contains the control, operational status, and error status registers.

INTERNAL FUNCTION CODES

The DMA Array determines the adapter´s specified operation by decoding the function word from the PP. The adapter responds with an inactive status only when a legal function is decoded. The function word arrives from the PP through the Channel Data Bus. Internal function codes are described in the following paragraphs.

Master Clear (0000)

This function clears all DMA Array Registers, IPI Array Registers, T Prime Register, and T Register.

Read Random Data Generator (0004)

In test mode, this function allows the PP to read the Random Data Generator. After the PP sends this function and an activate signal, the adapter responds with a full signal and the data.

Write Random Data Generator (0014)

In test mode, this function allows the PP to write the Random Data Generator. After the PP sends this function and an activate signal, the adapter accepts two words.

The first word (bits 48 through 63) contains data for the Random Data Generator.

The second word contains control information. Bit 48 indicates the IPI transfer will be in stream mode. Bit 49 inhibits the sync counter. This allows the data transfer to continue until the PP sends a master terminate function. Bits 50 through 63 contains the sync count. This count determines the number of sync in´s during a transfer. The data transfer terminates when the sync count reaches zero.

Clear IPI Error (0022)

This function clears the IPI error register and buffer counter in the IPI Array.

Force Error (0X22)

The following functions test the parity checkers in the IPI Array. Parity errors set corresponding IPI error register bits.

Function	Error Register Bit	Test
0122	60	IPI bus A during output transfer.
0222	61	IPI bus B during output transfer.
0322	60	IPI bus A during input transfer.
0422	61	IPI bus B during input transfer.
0522	48	Buffer counter 1 during data transfer.
0622	48	Buffer counter 2 during data transfer.
0722	48	Buffer write address during data transfer.
0822	48	Buffer read address 1 during data transfer.
0922	48	Buffer read address 2 during data transfer.
0A22	50	Sync counter during transfer.
0B22	51	Period counter during channel transfer.
0C22	58	ICI output data (lower) during transfer to PP or DMA Array.
0D22	57	ICI output data (upper) during transfer to PP or DMA Array.
0E22	53 or 58	ICI input data (lower) when DMA Array receives a function or data.
0F22	52 or 57	ICI input data (upper) when DMA Array receives a function or data.

Set Sync Period (XX42)

The following functions select the transfer rate for the IPI channel.

Function	12 MHz Ext Clk (MBytes/Sec)	16 MHz Ext Clk (MBytes/Sec)	20 MHz Ext Clk (MBytes/Sec)
8042	0.09	0.13	0.16
E742	0.48	0.64	0.80
E842	0.50	0.67	0.83
EC42	0.60	0.80	1.00
F342	0.92	1.23	1.54
F442	1.00	1.33	1.67
F542	1.09	1.45	1.82
F642	1.20	1.60	2.00
F742	1.33	1.78	2.22
F842	1.50	2.00	2.50
F942	1.71	2.29	2.86
FA42	2.00	2.67	3.33
FB42	2.40	3.20	4.00
FC42	3.00	4.00	5.00
FD42	4.00	5.33	6.67
FE42	6.00	8.00	10.00

Function	20 MHz Int Clk (MBytes/Sec)
0042	0.16
6842	0.80
6C42	1.00
7442	1.67
7642	2.00
7942	2.86
7B42	4.00
7C42	5.00
7D42	6.70
7E42	10.00

External Clock/Port Select (0X62)

The following functions select the external clock. If the internal clock is selected by a set sync period function (XX42), these functions also select port A or B for the IPI channel.

Function	Clock (MHz)	Port
0062	20	A
0162	12	A
0262	16	A
0362	--	A
0462	--	A
0562	--	A
0662	--	A
0762	--	A
0862	20	B
0962	12	B
0A62	16	B
0B62	--	B
0C62	--	B
0D62	--	B
0E62	--	B
0F62	--	B

Clear Error (0100)

This function clears the error status register (DMA Array) and the IPI error register (IPI Array).

Read Control Register (0200)

This function reads the control register (DMA Array). The sequence is:

1. PP sends this function and activate signal to adapter.
2. Adapter sends full signal and contents of control register to PP.
3. PP sends empty signal to adapter.
4. Adapter sends inactive signal to PP.

Write Control Register (0300)

This function writes the control register (DMA Array). After the PP sends this function and an activate signal, the adapter accepts the following word as control register write data. If the PP sends a second word, the adapter does not respond.

Select PP from DMA (0400)

This function allows the PP to read CM through the DMA path. The sequence is:

1. PP loads T Register through T Prime Register (internal function 0B00).
2. PP sends this function to adapter.
3. PP sends activate signal to adapter and inputs data. (Activating channel enables DMA output, DMA mode, and start DMA signals.)

Select PP to DMA (0500)

This function allows the PP to write CM through the DMA path. The sequence is:

1. PP loads T Register through T Prime Register (internal function 0B00).
2. PP sends this function to adapter.
3. PP sends activate signal to adapter and outputs data. (Activating channel enables DMA input, DMA mode, and start DMA signals.)

Read Error Status Register (0600)

This function reads the error status register (DMA Array). The sequence is:

1. PP sends this function and an activate signal to adapter.
2. Adapter sends full signal and contents of error status register to PP.
3. PP sends empty signal to adapter.
4. Adapter sends inactive signal to PP.

Read Operational Status Register (0700)

This function reads the operational status register (DMA Array). The sequence is:

1. PP sends this function and an activate signal to adapter.
2. Adapter sends full signal and contents of operational status register to PP.
3. PP sends empty signal to adapter.
4. Adapter sends inactive signal to PP.

Illegal Function (0900)

The adapter ignores this function and does not send an inactive signal to the PP.

Read T Register (0A00)

This function enables the PP to read the T Register. After the PP sends this function and an activate signal, the adapter sends three 16-bit words which contain the current contents of the T Register in the following order.

1. Byte Count Bits 0-15
2. CM Address Bits 36-51
3. CM Address Bits 52-63

Write T Prime Register (0B00)

This function enables the PP to write the T Prime Register. After the PP sends this function and an activate signal, the adapter accepts the next three 16-bit words as T Prime Register write data in the following order.

1. Byte Count Bits 0-15
2. CM Address Bits 36-51
3. CM Address Bits 52-63

If the PP sends more than three words, the fourth word remains in the BAS Register and the full flag remains set.

Select IPI to DMA (0C00)

This function enables the adapter to perform a DMA input operation. The sequence is:

1. PP sends this function and an activate signal to adapter.
2. PP writes three words into T Register.
3. Adapter sends inactive signal to PP.
4. DMA Array sends active signal to IPI Array.
5. IPI Array selects DMA input from external device.
6. DMA Array sends DMA mode and start DMA signals to A/D.

Select DMA to IPI (0D00)

This function enables the adapter to perform a DMA output operation. The sequence is the same as above except IPI Array selects DMA output to external device (step 5).

Clear T Prime Register (0E00)

This function clears the T Register, T Prime Register, Assembly Buffer, and Disassembly Buffer.

Illegal Functions (XF00)

The adapter ignores these functions and does not send an inactive signal to the PP.

BUS CONTROL FUNCTIONS

These functions establish the bus configuration for subsequent information transfers. Except for condition code 0, these functions are followed by one word from the external device on bus B which contains one byte of status and one byte of data. The conditions and signals defined by these functions remain unchanged until the next function arrives. The bus control function word is described below.

Bits	Function	Description
48-55	Bus A Output	Output on IPI channel bus A for condition codes 0-7.
56-59	Condition Code	Specifies under what conditions data is available to the PP, source of data, if parity is checked/regenerated, and transmitter/receiver enables.
60	Select Out	Causes IPI channel select out signal to activate.
61	Master Out	Causes IPI channel master out signal to activate.
62	Sync Out	Causes IPI channel sync out signal to activate.
63	Not Used	Constant one.

If bits 60 and 61 are clear and bit 62 is set, bit 53 becomes the IPI channel bus A parity bit.

The following steps describe the sequence of events for condition codes 0 through 3 and 5 through 7. Code 4 is not used. Parity is checked for codes 3 and 5 only. Except for code 0, bus B provides input data and status.

Code	Sequence
0	1. Output bus A if bus A transmitters are enabled.
	2. Set IPI controls (bits 1-3).
1-3, 5-7	1. Enable bus A transmitters and bus B receivers.
	2. Output bus A.
	3. Set IPI controls (bits 1-3).
	4. Return data to PP when: ● Channel goes active (code 1). ● Slave in signal goes active (codes 2, 3). ● Sync in signal goes active (code 5). ● Sync in signal goes inactive (code 6). ● Slave in signal goes inactive (code 7).
	5. Inactive channel when empty in signal arrives from PP.

The status and data from IPI channel bus B are listed below. The status bits from the external device are described under IPI Status Register. This status is in response to a channel function from the adapter.

Bit	Function
48	Error
49	Attention
50	Buffer Not Empty
51	Select Out
52	Slave In
53	Master Out
54	Sync In
55	Sync Out
56-63	Bus B Input (Data Source)

CHANNEL FUNCTIONS

Channel function codes are described in the following paragraphs.

Master Terminate (00A1)

This function terminates data transfers on the IPI channel. The sequence is:

1. For DMA input transfers, Assembly Buffer empties.
2. Master out signal to external device goes inactive to initiate master terminate sequence.
3. Sync out signals continue for every sync in signal from external device (stream mode).
4. When slave in signal from external device goes inactive, PP reads contents of IPI status register (IPI Array).
5. When empty in signal arrives from PP, IPI channel deactivates.

Attention Present (00C1)

This function returns the contents of the IPI status register (IPI Array) to the PP when the attention in signal arrives from the external device. The channel deactivates when the empty in signal arrives from the PP.

Read IPI Status Register (00E1)

This function returns the contents of the IPI status register (IPI Array) after the PP activates the channel. The channel deactivates when the empty in signal arrives from the PP.

Read IPI Error Register (00F1)

This function returns the contents of the IPI error register (IPI Array) after the PP activates the channel. The channel deactivates when the empty in signal arrives from the PP.

Data Transfer Functions (0X81)

The following functions prepare the IPI Array for data transfers by enabling its internal buffer and activating the master out signal. The PP activates the channel and executes the appropriate I/O instruction.

Code (Hex)	Function
0081	DMA Output, 16-Bit Word, Interlock Mode
0181	DMA Input, 16-Bit Word, Interlock Mode
0281	DMA Output, 16-Bit Word, Stream Mode
0381	DMA Input, 16-Bit Word, Stream Mode
0481	DMA Output, 8-Bit Word, Interlock Mode
0581	DMA Input, 8-Bit Word, Interlock Mode
0681	DMA Output, 8-Bit Word, Stream Mode
0781	DMA Input, 8-Bit Word, Stream Mode

CONTROL REGISTER

The control register in the DMA Array selects the different operating modes for the adapter. The PP reads or writes this register using the 0200 or 0300 function, respectively, through the Channel Data Bus. Power on master clear or a master clear function (0000) clears this register. MAC also reads this register through the MAC Mux. Bit assignments are described in the following paragraphs.

Enable Cache Invalidate (48)

This bit enables a cache invalidate signal with every fourth and last word written to CM during a DMA transfer.

Enable Test Mode (51)

This bit places the adapter in test mode. The Random Data Generator provides data and control signals to simulate high-speed I/O transfers. Test mode disables the transmitters and receivers which are not tested.

Inhibit Test Mode Increment (52)

In test mode, this bit allows the use of constant data patterns by preventing the Random Data Generator from incrementing.

Enable Transfer In Progress Flag (53)

This bit enables setting the channel flag when the transfer in progress signal clears. This indicates a DMA transfer is complete.

Enable T Prime Empty Flag (54)

This bit enables setting the channel flag when the T Prime Register empties. This indicates the contents of the T Prime Register has transferred to the T Register. The PP can now load the T Prime Register for the next transfer.

Enable Force Error Codes (56)

This bit enables the decoding of control register bits 59 through 63.

Force Error Codes (59-63)

When bit 56 is set, these codes enable testing the adapter´s parity checkers. The following paragraphs describe hexidecimal codes 00 through 18 .

Invert Operational Status Parity Upper, Lower (00, 01)

These codes invert the parity bits for the upper and lower bytes of the operational status register. A parity error occurs when the PP reads this status. Error status register bit 61 sets.

Force T Register Read/Write Counter Parity Error (02)

This code inverts the parity bit for the T register read/write select counter. A parity error occurs in the next clock period. Error status register bits 56 and 61 and operational status register bit 52 set.

Force Function Register Parity Error (03)

This code inverts the parity bit for the function register. A parity error occurs in the next clock period. Error status register bits 56 and 61 and operational status register bit 48 set.

Force Invalid Response (04)

This code causes an illegal translation of the CM response code during a CM reference. Error status register bit 52 sets.

Invert Response Code Parity (05)

This code inverts the parity bit for the CM response code during a CM reference. Error status register bit 63 sets and the LX board LED lights.

Force BAS Parity Error Upper, Lower (06, 07)

These codes force parity errors on the upper and lower bytes of data transferred from the PP to the BAS Register. Error status register bits 60 and 63 set.

Invert Input Data Parity to BAS (08)

This code inverts the parity bit for data transferred from the LZ board to the BAS Register (LX board). Error status register bits 60 and 63 set.

Force PP BAS Input Data Parity Error (09)

This code inverts the parity bit for data transferred from the BAS Register to the DMA Array. A parity error occurs in the next clock period. Error status register bits 56 and 61 and operational status register bit 50 set.

Force DMA/IPI Input Data Parity Error Upper, Lower (0A, 0B)

These codes invert the parity bits for the upper and lower bytes of data transferred from the IPI Array to the DMA Array. A parity error occurs in the next clock period. Error status register bits 56 and 61 and operational status register bit 51 set.

Force Output Data Parity Error Upper, Lower (0C, 0D)

These codes invert the parity bits for the upper and lower bytes of data transferred from the DMA Array to the IPI Array or A/D. The DMA Array detects a parity error. Error status register bits 56 and 61 and operational status register bit 51 set.

Force Error Status Register Parity Error Upper, Lower (0E, 0F)

These codes invert the parity bits for the upper and lower bytes of the error status register. A parity error occurs when the PP reads the status. Error status register bit 61 sets. (PP must do a second read to detect this error.)

Force Channel Input Parity 0, 1 (10, 11)

These codes force the parity bit low for bits 48 through 55 (parity 0) and 56 through 63 (parity 1) as DMA input data enters the Assembly Buffer. A parity error occurs when the 64-bit CM word leaves the buffer. Error status register bits 59 and 62 set.

Force T Parity Low (12)

This code forces the parity bit low for T Register data as it enters the T Prime Register. A parity error occurs when T prime data transfers to the T Register. Error status register bit 62 sets. This error inhibits CM requests until the PP issues a clear T registers function or the adapter is master cleared.

Invert Output Parity Upper, Lower (13, 14)

These codes invert the parity bit for bits 48 through 55 (upper) and 56 through 63 (lower) as DMA output data leaves the Disassembly Buffer. Error status register bits 59 and 62 set.

Force Address Parity Prediction Error (15)

This code forces the real memory address parity predictor to predict the parity bit will change state on every CM reference. Error status register bit 62 sets. This error inhibits CM requests until the PP issues a clear T registers function or the adapter is master cleared.

Force Byte Count Equal to Zero (16)

This code forces the CM request counter to report an error after the PP issues 16 CM requests. This condition stimulates the constant CM request counter. Error status register bit 62 sets. This error inhibits CM requests until the PP issues a clear T registers function or the adapter is master cleared.

Force Control Register Parity Error (17)

This code inverts the parity bit for the control register. Error status register bits 56 and 61 and operational status register bit 49 set.

Force Deadman Timer Counter Parity Error (18)

This code forces a deadman timer counter parity error. Error status register bits 56 and 61 and operational status register bit 53 set.

OPERATIONAL STATUS REGISTER

This read-only register in the DMA Array provides information regarding the state of the adapter and IPI channel during DMA transfers. The PP reads this register through the Channel Data Bus using the 0700 function. This status allows the PP to control the operation of the adapter. MAC also reads this register through the MAC Mux. Bit assignments are described in the following paragraphs.

Parity Errors (48 through 53)

These bits indicate the parity checkers in the following registers/counters detected a parity error.

Bit	Description
48	Function Register
49	Control Register
50	Data Register Input
51	Data Register Output
52	T Register Counter
53	Deadman Timer Counter

DMA Transfer in Progress (56)

This bit indicates the JY or LZ buffers contain data.

IPI Transfer in Progress (57)

This bit indicates the IPI Array has not sent an inactive out signal to the DMA Array indicating completion of the data transfer.

Output Mode (58)

This bit indicates the A/D is in output mode. Data flow is from CM to the external device or PP. This bit sets during DMA to IPI (0D00) and DMA to PP (0400) functions.

DMA/IPI Mode (60)

This bit indicates a DMA/IPI data transfer is selected.

PP/IPI Moue (61)

This bit indicates a DMA operation is not in progress.

T Prime Register Empty (62)

This bit indicates the T Prime Register is empty and can be written by any of the following functions.

- Write T Prime Register (0B00)
- Select DMA to IPI (0D00)
- Select IPI to DMA (0C00)
- Select PP to DMA (0500)
- Select PP from DMA (0400)

Transfer in Progress (63)

This bit indicates the adapter issued a request to CM or IPI and did not receive a response. In DMA mode, this bit remains set during the entire transfer, provided the T register is nonzero and all outstanding requests have not been honored.

ERROR STATUS REGISTER

This read-only register in the DMA Array monitors the adapter´s error checking circuits to determine if any hardware errors have occurred. The PP reads this register through the Channel Data Bus. The PP uses this error status for fault isolation and to determine the validity of a transfer. All error bits are ORed to form the adapter´s error flag. This register is cleared by a master clear (0000) function or a clear error (0100) function. MAC also reads this register through the MAC Mux. Bit assignments are described in the following paragraphs.

Illegal Function of Sequence (49)

This bit indicates an illegal function or sequence of operation.

Uncorrectable CM Error (50)

This bit indicates an uncorrectable error response was received from CMI.

CM Reject (51)

This bit indicates a reject response was received from CMI.

Invalid Response (52)

This bit indicates the response code received from CMI decoded into an illegal value.

Response Code Parity Error (53)

This bit indicates a parity error was detected on the CM response code. If LX error (bit 63) is set, the parity error was detected on the LX board; if not set, the error was detected in CMI.

CMI Read Data Parity Error (54)

This bit indicates the CMI detected a read data parity error during a DMA output transfer.

IPI Error (55)

This bit indicates the IPI Array detected an error.

DMA Register Parity Error (56)

This bit indicates the DMA Array detected an error.

MAC Status Parity Error (57)

This bit indicates the LX board detected a parity error on status from the LZ board to the MAC Interface.

Timeout (58)

This bit sets when no activity is detected on the IPI channel for approximately one second after an I/O operation is starts. The timer starts after receiving an active signal from the PP. The active signal follows an IPI transfer function (XX81). When active, the full in or full out signal resets the timer.

A/D Data Error (59)

This bit indicates a parity error occurred during assembly/disassembly of CM data. The JY error (bit 62) also sets.

BAS Parity Error (60)

This bit indicates a parity error occurred in the output or function word received from the PP. The LX error (bit 63) also sets.

LZ Error (61)

This bit indicates the LZ board detected one of the following errors.

- IPI Input Data Error
- Input Buffer Data Error
- Overflow Error
- Output Buffer Data Error

JY Error (62)

This bit indicates the JY board detected an error. If bit 59 is also set, the error occurred during assembly/disassembly and the transfer continues. If bit 59 is not set, one of the following errors occurred.

- RMA Parity Predictor Error
- T Register Byte Count Parity Error
- Constant CM Request Error

These errors inhibit CM requests until the PP issues a clear T function or the adapter is master cleared.

LX Error (63)

This bit indicates the LX board detected one of the following errors.

- LX Response Code Parity Error
- BAS Parity Error
- MAC Parity Error

IPI ARRAY

The IPI Array transfers data between the external device and CMI through a 16-word buffer. It also contains the IPI status and error registers.

IPI STATUS REGISTER

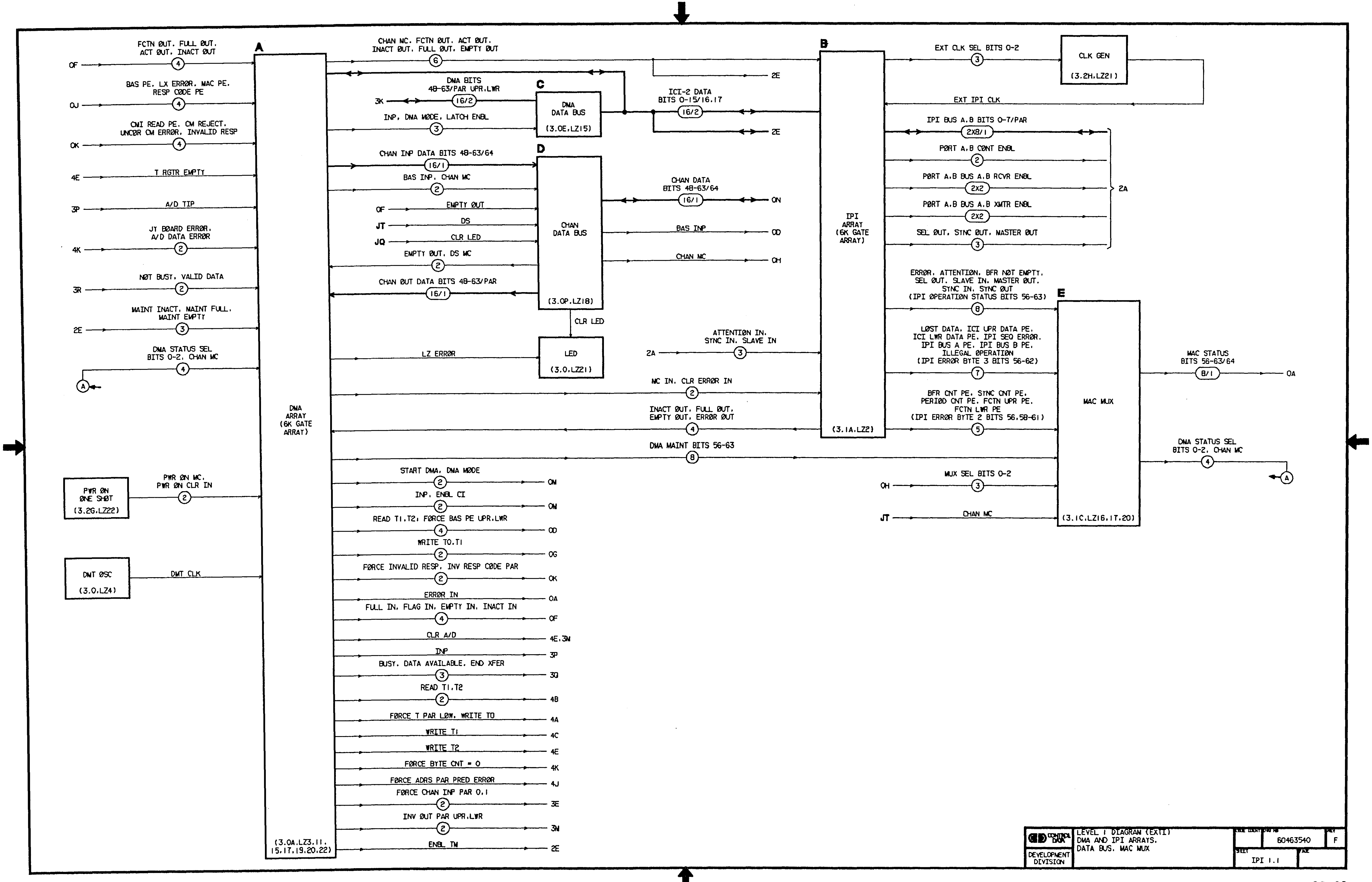
This read-only register in the IPI Array provides information regarding the state of the IPI channel to MAC through the MAC Mux during DMA transfers. Bit assignments are described below.

Bit	Status	Indication
48	Error	Any bit is set in IPI error register.
49	Attention	Attention in signal from external device is active.
50	Buffer Not Empty	Sixteen-word buffer is not empty.
51	Select Out	Select out signal to external device is active.
52	Slave In	Slave in signal from external device is active.
53	Master Out	Master out signal to external device is active.
54	Sync In	Sync in signal from external device is active.
55	Sync Out	Sync out signal to external device is active.
56-63	Not Used	Constant zeros.

IPI ERROR REGISTER

This read-only register monitors the IPI Array's error checking circuits during DMA transfers. Error information goes to MAC through the Mac Mux. Bit assignments are described below.

Bit	Error	Indication
48	Buffer Count Parity Error	Parity error or overflow/underflow in buffer counters.
49	Not Used	Constant zero.
50	Sync Count Parity Error	Parity error or overflow/underflow in sync in counter.
51	Period Count Parity Error	Parity error in sync period counter.
52	Function Upper Parity Error	Parity error in most significant byte of function word.
53	Function Lower Parity Error	Parity error in least significant byte of function word.
54, 55	Not Used	Constant zero.
56	Lost Data	External device (bus slave) terminated a data transfer and IPI interface buffer is not empty.
57	ICI Upper Data Parity Error	Parity error in most significant byte of data transferred on ICI.
58	ICI Lower Data Parity Error	Parity error in least significant byte of data transferred on ICI.
59	IPI Sequence Error	Illegal sequence of control signals in IPI Array.
60	IPI Bus A Parity Error	Parity error in bus A of IPI channel.
61	IPI Bus B Parity Error	Parity error in bus B of IPI channel.
62	Illegal Operation	Illegal function code from PP.
63	Not Used	Constant zero.


A
DMA ARRAY (6K GATE ARRAT)
(3.0A.LZ3.11.15.17.19.20.22)
OF
FCTN ØUT. FULL ØUT. ACT ØUT. INACT ØUT
4
OJ
BAS PE. LX ERRØR. MAC PE. RESP CØDE PE
4
OK
CMI READ PE. CM REJECT. UNCØR CM ERRØR. INVALID RESP
4
4E
T RGTR EMPTY
3P
A/D TIP
4K
JY BØARD ERRØR. A/D DATA ERRØR
2
3R
NØT BUSY. VALID DATA
2
2E
MAINT INACT. MAINT FULL. MAINT EMPTY
3
DMA STATUS SEL BITS 0-2. CHAN MC
4
A
PWR ØN ØNE SHØT (3.2G.LZ22)
PWR ØN MC. PWR ØN CLR IN
2
DMT ØSC (3.0.LZ4)
DMT CLK
CHAN MC. FCTN ØUT. ACT ØUT. INACT ØUT. FULL ØUT. EMPTY ØUT
6
2E
DMA BITS 48-63/PAR UPR.LWR
3K
16/2
INP. DMA MØDE. LATCH ENBL
3
C
DMA DATA BUS (3.0E.LZ15)
ICI-2 DATA BITS 0-15/16.17
16/2
2E
CHAN INP DATA BITS 48-63/64
16/1
BAS INP. CHAN MC
2
D
CHAN DATA BUS (3.0P.LZ18)
OF
EMPTY ØUT
JT
DS
JQ
CLR LED
EMPTY ØUT. DS MC
2
CHAN ØUT DATA BITS 48-63/PAR
16/1
CHAN DATA BITS 48-63/64
16/1
ON
BAS INP
OD
CHAN MC
OH
CLR LED
LED (3.0.LZ21)
LZ ERRØR
ATTENTIØN IN. SYNC IN. SLAVE IN
2A
3
MC IN. CLR ERRØR IN
2
INACT ØUT. FULL ØUT. EMPTY ØUT. ERRØR ØUT
4
DMA MAINT BITS 56-63
8
START DMA. DMA MØDE
2
OM
INP. ENBL CI
2
OM
READ T1.T2; FØRCE BAS PE UPR.LWR
4
OD
WRITE T0.T1
2
OG
FØRCE INVALID RESP. INV RESP CØDE PAR
2
OK
ERRØR IN
OA
FULL IN. FLAG IN. EMPTY IN. INACT IN
4
OF
CLR A/D
4E.3M
INP
3P
BUSY. DATA AVAILABLE. END XFER
3
3Q
READ T1.T2
2
4B
FØRCE T PAR LØW. WRITE T0
4A
WRITE T1
4C
WRITE T2
4E
FØRCE BYTE CNT = 0
4K
FØRCE ADRS PAR PRED ERRØR
4J
FØRCE CHAN INP PAR 0.1
2
3E
INV ØUT PAR UPR.LWR
2
3M
ENBL TM
2E
B
IPI ARRAY (6K GATE ARRAY) (3.1A.LZ2)
EXT CLK SEL BITS 0-2
3
CLK GEN (3.2H.LZ21)
EXT IPI CLK
IPI BUS A.B BITS 0-7/PAR
2X8/1
PØRT A.B CØNT ENBL
2
PØRT A.B BUS A.B RCVR ENBL
2X2
PØRT A.B BUS A.B XMTR ENBL
2X2
SEL ØUT. SYNC ØUT. MASTER ØUT
3
2A
ERRØR. ATTENTIØN. BFR NØT EMPTY. SEL ØUT. SLAVE IN. MASTER ØUT. SYNC IN. SYNC ØUT (IPI ØPERATIØN STATUS BITS 56-63)
8
E
MAC MUX (3.1C.LZ16.1T.20)
LØST DATA. ICI UPR DATA PE. ICI LWR DATA PE. IPI SEQ ERRØR. IPI BUS A PE. IPI BUS B PE. ILLEGAL ØPERATIØN (IPI ERRØR BYTE 3 BITS 56-62)
7
BFR CNT PE. SYNC CNT PE. PERIØD CNT PE. FCTN UPR PE. FCTN LWR PE (IPI ERRØR BYTE 2 BITS 56.58-61)
5
MAC STATUS BITS 56-63/64
8/1
OA
DMA STATUS SEL BITS 0-2. CHAN MC
4
A
OH
MUX SEL BITS 0-2
3
JT
CHAN MC

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 1 DIAGRAM (EXT)
DMA AND IPI ARRAYS.
DATA BUS. MAC MUX

60463540 | F
IPI 1.1

IPI DATA OUT MUX, RANDOM DATA GENERATOR, TRANSMITTERS, RECEIVERS (IPI 1.2)

DATA PATHS

The following paragraphs describe data flow through the IPI Data Out Mux, Random Data Generator, and IPI Ports A, B Transmitters/Receivers.

PP AND DMA OUTPUT TRANSFERS

1. IPI bus data from the IPI Array (1.1B) goes to the IPI Data Out Mux.
2. Bus out data from the IPI Data Out Mux goes to the external device through the transmitters.

PP AND DMA INPUT TRANSFERS

Bus data from the external device goes to the IPI Array through the receivers.

TEST MODE DATA PATHS

The following paragraphs describe data flow when the adapter is in test mode.

PP AND DMA OUTPUT TRANSFERS

1. A block of words (IPI bus data) goes from the IPI Array to the IPI Data Out Mux.
2. Bus out data goes from the IPI Data Out Mux to the Random Data Generator.
3. Result sum (ICC-2 data) goes from the Random Data Generator to the DMA Array (1.1A).

PP AND DMA INPUT TRANSFERS

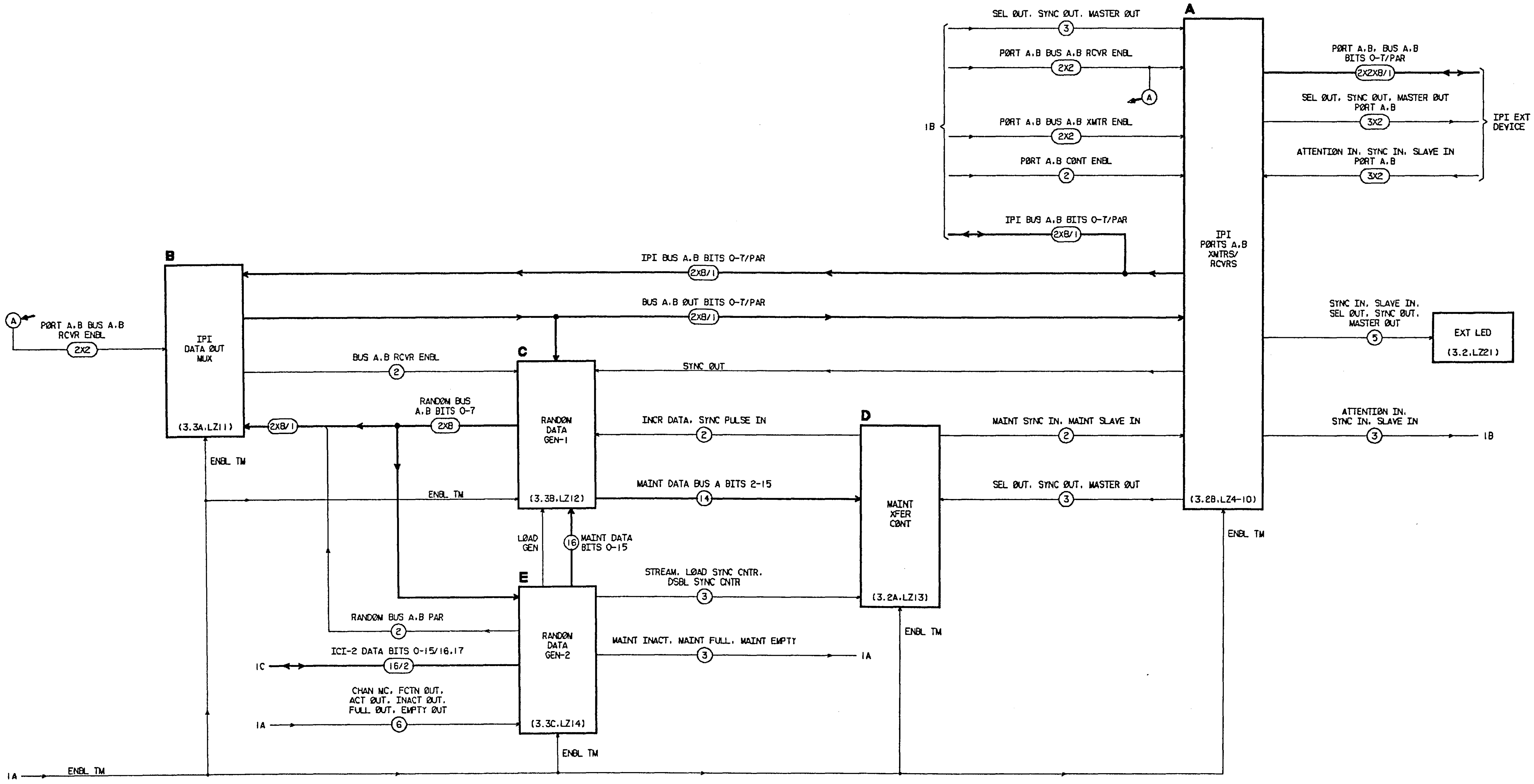
1. A block of words (random bus data) from the Random Data Generator goes to the IPI Data Out Mux.
2. Bus out data from the IPI Data Out Mux goes to the IPI Array through the transmitters/receivers.

RANDOM DATA GENERATOR

In test mode, the PP directs the Random Data Generator to emulate the external device. Test mode allows testing the adapter´s internal data paths without an external device. This generator supplies random data for input transfers and produces a check sum for output transfers.

MAINTENANCE TRANSFER CONTROL

In test mode, this circuit controls the Random Data Generator. Together, the Maintenance Transfer Control and the Random Data Generator emulate the external device. These circuits allow the PP to test the adapter when the external device is inoperative or not present.


A
IPI PORTS A,B XMTRS/ RCVRS
(3.2B,LZ4-10)
SEL OUT, SYNC OUT, MASTER OUT
3
PORT A,B BUS A,B RCVR ENBL
2X2
A
PORT A,B BUS A,B XMTR ENBL
2X2
PORT A,B CONT ENBL
2
IPI BUS A,B BITS 0-7/PAR
2X8/1
1B
PORT A,B, BUS A,B BITS 0-7/PAR
2X2X8/1
SEL OUT, SYNC OUT, MASTER OUT PORT A,B
3X2
ATTENTION IN, SYNC IN, SLAVE IN PORT A,B
3X2
IPI EXT DEVICE
SYNC IN, SLAVE IN, SEL OUT, SYNC OUT, MASTER OUT
5
EXT LED
(3.2,LZ21)
ATTENTION IN, SYNC IN, SLAVE IN
3
1B
ENBL TM
B
IPI DATA OUT MUX
(3.3A,LZ11)
A
PORT A,B BUS A,B RCVR ENBL
2X2
IPI BUS A,B BITS 0-7/PAR
2X8/1
BUS A,B OUT BITS 0-7/PAR
2X8/1
BUS A,B RCVR ENBL
2
SYNC OUT
C
RANDOM DATA GEN-1
(3.3B,LZ12)
RANDOM BUS A,B BITS 0-7
2X8
2X8/1
ENBL TM
ENBL TM
INCR DATA, SYNC PULSE IN
2
MAINT DATA BUS A BITS 2-15
14
D
MAINT XFER CONT
(3.2A,LZ13)
MAINT SYNC IN, MAINT SLAVE IN
2
SEL OUT, SYNC OUT, MASTER OUT
3
ENBL TM
LOAD GEN
16
MAINT DATA BITS 0-15
E
RANDOM DATA GEN-2
(3.3C,LZ14)
STREAM, LOAD SYNC CNTR, DSBL SYNC CNTR
3
MAINT INACT, MAINT FULL, MAINT EMPTY
3
1A
RANDOM BUS A,B PAR
2
ICI-2 DATA BITS 0-15/16,17
16/2
1C
CHAN MC, FCTN OUT, ACT OUT, INACT OUT, FULL OUT, EMPTY OUT
6
1A
ENBL TM
1A
ENBL TM

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL I DIAGRAM (EXTI)
IPI DATA OUT MUX, RANDOM
DATA GEN, XMTRS/RCVRS

CODE IDENT	DWG NO	REV
	60463540	D

SHEET	PAGE
IPI 1.2	

ASSEMBLY/DISASSEMBLY, CONTROL COUNTERS (IPI 1.3)

This diagram shows the data paths from EXTI to CM through the Assembly Buffer and from CM to EXTI through the Disassembly Buffer.

ASSEMBLY

The adapter assembles 16-bit channel words into 64-bit CM words during DMA input transfers as follows.

1. External device sends channel words to input buffer in IPI Array (1.1B).
2. T Register Byte Count (1.4A) decrements by two for every 16-bit CM word parcel.
3. Assembly Buffer assembles four 16-bit parcels into a 64-bit CM word.
4. Assembly Buffer Output Register sends 64-bit word to CM.
5. T Register RMA (1.4C,F) increments by eight to set up next CM address.
6. DMA input transfer terminates when T Register Byte Count equals zero or if external device sends an inactive in.

DISASSEMBLY

The adapter disassembles 64-bit CM words into 16-bit channel words during DMA output transfers as follows.

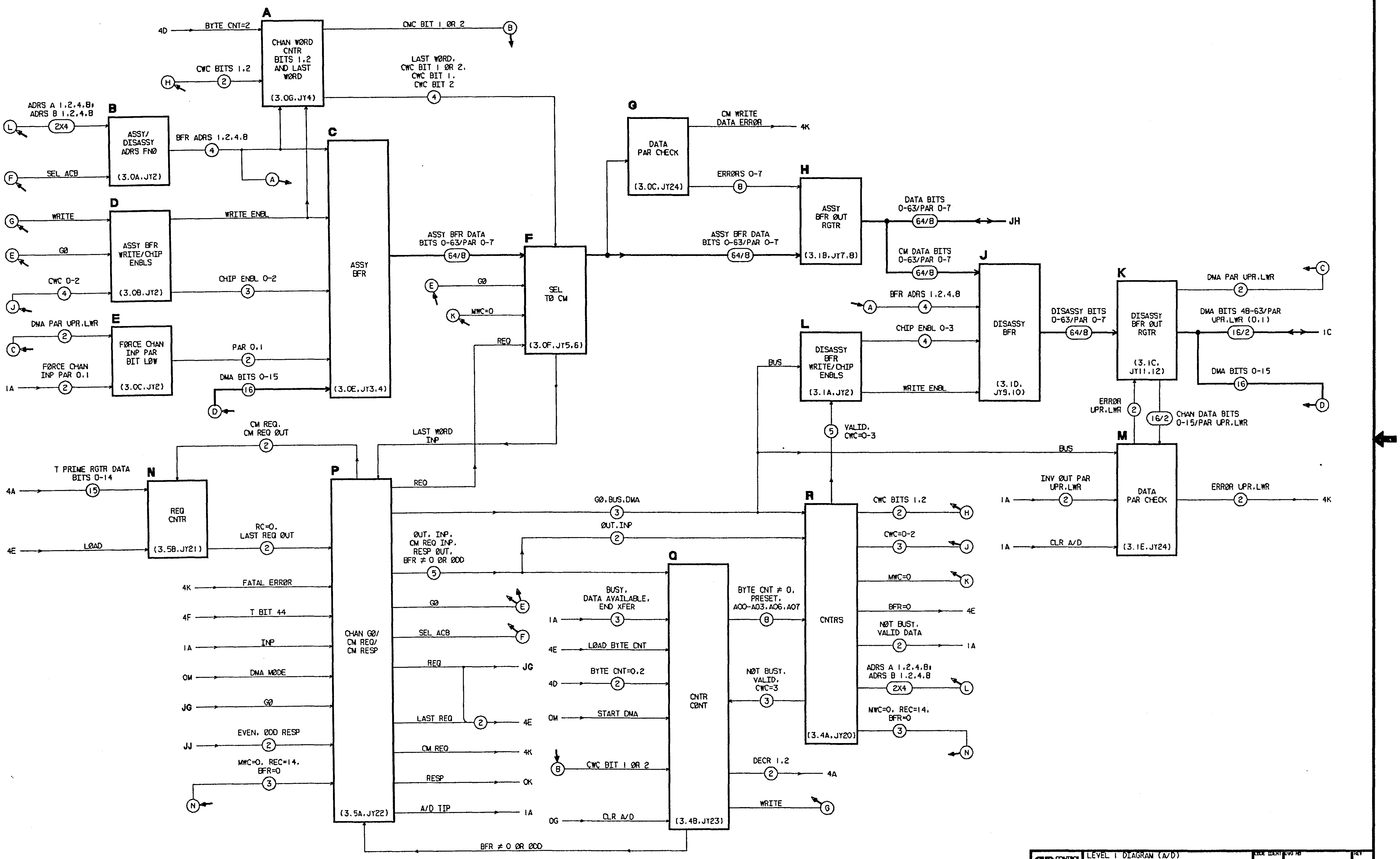
1. CM sends word to Disassembly Buffer.
2. T Register RMA (1.4C,F) increments by eight to set up next CM address.
3. Disassembly Buffer Output Register sends disassembled 16-bit word parcels to output buffer in IPI Array (1.1B).
4. T Register Byte Count (1.4A) decrements by two for every 16-bit word parcel.
5. Output buffer in IPI Array sends channel words to external device.
6. DMA output transfer terminates when T Register Byte Count equals zero or if external device sends an inactive in.

COUNTERS

The Counters keep track of the number of 16-bit words that are being processed by the assembly/disassembly circuits.

CHANNEL GO/CM REQUEST/CM RESPONSE

These circuits coordinate the DMA assembly/disassembly operations with the CM requests and responses.



CONTROL DATA	LEVEL 1 DIAGRAM (A/D) ASSEMBLY, DISASSEMBLY, CONTROL COUNTERS
DEVELOPMENT DIVISION	
DWG NO	60463540
REV	F
SHEET	IPI 1.3

This diagram shows the CM address path for DMA transfers and an Error Fan-In which detects JY board errors.

T REGISTER

The T Register receives the 16-bit byte count and the 32-bit real memory address (RMA) from the T Prime Register. The least significant bit of the byte count, the most significant bit of RMA, and the three least significant bits of RMA are not used. These unused bits are always zero. The PP must load the T Register through the T Prime Register before a DMA transfer may proceed.

The 15-bit byte count decrements by two as every 16-bit word enters the Assembly Buffer (1.3C, DMA input) or leaves the Disassembly Buffer (1.3J, DMA output). The 28-bit RMA increments by eight after every CM reference.

The PP may read the 48-bit T Register by issuing a read T function, activating the adapter, inputting three 16-bit words, and deactivating the adapter.

T PRIME REGISTER

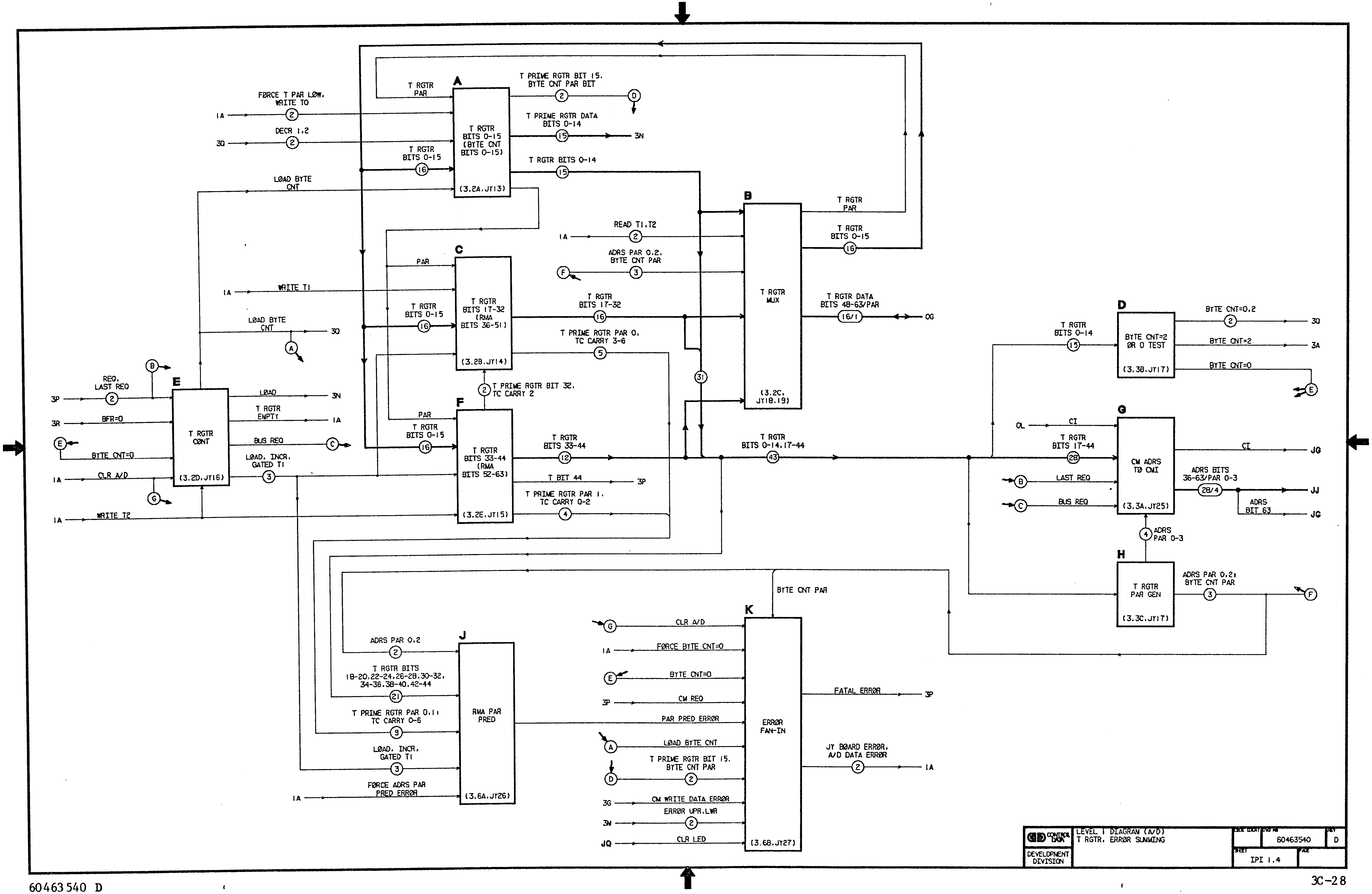
The T Prime Register receives the 16-bit byte count and the 32-bit RMA from the PP. When the T Register is empty (status bit 62), the PP may write the 48-bit T Prime Register by issuing a write T function, activating the adapter, outputting three 16-bit words, and deactivating the adapter. All three words must be written. The PP cannot read this register.

When the T Prime Register is full, the contents transfer to the T Register as follows.

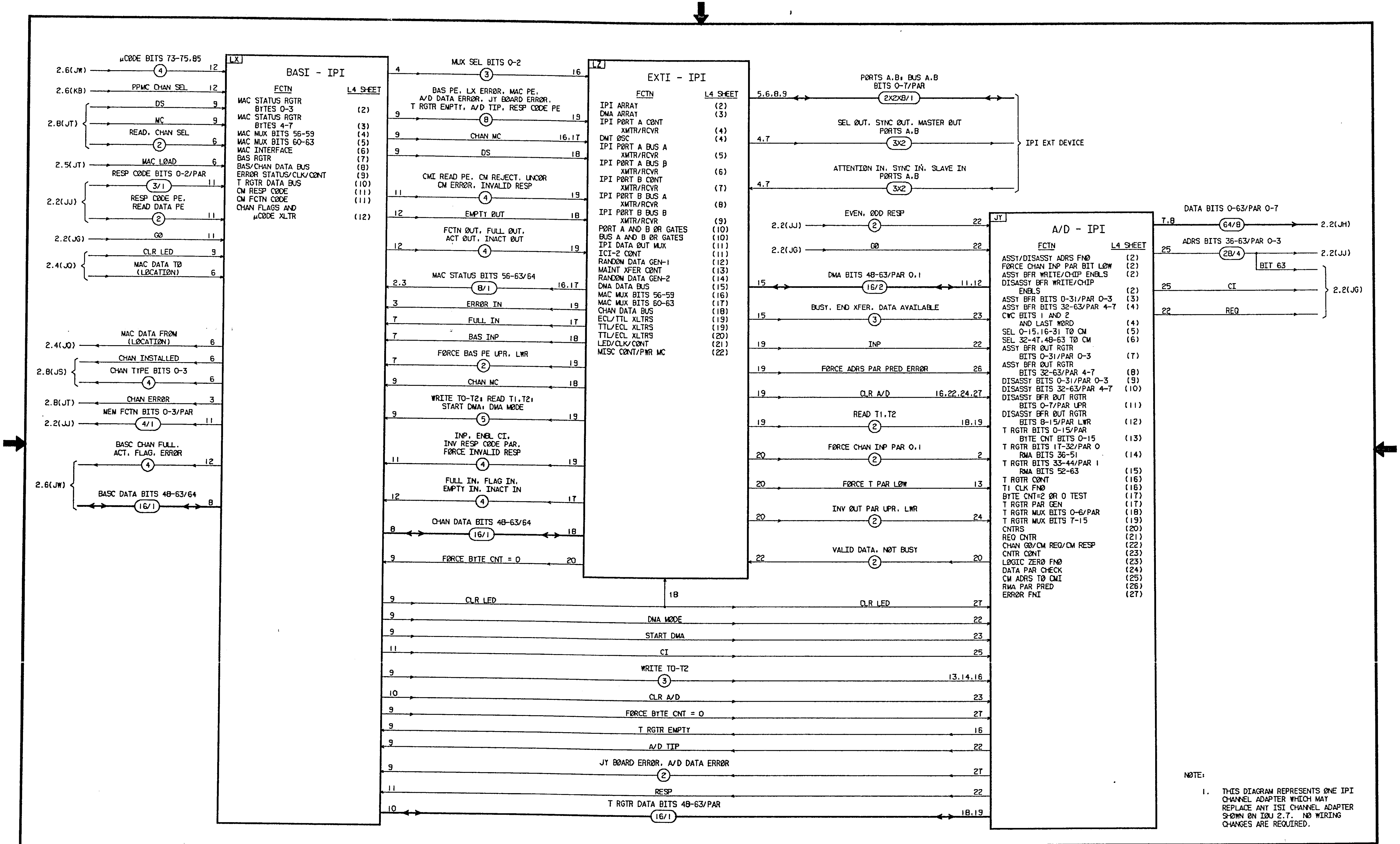
- If DMA transfer is not in progress, T Register Byte Count is zero, and Assembly Buffer or Disassembly Buffer is empty, all 48 bits transfer and bit 62 sets in the operational status register (1.1A, DMA Array).
- If DMA transfer is in progress and T Register Byte Count is zero, the 16-bit byte count transfers. During DMA output transfers, bit 62 sets in the operational status register.
- If DMA transfer is in progress and last CM reference occurs, the 32-bit RMA transfers. During DMA input transfers, bit 62 sets in the operational status register.

CM ADDRESS TO CMI

This circuit sends the RMA from the T Register to CMI during a DMA transfer. The circuit also sends Cache Invalidate to CMI on every fourth and last CM write if bit 48 is set in the control register (1.1A, DMA Array).



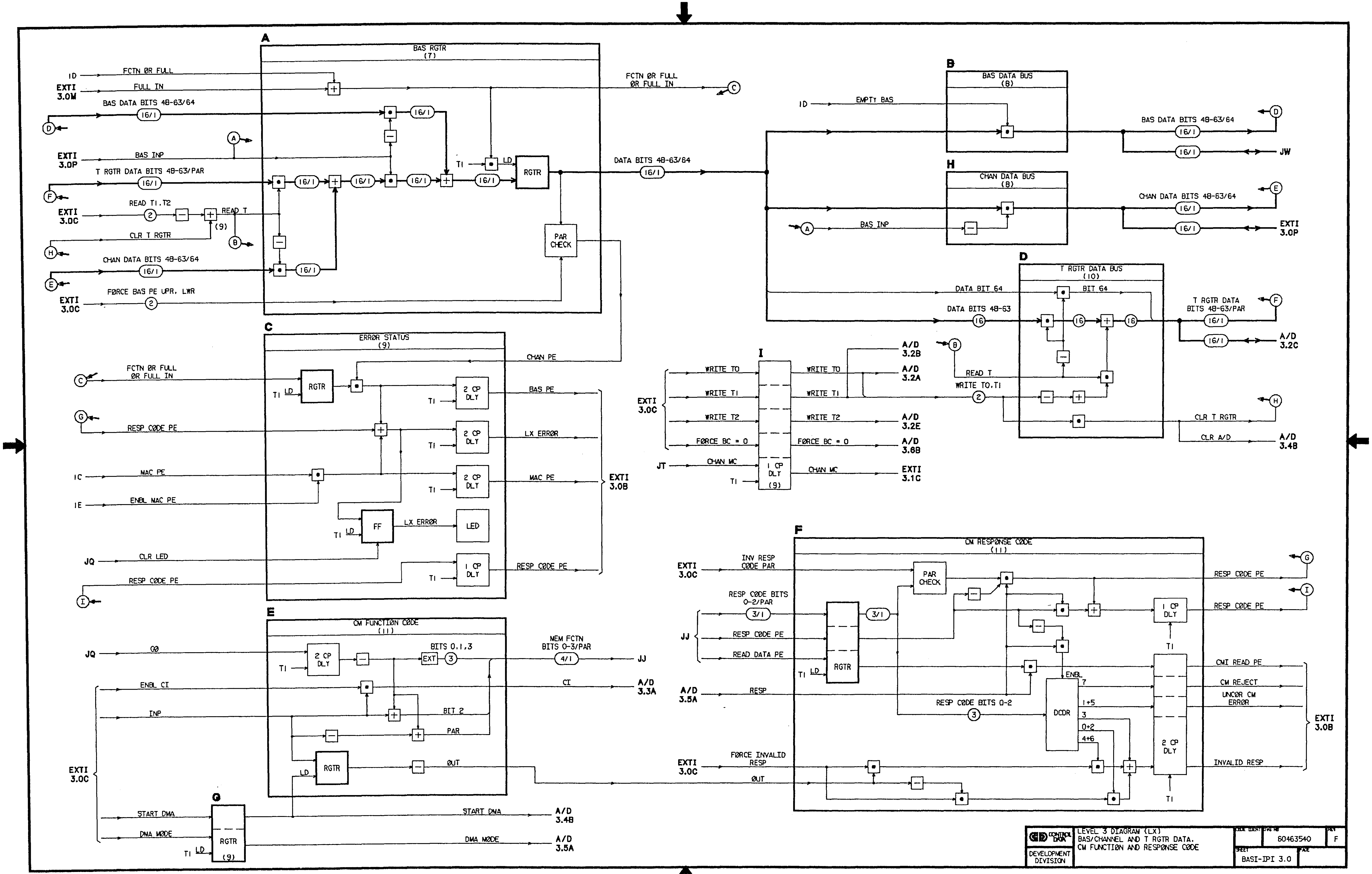
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 1 DIAGRAM (A/D)
T RGTR. ERROR SUMMING
CODE IDENT
DWG NO 60463540
REV D
SHEET IPI 1.4
PAGE

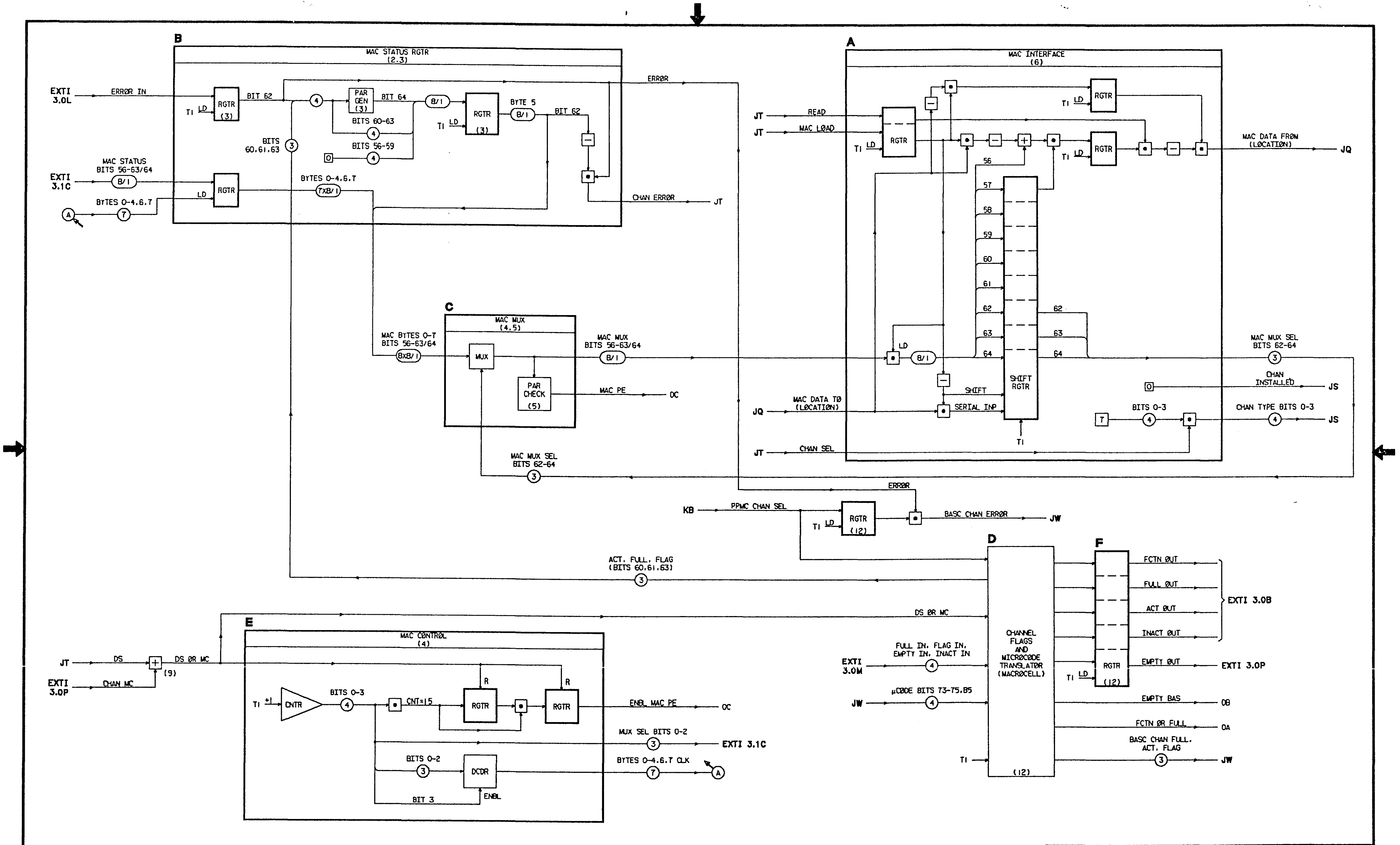


NOTE:

1. THIS DIAGRAM REPRESENTS ONE IPI CHANNEL ADAPTER WHICH MAY REPLACE ANY ISI CHANNEL ADAPTER SHOWN ON IOU 2.7. NO WIRING CHANGES ARE REQUIRED.

CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
DMA ENHANCED IPI
CHANNEL ADAPTER
60463540
F
SHEET IPI 2.0


A
BAS RGTR (7)
ID
FCTN ØR FULL
EXTI 3.0M
FULL IN
BAS DATA BITS 48-63/64
16/1
D
A
EXTI 3.0P
BAS INP
T RGTR DATA BITS 48-63/PAR
F
EXTI 3.0C
READ T1,T2
2
READ T
(9)
CLR T RGTR
H
B
CHAN DATA BITS 48-63/64
E
FØRCE BAS PE UPR, LWR
TI
LD
RGTR
PAR CHECK
FCTN ØR FULL ØR FULL IN
C
DATA BITS 48-63/64
B
BAS DATA BUS (8)
EMPTY BAS
BAS DATA BITS 48-63/64
JW
H
CHAN DATA BUS (8)
CHAN DATA BITS 48-63/64
EXTI 3.0P
BAS INP
D
T RGTR DATA BUS (10)
DATA BIT 64
BIT 64
DATA BITS 48-63
16
T RGTR DATA BITS 48-63/PAR
A/D 3.2C
READ T
WRITE T0,T1
CLR T RGTR
CLR A/D
A/D 3.4B
C
ERRØR STATUS (9)
CHAN PE
FCTN ØR FULL ØR FULL IN
G
RESP CØDE PE
IC
MAC PE
IE
ENBL MAC PE
JQ
CLR LED
RESP CØDE PE
I
2 CP DLY
1 CP DLY
FF
LX ERRØR
LED
BAS PE
LX ERRØR
MAC PE
RESP CØDE PE
EXTI 3.0B
I
EXTI 3.0C
WRITE T0
WRITE T1
WRITE T2
FØRCE BC = 0
JT
CHAN MC
1 CP DLY (9)
A/D 3.2B
A/D 3.2A
A/D 3.2E
A/D 3.6B
EXTI 3.1C
E
CM FUNCTIØN CØDE (11)
JQ
GØ
ENBL CI
INP
BITS 0,1,3
EXT
3
BIT 2
PAR
ØUT
NEW FCTN BITS 0-3/PAR
4/1
JJ
CI
A/D 3.3A
EXTI 3.0C
G
START DMA
DMA MØDE
RGTR (9)
A/D 3.4B
A/D 3.5A
F
CM RESPØNSE CØDE (11)
EXTI 3.0C
INV RESP CØDE PAR
RESP CØDE BITS 0-2/PAR
3/1
JJ
RESP CØDE PE
READ DATA PE
A/D 3.5A
RESP
RESP CØDE BITS 0-2
DCDR
ENBL
7
1+5
3
0+2
4+6
FØRCE INVALID RESP
ØUT
RESP CØDE PE
CMI READ PE
CM REJECT
UNCØR CM ERRØR
INVALID RESP
EXTI 3.0B
CONTROL DATA
DEVELOPMENT DIVISION
LEVEL 3 DIAGRAM (LX)
BAS/CHANNEL AND T RGTR DATA.
CM FUNCTIØN AND RESPØNSE CØDE
60463540
F
BASI-IPI 3.0



CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (LX)
MAC INTERFACE.
CHANNEL FLAGS

12-10-87

CODE IDENT | DWG NO 60463540 | REV D

SHEET BASI-IPI 3.1 | PAGE

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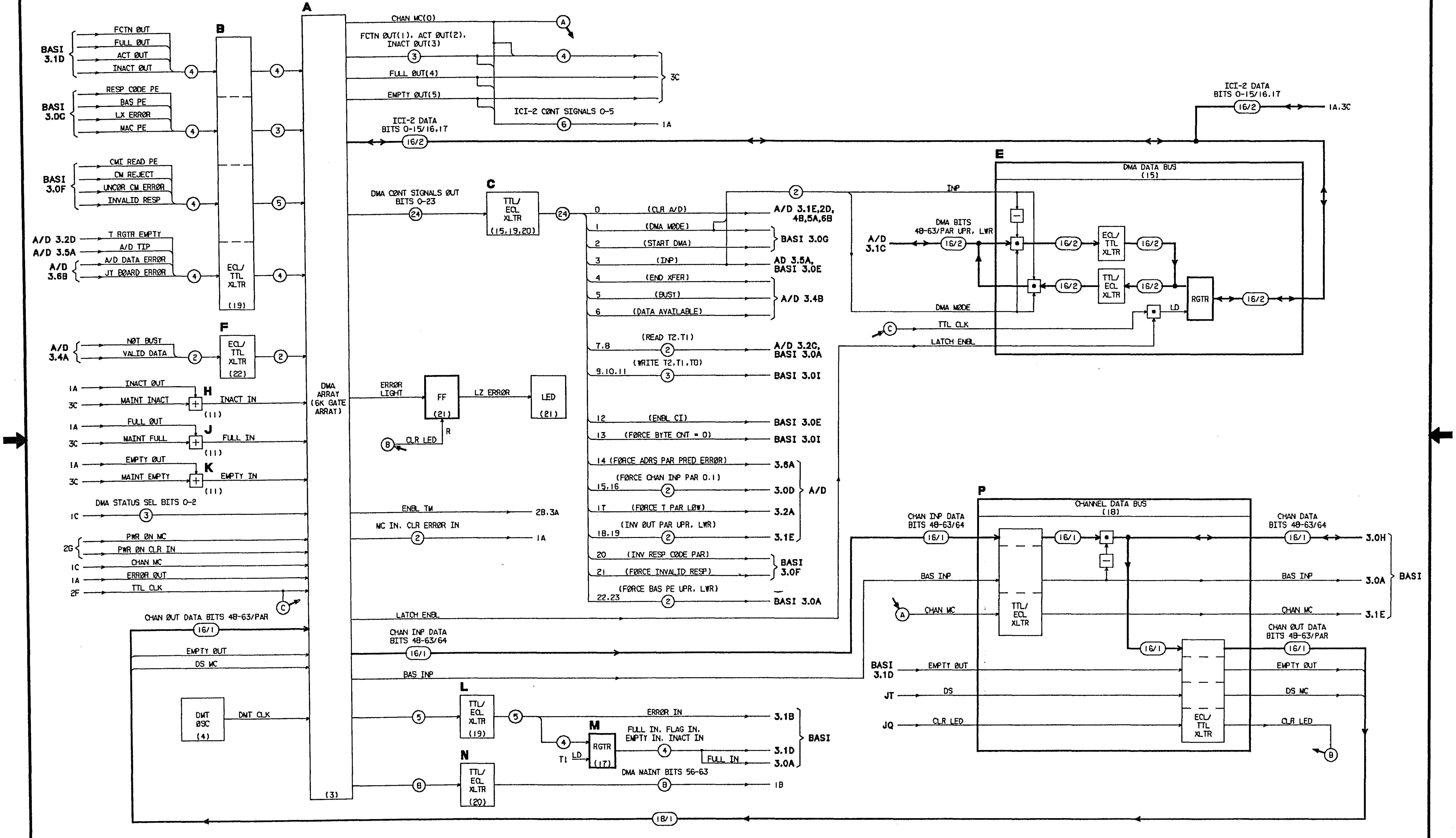

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (LZ)
DMA ARRAY AND DATA BUS,
CHANNEL DATA BUS

CODE IDENT
DWG NO 60463540
REV F
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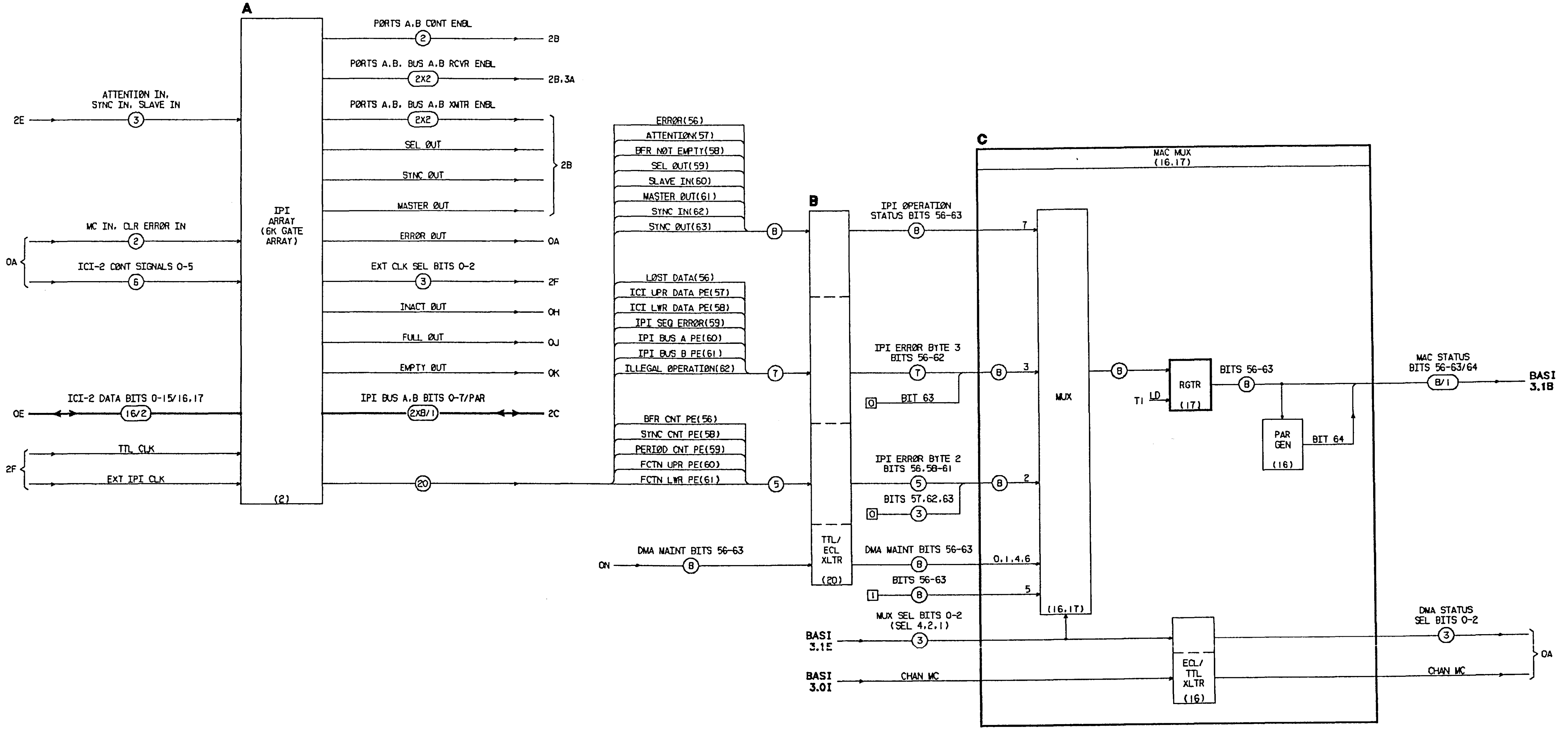

CONTROL DATA
DEVELOPMENT
DIVISION

LEVEL 3 DIAGRAM (LZ)
IPI ARRAY, MAC MUX

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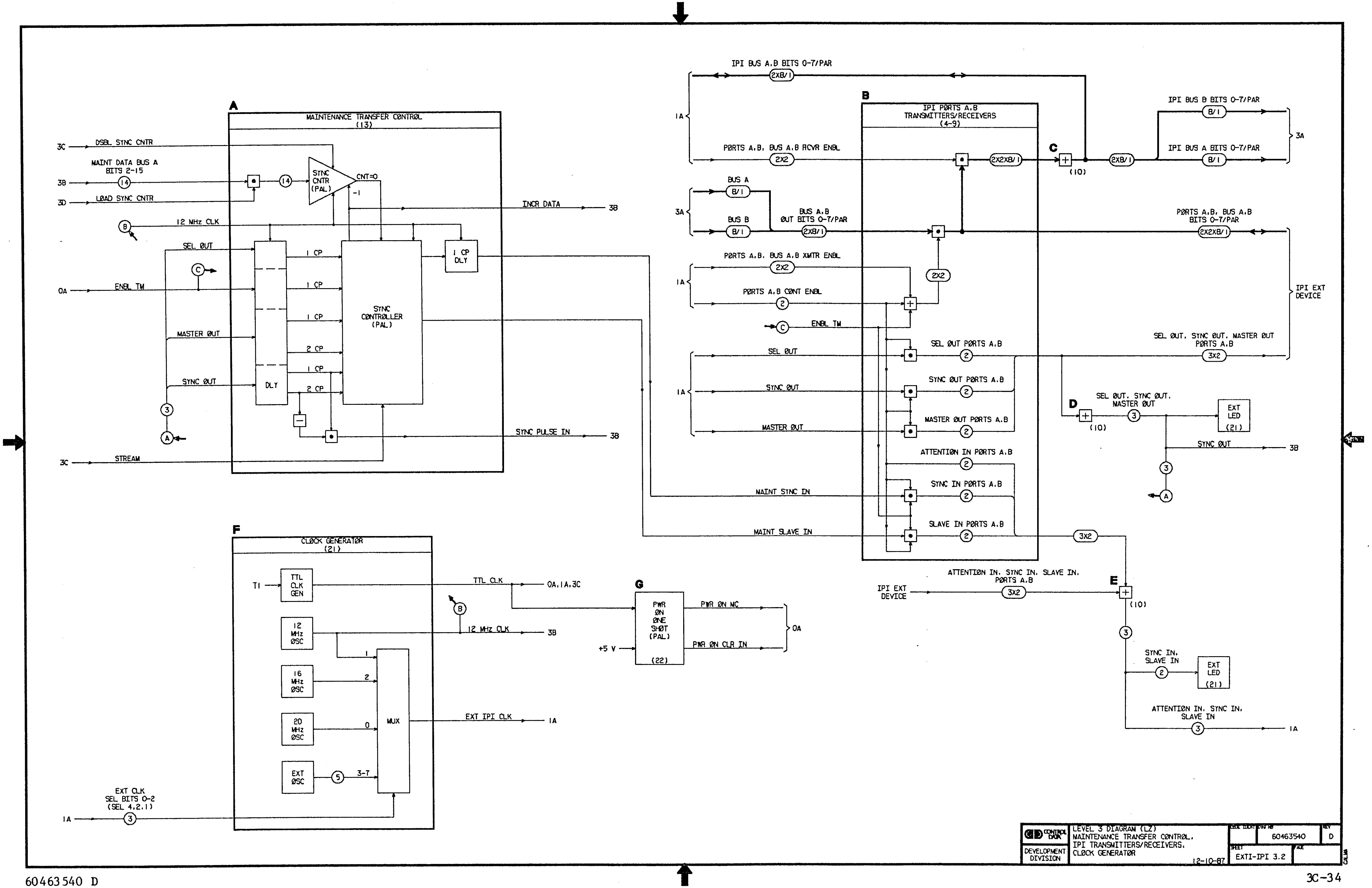


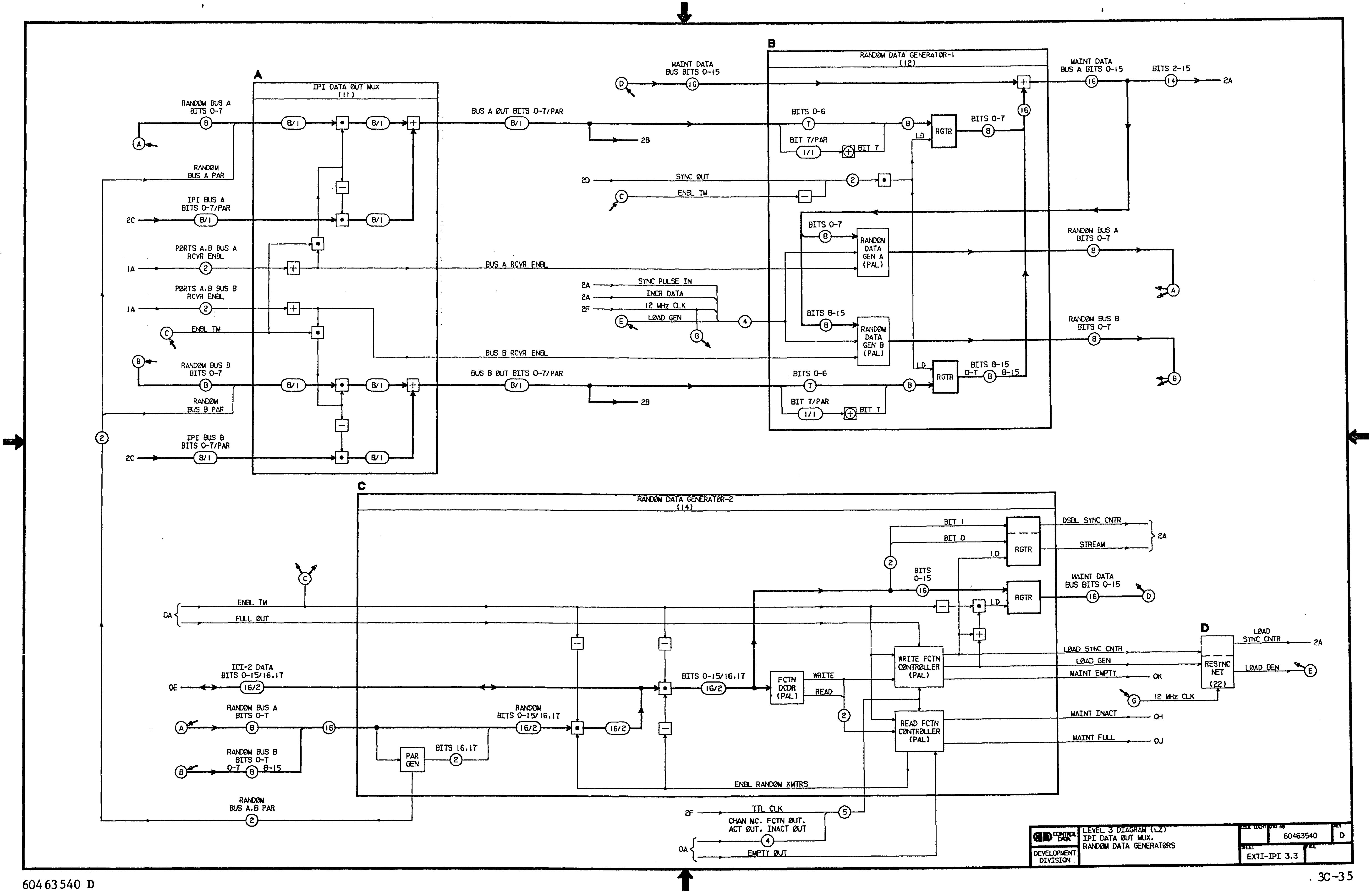
CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (LZ)
MAINTENANCE TRANSFER CONTROL,
IPI TRANSMITTERS/RECEIVERS,
CLOCK GENERATOR
12-10-87

60463540 D

EXTI-IPI 3.2



CONTROL DATA

DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (LZ)
IPI DATA ØUT MUX.
RANDØM DATA GENERATØRS

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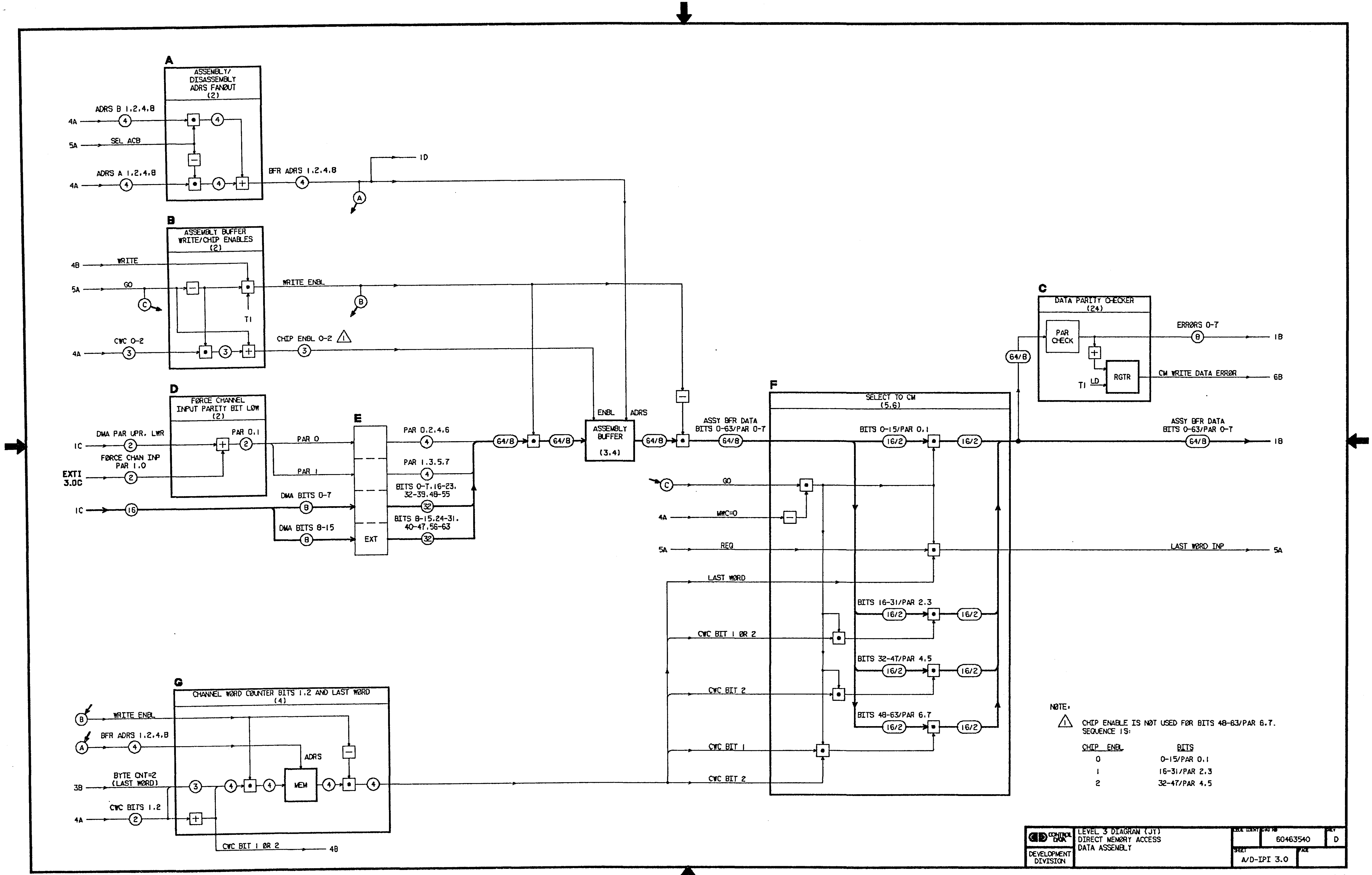
EXTI-IPI 3.3



NØTE:

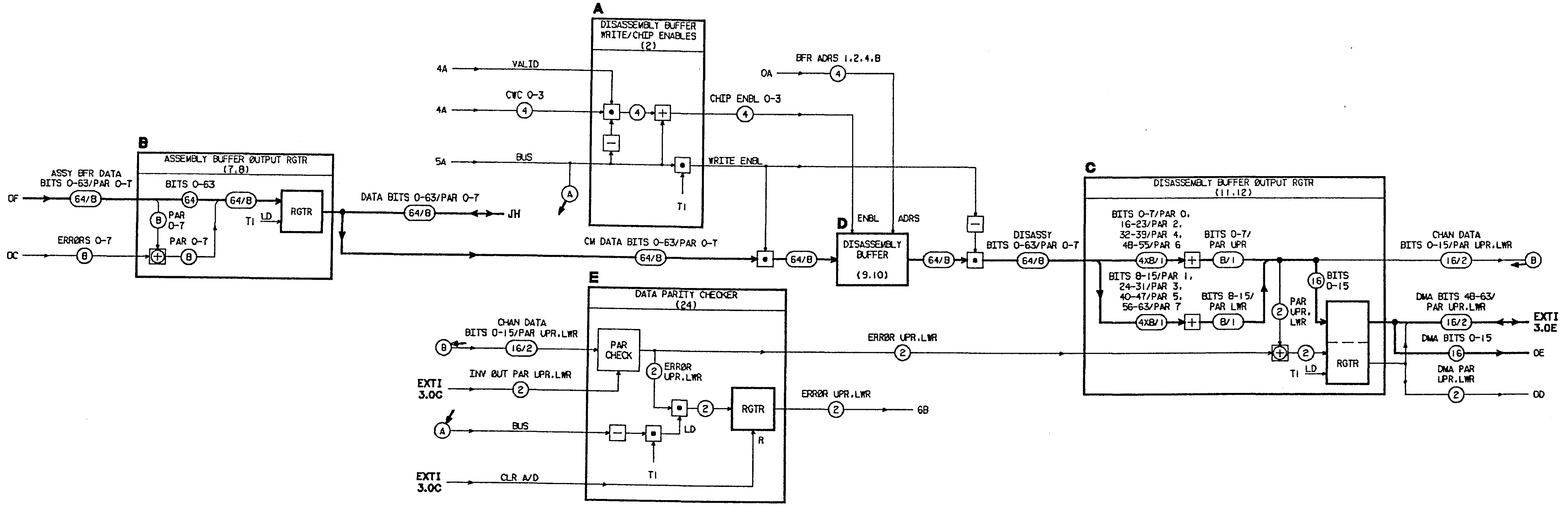
⚠ CHIP ENABLE IS NØT USED FØR BITS 48-63/PAR 6,7. SEQUENCE IS:

CHIP ENBL	BITS
0	0-15/PAR 0,1
1	16-31/PAR 2,3
2	32-47/PAR 4,5

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
DIRECT MEMØRY ACCESS
DATA ASSEMBLY

CODE IDENT / DWG NO 60463540
REV D
SHEET A/D-IPI 3.0
PAGE



NØTE:

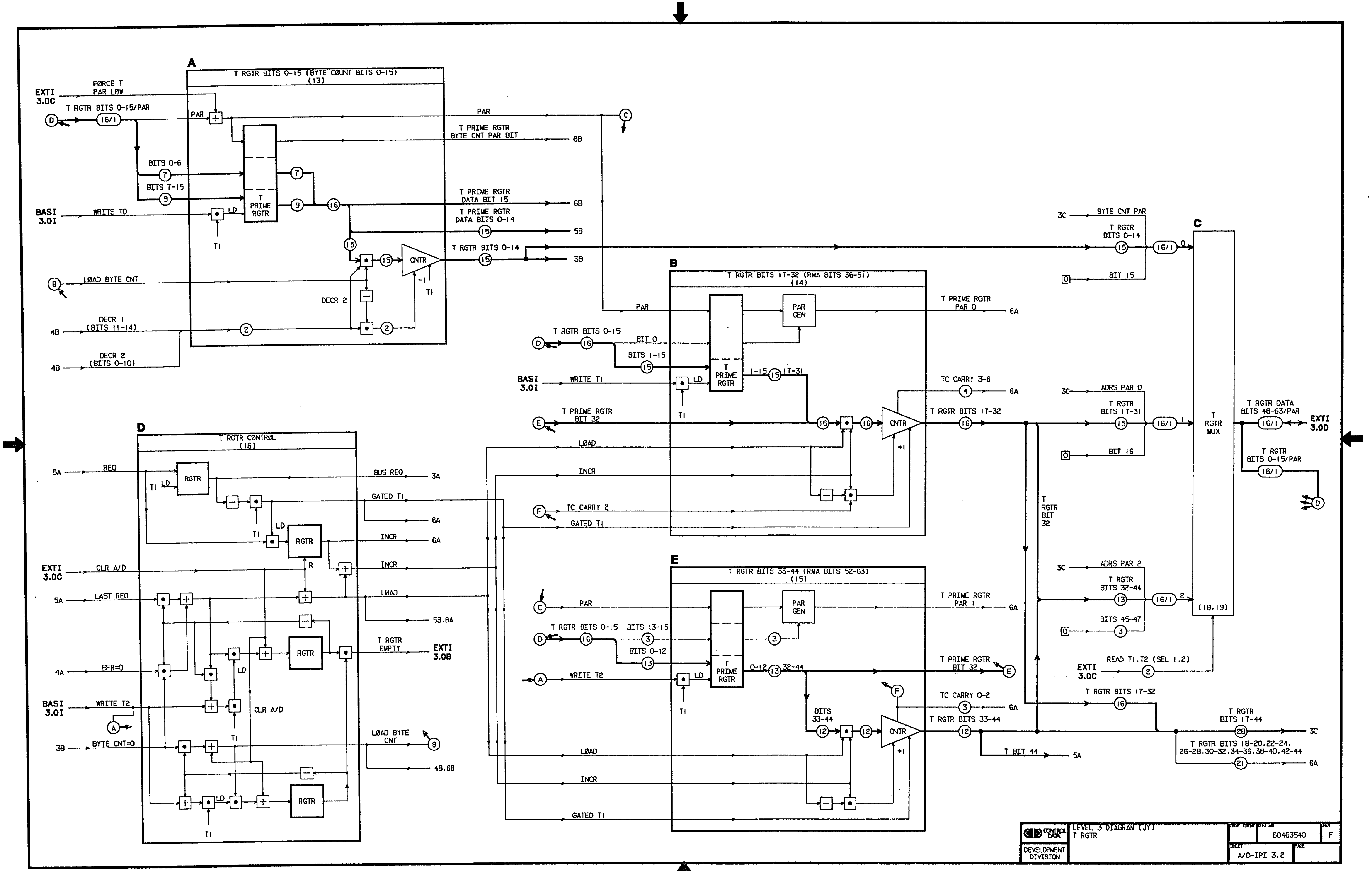
⚠ CHIP ENABLE SEQUENCE IS:

CHIP ENBL	BITS
0	0-15/PAR 0,1
1	16-31/PAR 2,3
2	32-47/PAR 4,5
3	48-63/PAR 6,7

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
CM DATA DISASSEMBLY

CODE IDENT
DWG NO 60463540
REV D
SHEET A/D-IPI 3.1
PAGE



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
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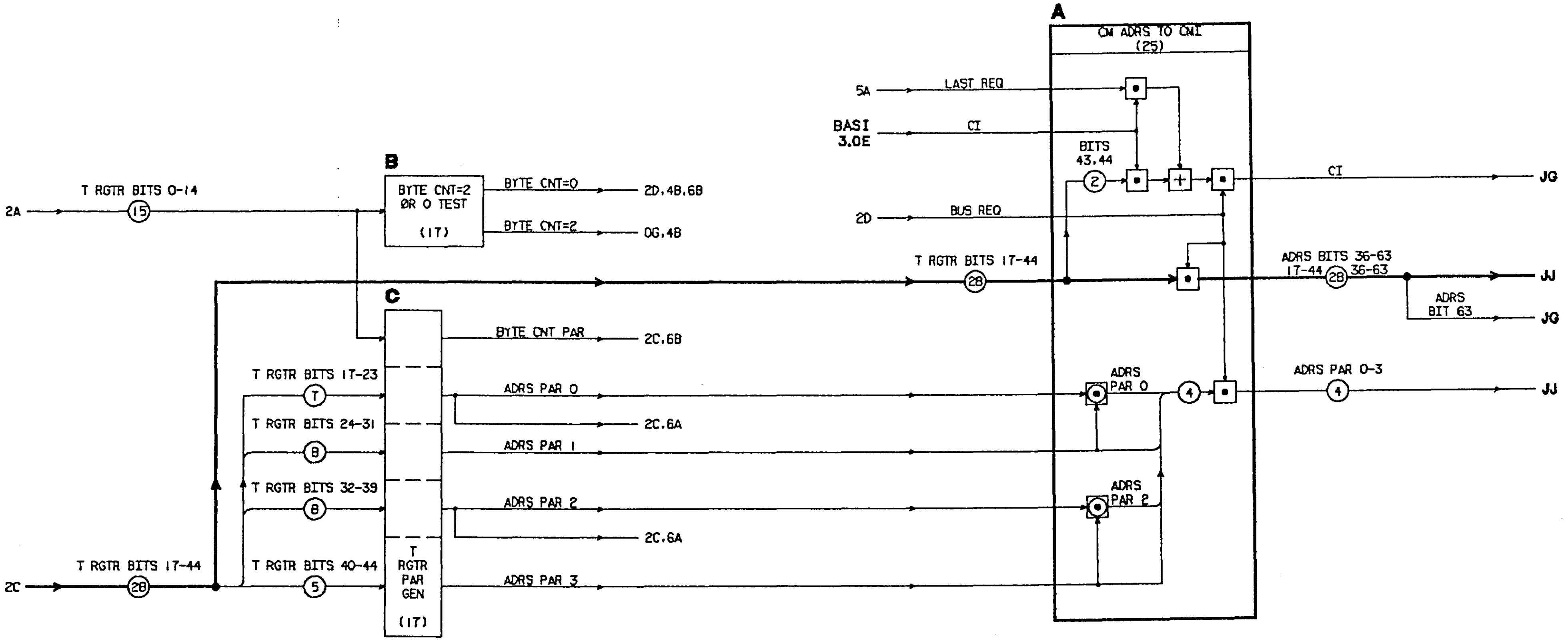

CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
CM ADRS TØ CMI

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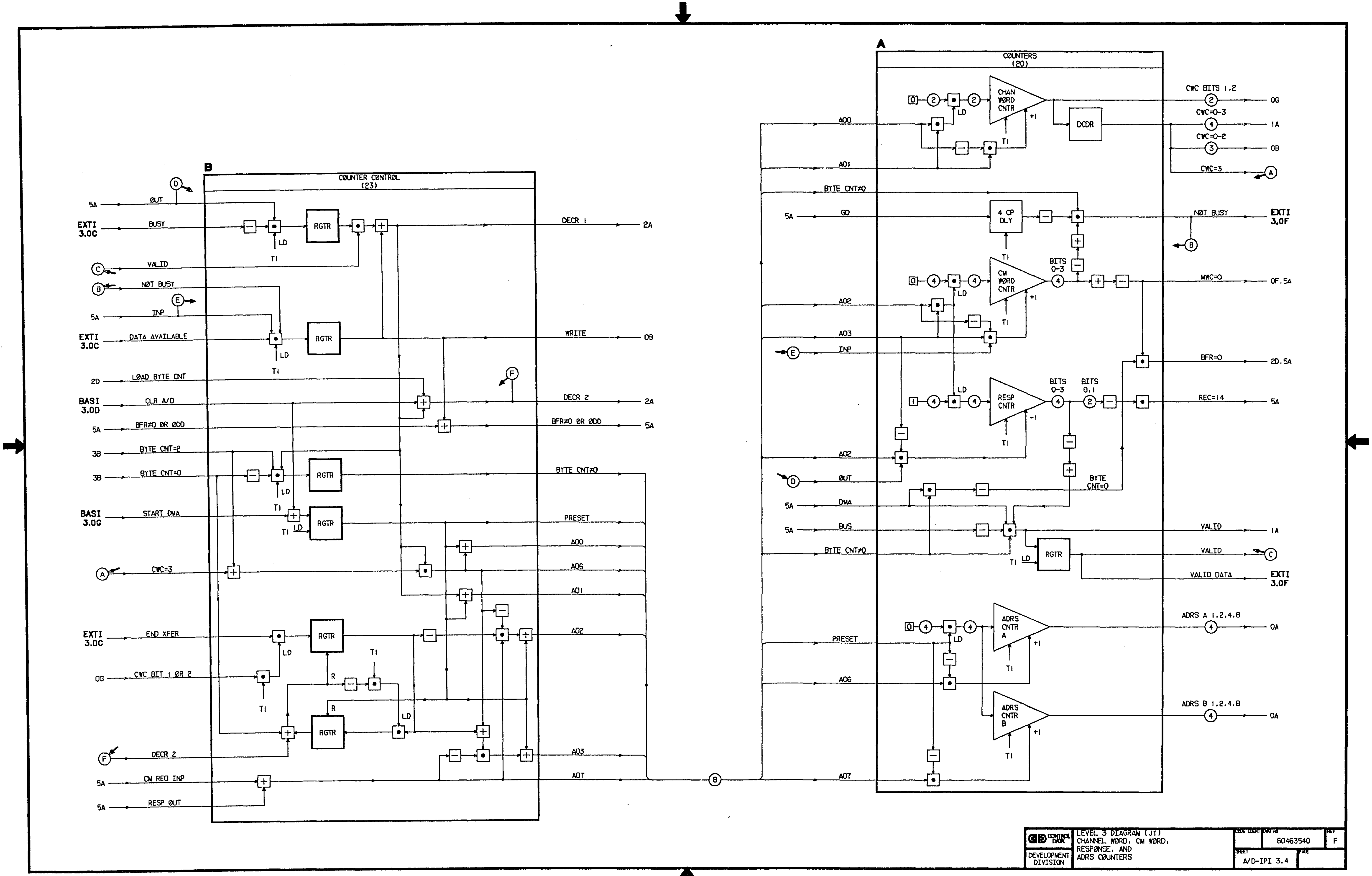
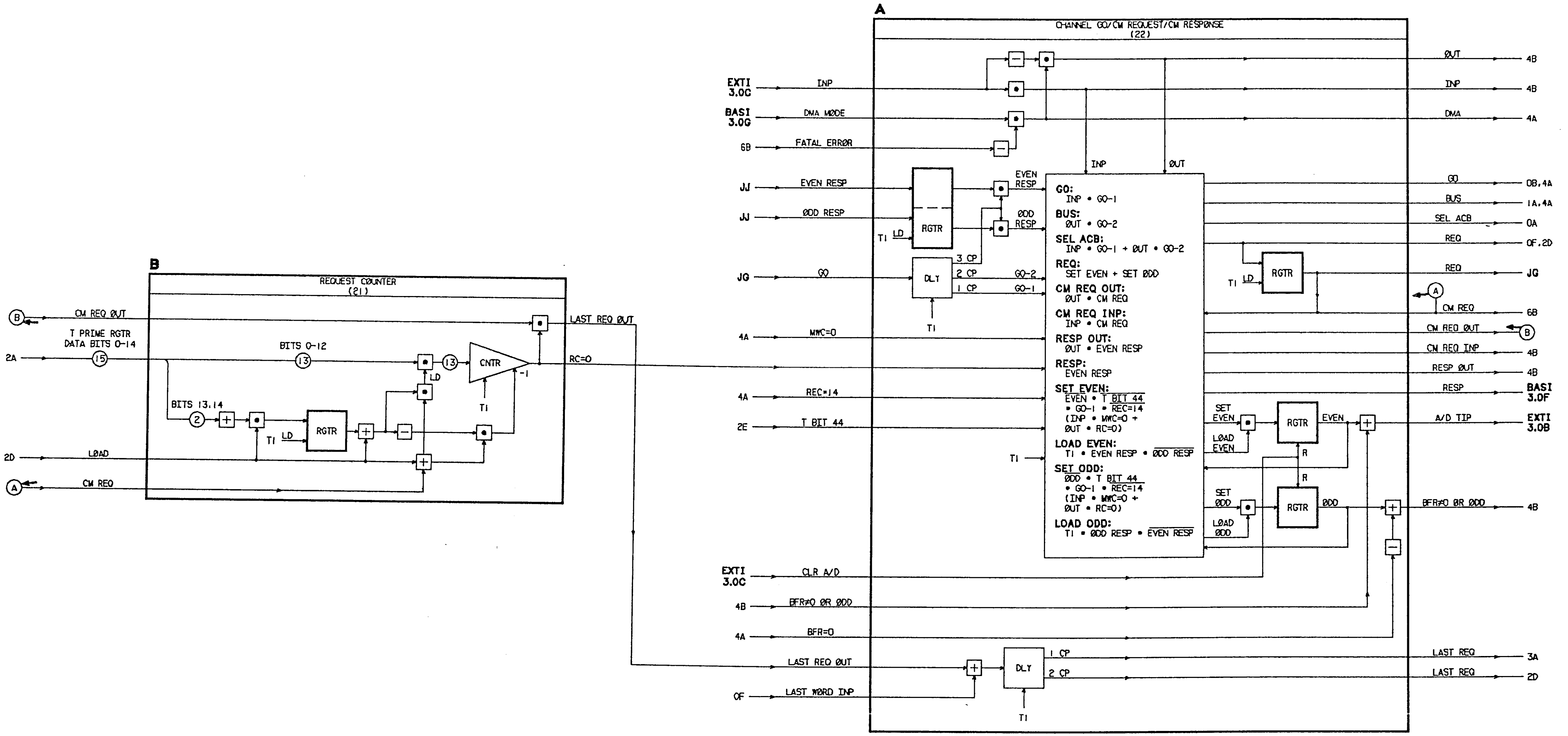
A/D-IPI 3.3



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JT)
CHANNEL WORD, CW WORD,
RESPONSE, AND
ADRS COUNTERS

DWG NO 60463540
REV F
SHEET A/D-IPI 3.4



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
ASSEMBLY/DISASSEMBLY
CONTROL

CODE IDENT	DWG NO	REV
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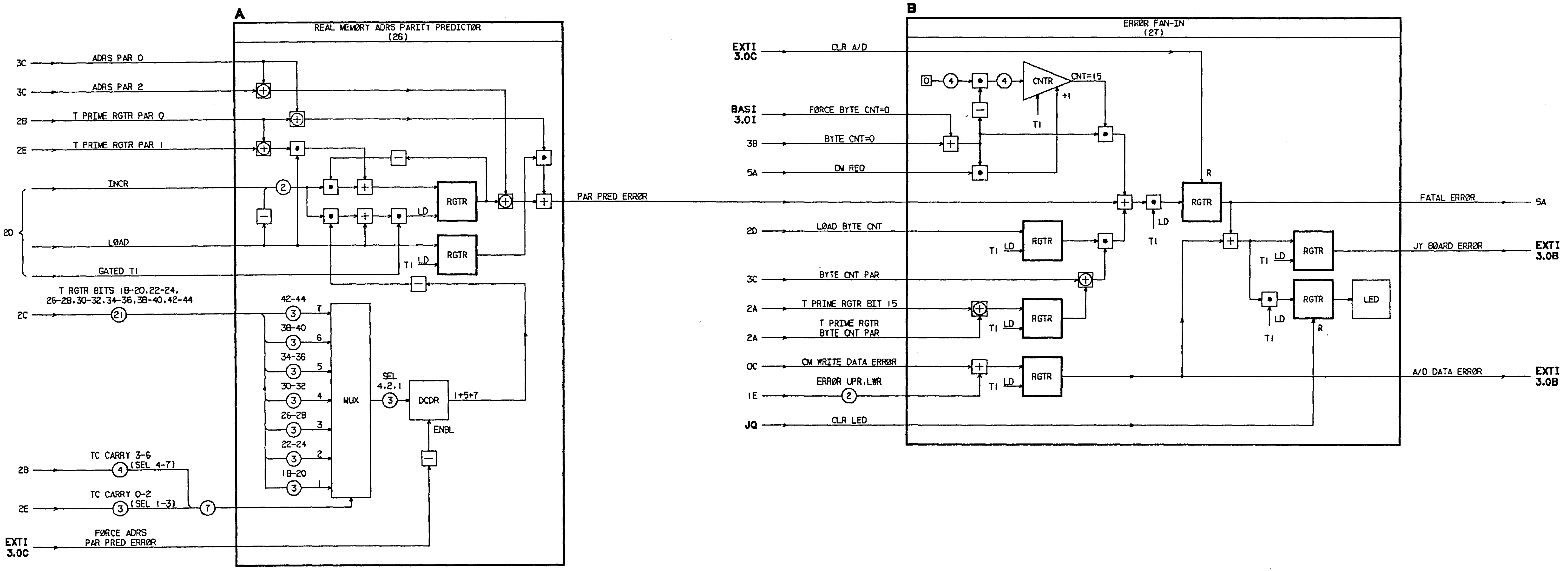
A/D-IPI 3.5	



CONTROL DATA
DEVELOPMENT DIVISION

LEVEL 3 DIAGRAM (JY)
ERROR DETECTOR

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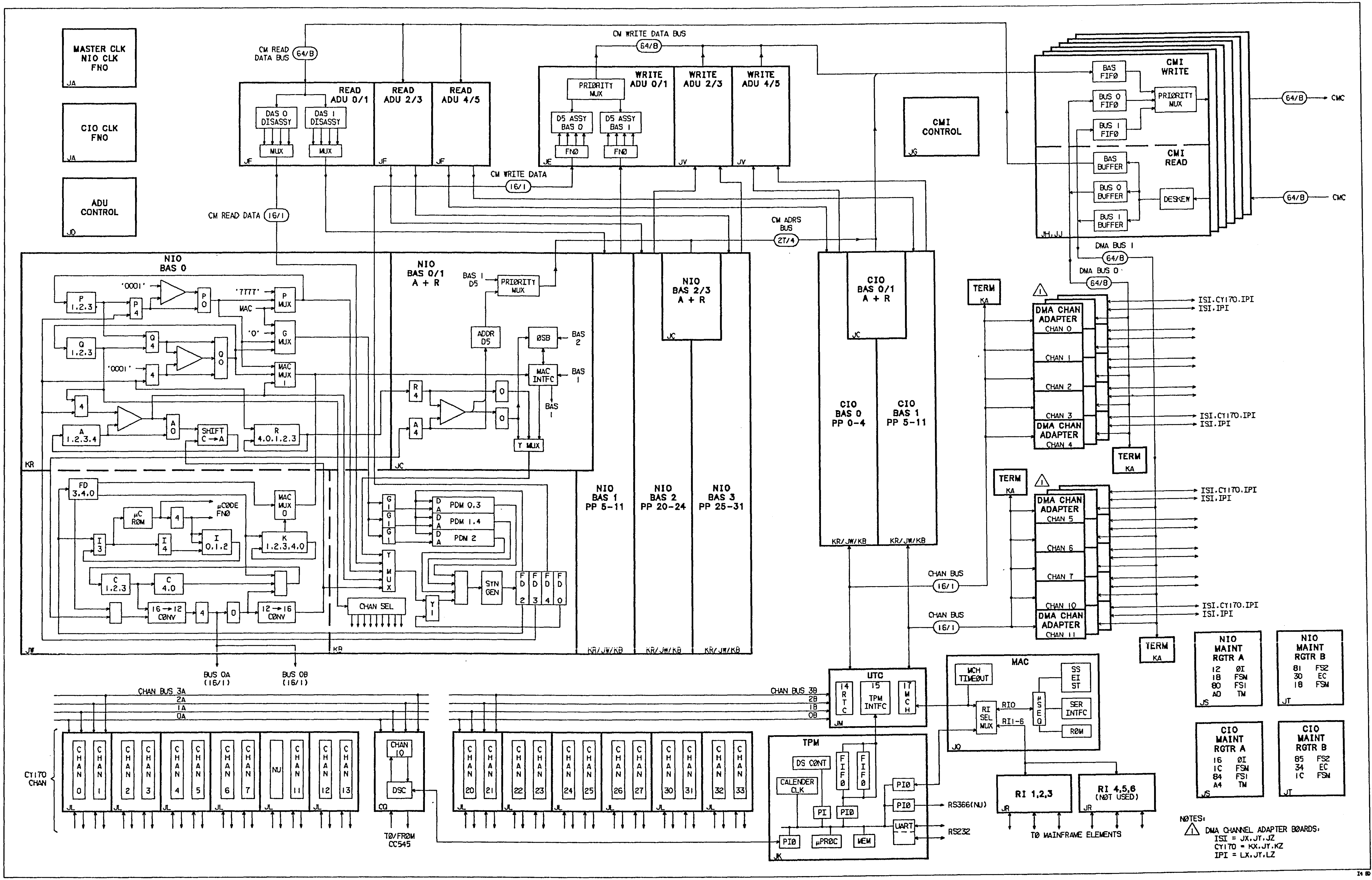
A/D-IPI 3.6	



IOU BLOCK DIAGRAM

ABBREVIATIONS

B

ACA, B	address counter A, B
ACK	acknowledge
ACT	active
A/D	assembly/disassembly
ADRS	address
ADU	assembly/disassembly unit
ASCII	american standard code for information interchange
ASSY	assembly
ASTIG	astigmatism
BAS	barrel and slot; barrel
BASI	barrel and slot interface
BFR	buffer
BSR	bit significant response
BOUND	boundary
BTF	branch test failed
CAL	calendar
CHAN	channel
CHAR	character
CI	cache invalidate
CIO	concurrent input/output
CLK	clock
CLR	clear
CM	central memory
CMC	central memory control
CMD	command
CMI	central-memory interface
CMPR	compare
CNT	count
CNTR	counter
CONT	control
COR	corrected
CP	clock period
CPU	central processing unit
CRT	cathode-ray tube
CWC	channel word counter
DCDR	decoder
DECR	decrement
DISASSY	disassembly
DLY	delay

UNDERLINED: Abbreviation always used.

DMA	direct-memory access
DMT	deadman timeout
DS	deadstart
DSBL	disable
DSC	display station controller
EC	environmental control
ECL	emitter-coupled logic
EI	error in
EID	element identifier
ENBL	enable
EPROM	erasable programmable read-only memory
ESM	extended semiconductor memory
EXCH	exchange
EXTI	external interface
FCTN	function
FF	flip-flop
FIFO	first-in first-out
FNI	fanin
FNO	fanout
FS1, 2	fault status 1, 2
GEN	generator
HLDG	holding
ICI	integrated control interface
INACT	inactive
INCR	Increment
INH	inhibit
INP	input
INTRPT	interrupt
INV	invert
IOU	input/output unit
I/O	input/output
IPI	intelligent peripheral interface
ISI	intelligent standard interface
LDS	long deadstart sequence
LED	light-emitting diode
LWR	lower
MAC	maintenance access control
MAINT	maintenance
MC	master clear
MCC	major cycle
MCH	maintenance channel

MED	medium
MEM	memory
MHz	megahertz
MRA, B	maintenance register A, B
MUX	multiplexer
MWC	CM word counter
NCODE	nanocode
NIO	noncurrent input/output
ns	nanosecond
OI	options installed
OP	operand
OPCODE	operation code
OS	operating system
OSB	operating system bounds
OSC	oscillator
OUT	output
OVFL	overflow
P	program address
PAL	programmable array logic
PAR	parity
PC	parcel counter
PE	parity error
PP	peripheral processor
PPM	peripheral-processor memory
PROM	programmable read-only memory
PRED	predictor
PWR	power
RAM	random-access memory
RC	request counter
REC	response counter
RCVR	receiver
ROC	CM request output counter
RDY	ready
RECONFIG	reconfiguration
REGEN	regenerated, regenerator
REQ	request
RESP	response
RESYNC	resynchronize, resynchronizer, resynchronization
RGTR	register
RI	radial interface
RMA	real memory address
ROM	read-only memory
RTC	real time clock
SECDED	single-error correction/double-error detection
SEL	select
SEQ	sequence
SIG	signficant
SML	small
SUBTR	subtract
SYNC	synchronize
TC	T counter
TIP	transfer in progress
TM	test mode
TPM	two-port mux
TTL	transistor-transistor logic
T1	time 1
UART	universal asynchronous receiver/transmitter
uCODE	microcode
uSEC	microsecond
UNCOND	unconditional
UNCOR	uncorrectable
UPR	upper
UTC	utility channel
XFER	transfer
XLTR	translator
XMTR	transmitter

UNDERLINED: Abbreviation always used.

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L0-L3 Theory/Diagrams
Hardware Maintenance Manual, Volume 1

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